DALTA IMAM MAULANA

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EDUCATION

Doctor of Philosophy in Electrical Engineering 2022 - Present
Korea Advanced Institute of Science and Technology, South Korea
Advisor: Wanyeong Jung

Master of Science in Electrical Engineering 2020 - 2022
Korea Advanced Institute of Science and Technology, South Korea
Thesis: An Energy Efficient Asynchronous Interface with Delay Insensitive Protocol for Globally Asynchronous Locally Synchronous (GALS) System
Advisor: Wanyeong Jung

Bachelor of Science in Electrical Engineering 2015 - 2019
Bandung Institute of Technology, Indonesia
Honor: *cum laude* (GPA: 3.85 / 4.00)
Thesis: Design and Implementation of Data Processing Subsystem for In-Store Traffic Monitoring System
Advisor: Trio Adiono

RESEARCH EXPERIENCE

Graduate Research, Smart and Energy Efficient Design Lab August 2020 - Present
Korea Advanced Institute of Science and Technology, South Korea

- Create energy-efficient and high bandwidth asynchronous link for Globally Asynchronous Locally Synchronous (GALS) system.
- Designed near memory radix sort accelerator on Xilinx SoC device.

Research Assistant, IC Design Laboratory September 2019 - July 2020
Bandung Institute of Technology, Indonesia

- Designed hardware accelerator for real time object detection using Tiny YOLO algorithm on Xilinx SoC device.
- Implemented Sobel filter algorithm on Xilinx SoC device.

Undergraduate Research, Department of Electrical Engineering July 2018 - July 2019
Bandung Institute of Technology, Indonesia

- Designed and implemented deep neural network for pre-seizure detector on FPGA device.
- Designed 8-bit radix-4 parallel booth multiplier integrated circuit (IC) layout using Mentor Graphics software.

WORK EXPERIENCE

Head Teaching Assistant, EL2102 - Digital System Laboratory September 2018 - December 2018
Bandung Institute of Technology, Indonesia

- Planned and managed training session for digital system lab assistants.
- Taught preliminary lab course to sophomore year students.

Embedded Systems Engineer Intern May 2018 - August 2018
Fusi Global Teknologi, Indonesia

- Created Android application for disaster warning system IoT project.
- Coordinated with other engineer to design hardware and software subsystems.

Teaching Assistant, EL2102 - Electronics Laboratory February 2018 - May 2018
Bandung Institute of Technology, Indonesia

- Assisted second year students in electronics lab course.
- Graded electronics lab course assignments.

PUBLICATIONS

Conference Papers

Maulana, Dalta I. and Wanyeong Jung, "An Energy-Efficient Delay Insensitive Asynchronous Interface for Globally Asynchronous Locally Synchronous (GALS) System," IEEE International Symposium on Circuits and Systems (ISCAS), 2023

Da Won Kim, **Maulana, Dalta I.**, and Wanyeong, Jung. "Kyber Accelerator on FPGA Using Energy-Efficient LUT-Based Barrett Reduction." IEEE International SoC Design Conference (ISOCC), 2022

Jihwan, Cho, **Maulana, Dalta I.**, and Wanyeong, Jung. " A Near-Memory Radix Sort Accelerator with Parallel 1-bit Sorter." IEEE International Symposium On Field-Programmable Custom Computing Machines (FCCM), 2022

Atmaja, P., **Maulana, Dalta I.**, and Adiono, T. " AI-based Customer Behaviour Analytics System using Edge Computing Device." International Conference on Electronics, Information, and Communication (ICEIC), 2020

Maulana, Dalta I., Amaral, S.T., Putri, D. N. F, and Adiono, T. "Artificial Intelligence Based In-Store Traffic Monitoring System for Evaluating Retail Performance." Proceedings of IEEE Global Conference on Consumer Electronics (GCCE), 2019

Tahar, C., **Maulana, Dalta I.**, Pandia, R. R. S, and Adiono, T. "FPGA Implementation of Deep Neural Network for Wearable Pre-Seizure Detector on Epileptic Patient." Proceedings of International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTICON), 2019

PROJECTS

Cluster Graph Attention Network, EE595 - Parallel Computer Architecture

- Implemented graph attention network with data clustering technique.
- Reduced memory consumption and training time for large datasets training.
- Trained and verified the model using Reddit dataset.

Dogleg Channel Router, EE574 - CAD for VLSI

- Implemented dogleg channel routing with constrained left edge algorithm (LEA) using C++.
- Able to route up to 10 pairs of pins without track overlap.

PROFESSIONAL AFFILIATION

Student member 2020 - Present
Institute of Electrical and Electronics Engineer (IEEE)

CERTIFICATION

ETS TOEFL iBT December 2019
Vista International Programs, Bandung, Indonesia
Score: 102

SKILLS

Programming Languages	Python, C, C++, Java, MATLAB
Hardware Description Languages	Verilog, VHDL
Engineering Tools	Cadence Virtuoso, Synopsys Design Compiler, Fusion360

LANGUAGES

Indonesian	Native
English	Proficient
Korean	Basic