San Diego State University
CS 370 Computer Architecture

Homework Assignment 2 [100 points, Weight 4%]

- You are required to write by hand legibly to solve each problem. When you plot a circuit, please make sure that you use a ruler. You are not allowed to use any software to draw a circuit or answer any question. An answer that is not written by your hand will receive zero credit for the corresponding problem.
- Please write down your full name and SDSU Red ID on the first scratch paper. After you finish writing all your answers on multiple scratch papers (print papers preferred), please take a photo for each of them. Next, please insert these image files into a Word file. Finally, convert the Word file into a single PDF file, and then, submit the PDF file from within Canvas.
- Please note that we only accept your PDF file submissions. A submission in any other format will not be graded and will receive zero credit. For example, submitting multiple image files will receive zero credit.
- Please pay special attention to the due date – a late submission will receive zero.
- For your convenience, the text of each question is appended to this document.
- Please do the following problems from the textbook, and submit solutions.

1. [15 points] Problem 4-6 (the circuit takes 5 points, the state table takes 5 points, the state diagram takes 5 points)
2. [15 points] Problem 4-7 (the state table is 5 points, each part of the two state diagrams is 5 points; **hint:** you need to draw two state diagrams, one is in the case of X=0, the other is in the case of X=1)
3. [15 points] Problem 4-12 (a)
4. [20 points] Problem 4-17 (10 points for the state table, 10 points for the circuit)
5. [15 points] Problem 6-8 (each sub-qestion is 5 points)
6. [20 points] Problem 6-12 (each sub-question is 10 points)

4-6. A sequential circuit with two D flip-flops A and B, two inputs X and Y, and one output Z is specified by the following input equations:

$$D_A = XA + \overline{X}\,\overline{Y},\quad D_B = XB + \overline{X}A,\quad Z = \overline{X}B$$

(a) Draw the logic diagram of the circuit.

(b) Derive the state table.

(c) Derive the state diagram.

(d) Is this a Mealy or a Moore machine?

4-7. *A sequential circuit has three D flip-flops A, B, and C, and one input X. The circuit is described by the following input equations:

$$D_A = (B\overline{C} + \overline{B}C)X + (BC + \overline{B}\,\overline{C})\overline{X}$$

$$D_B = A$$

$$D_C = B$$

(a) Derive the state table for the circuit.

(b) Draw two state diagrams, one for $X = 0$ and the other for $X = 1$.

4-12. A sequential circuit is given in Figure 4-13.

(a) Add the necessary logic and/or connections to the circuit to provide an asynchronous reset to state $A = 1, B = 0$ for signal $Reset = 0$.

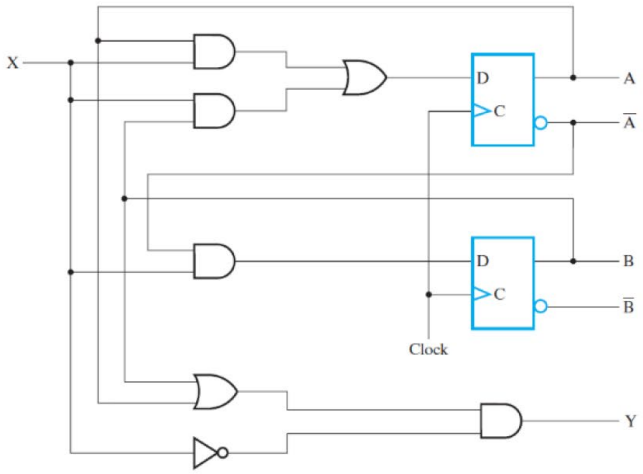

FIGURE 4-13
Example of a Sequential Circuit

4-17. A sequential circuit for a luggage lock has ten pushbuttons labeled 0, 1, 2, 3, 4, 5, 6, 7, 8, and 9. Each pushbutton 0 through 9 produces a 1 on $X_i, i = 0$ through 9, respectively, with all other values on variable $X_j, j \neq i$, equal to 0. Also, these ten pushbuttons produce a positive pulse on the clock C for clocking the flip-flops in the circuit. The circuitry that produces the X_i signals and the clock C has already been designed. The lock opens in response to a sequence of four X_i values, $i = 0, \ldots, 9$, set by the user. The logic for connecting the four selected X_i values to variables X_a, X_b, X_c, and X_d has also been designed. The circuit is locked and reset to its initial state by pushing pushbutton *Lock*, which provides L, the asynchronous reset signal for the circuit. The lock is to unlock in response to the sequence X_a, X_b, X_c, X_d, regardless of all past inputs applied to it since it was reset. The circuit has a single Moore type output U which is 1 to unlock the lock, and 0 otherwise. Design the circuit with inputs X_a, X_b, X_c, and X_d, reset L, clock C, and output U. Use a one-hot code for the state assignment. Implement the circuit with D flip-flops and AND gates, OR gates, and inverters.

6-8. How many flip-flop values are complemented in an 8-bit binary ripple counter to reach the next count value after:

(a) 11111111? **(b)** 01100111? **(c)** 01010110

6-12. **(a)** Using the synchronous binary counter of Figure 6-14 and an AND gate, construct a counter that counts from 0000 through 1010.

(b) Repeat for a count from 0000 to 1110. Minimize the number of inputs to the AND gate.

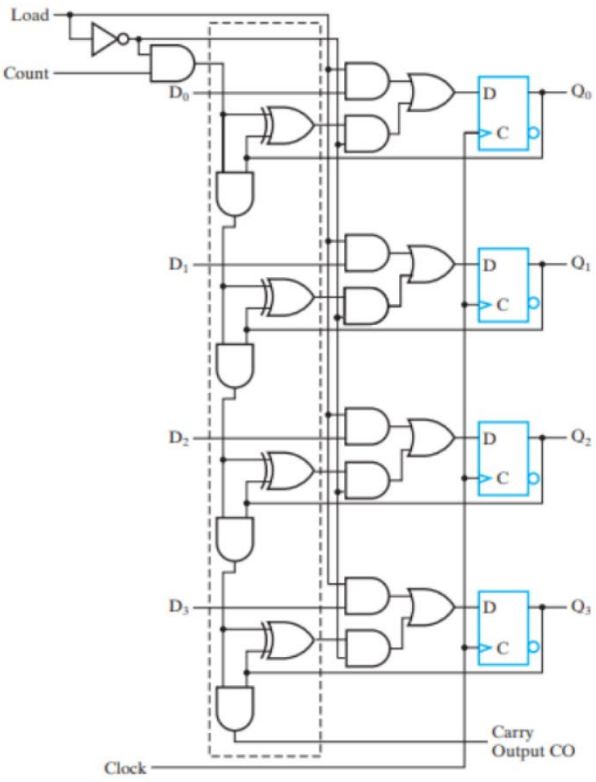

FIGURE 6-14
4-Bit Binary Counter with Parallel Load