EE445L – Lab6: Introduction to PCB Design

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2/18/14

OBJECTIVES

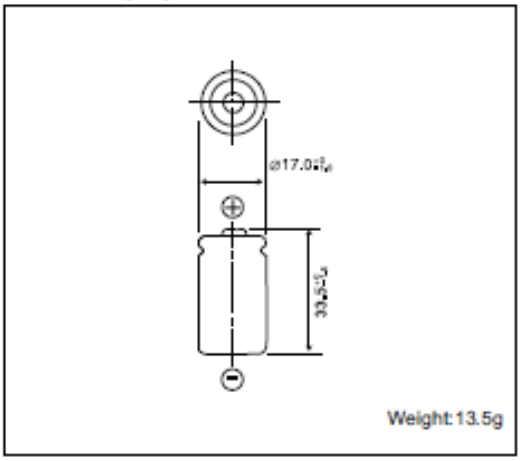
The objective for this lab is system level approach to embedded system design. We will implement a PCB layout, consider the mechanics, understand available parts, consider the costs, and consider the power. We will also need to figure out how to test our PCB design to make sure it is working.

HARWARE DESIGN
Battery Description

Poly-carbonmonofluoride Lithium Batteries: Individual Specifications

BR-2/3AG

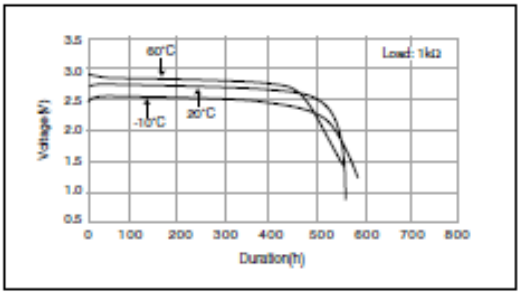
■ Dimensions(mm)



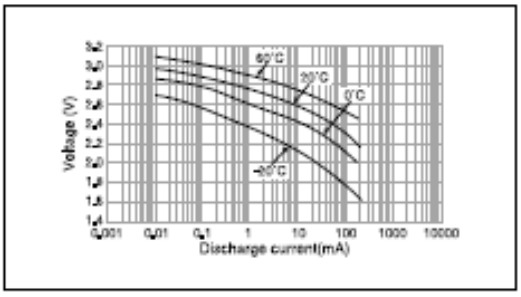
■ Specification

Nominal voltage (V)	3
Nominal capacity (mAh)	1,450
Continuous standard load (mA)	2.5
Operating temperature (C)	-40 ~ +85

■ Temperature Characteristics

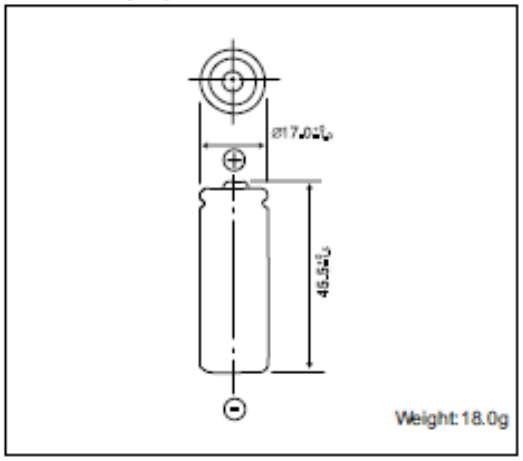


■ Operating voltage vs. Discharge current(voltage at 50% discharge depth)



BR-A

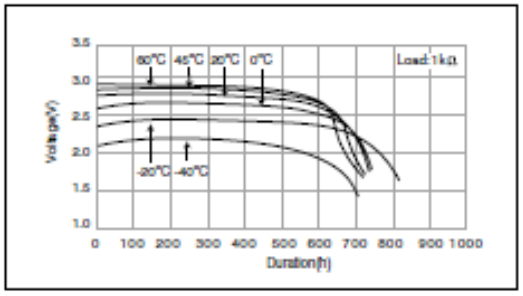
■ Dimensions(mm)



■ Specification

Nominal voltage (V)	3
Nominal capacity (mAh)	1,800
Continuous standard load (mA)	2.5
Operating temperature (C)	-40 ~ +85

■ Temperature Characteristics



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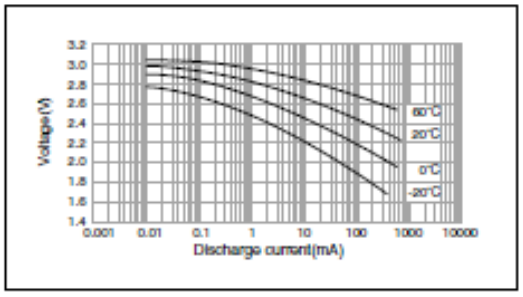
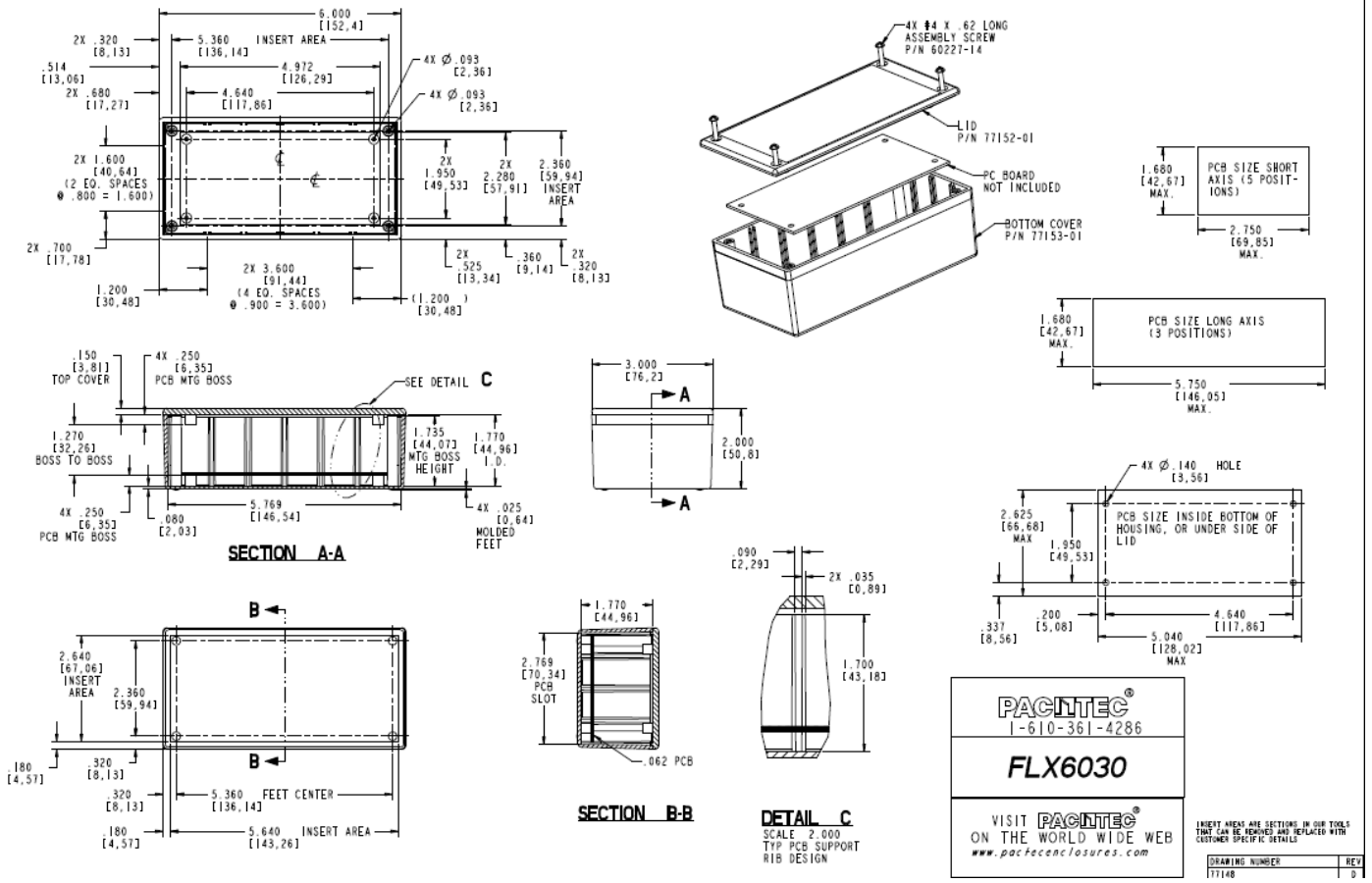


Box Description



Created Component

Dual-Channel, 16-Bit, 800 MSPS, Digital-to-Analog Converter (DAC)

Check for Samples: DAC3283

FEATURES

- Dual, 16-Bit, 800 MSPS DACs
- 8-Bit Input LVDS Data Bus
  - Byte-Wide Interleaved Data Load
  - 8 Sample Input FIFO
  - Optional Data Pattern Checker
- Multi-DAC Synchronization
- Selectable 2x-4x Interpolation Filters
  - Stop-Band Attenuation > 85 dB
- Fs/2 and ± Fs/4 Coarse Mixer
- Digital Quadrature Modulator Correction
  - Gain, Phase and Offset Correction
- Temperature Sensor
- 3- or 4-Wire Serial Control Interface
- On-Chip 1.2-V Reference
- Differential Scalable Output: 2 to 20 mA
- Single-Carrier TM1 WCDMA ACLR: 82 dBc at f_{OUT} = 122.88 MHz
- Low Power: 1.3 W at 800 MSPS
- Space Saving Package: 48-pin 7×7mm QFN

APPLICATIONS

- Cellular Base Stations
- Diversity Transmit
- Wideband Communications
- Digital Synthesis

DESCRIPTION

The DAC3283 is a dual-channel 16-bit 800 MSPS digital-to-analog converter (DAC) with an 8-bit LVDS input data bus with on-chip termination, optional 2x-4x interpolation filters, digital IQ compensation and internal voltage reference. The DAC3283 offers superior linearity, noise and crosstalk performance.

Input data can be interpolated by 2x or 4x through on-chip interpolating FIR filters with over 85 dB of stop-band attenuation. Multiple DAC3283 devices can be fully synchronized.

The DAC3283 allows either a complex or real output. An optional coarse mixer in complex mode provides frequency upconversion and the dual DAC output produces a complex Hilbert Transform pair. The digital IQ compensation feature allows optimization of phase, gain and offset to maximize sideband rejection and minimize LO feed-through of an external quadrature modulator performing the final single sideband RF up-conversion.

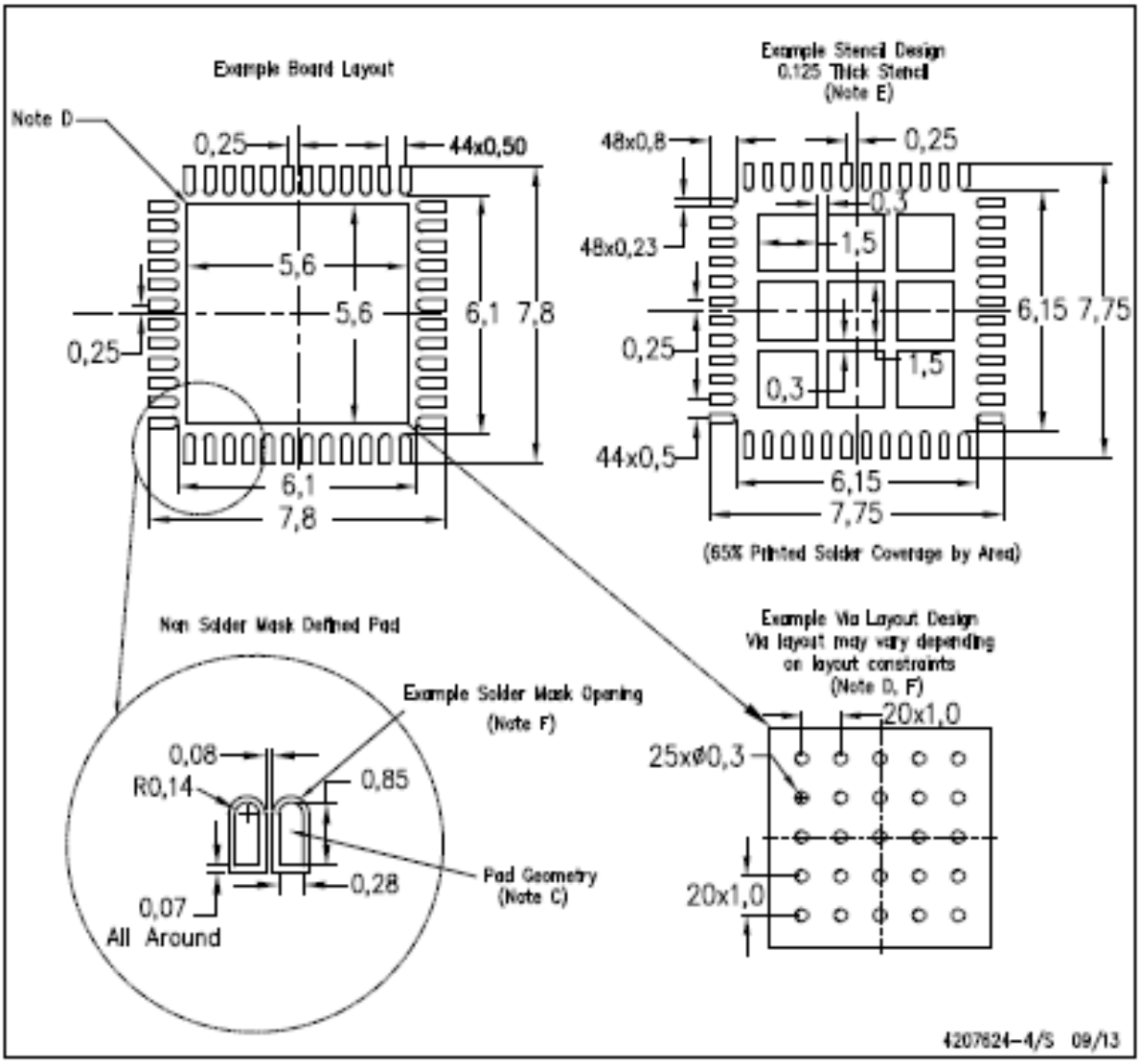
The DAC3283 is characterized for operation over the entire industrial temperature range of –40°C to 85°C and is available in a 48-pin 7×7mm QFN package.

ORDERING INFORMATION

T_A	ORDER CODE	PACKAGE DRAWING/TYPE (1) (2) (3)	TRANSPORT MEDIA	QUANTITY
–40°C to 85°C	DAC3283IRGZT	RGZ/64QFN Quad Flatpack No-Lead	Tape and Reel	250
	DAC3283IRGZR			2000

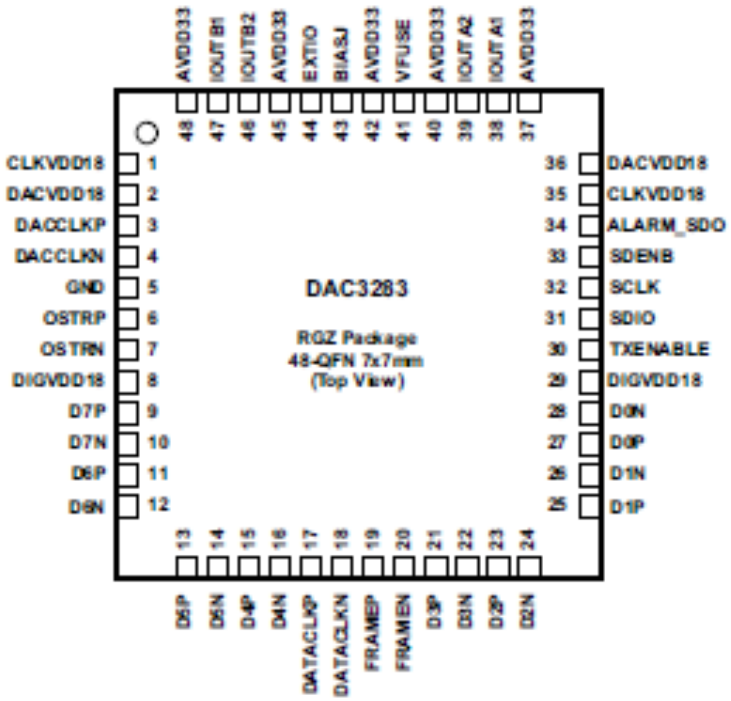
(1) Thermal Pad Size: 5,6 mm × 5,6 mm
(2) MSL Peak Temperature: Level-3-260C-168 HR
(3) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

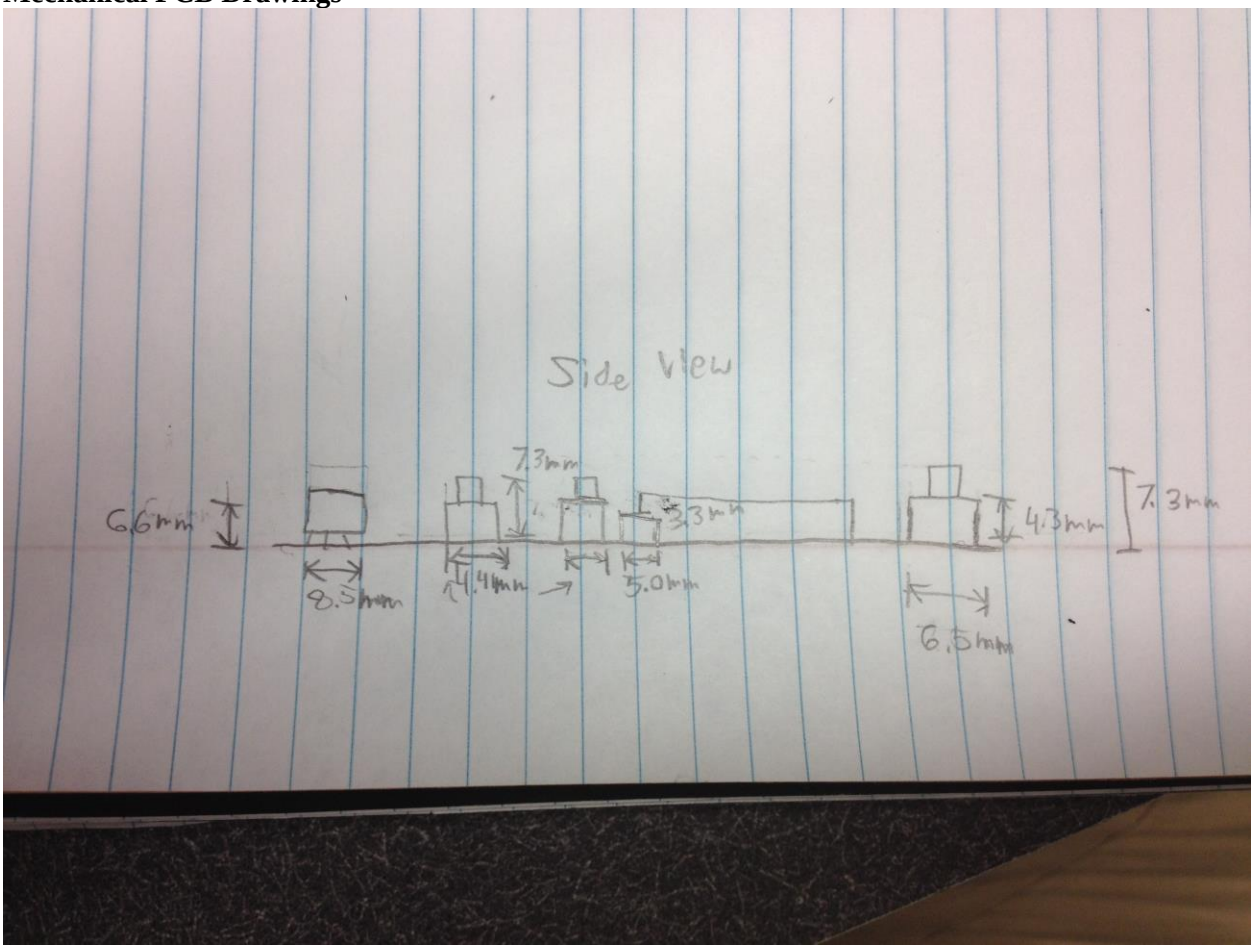
DAC3283
RGZ PACKAGE
(TOP VIEW)

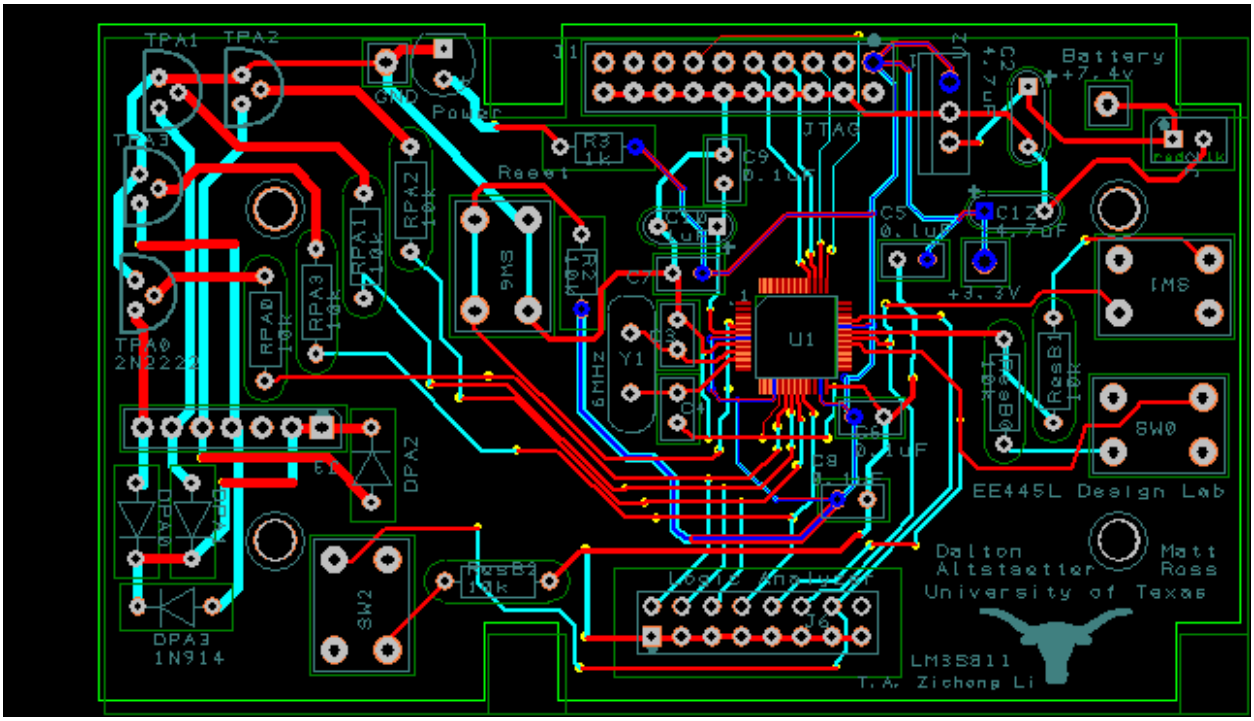


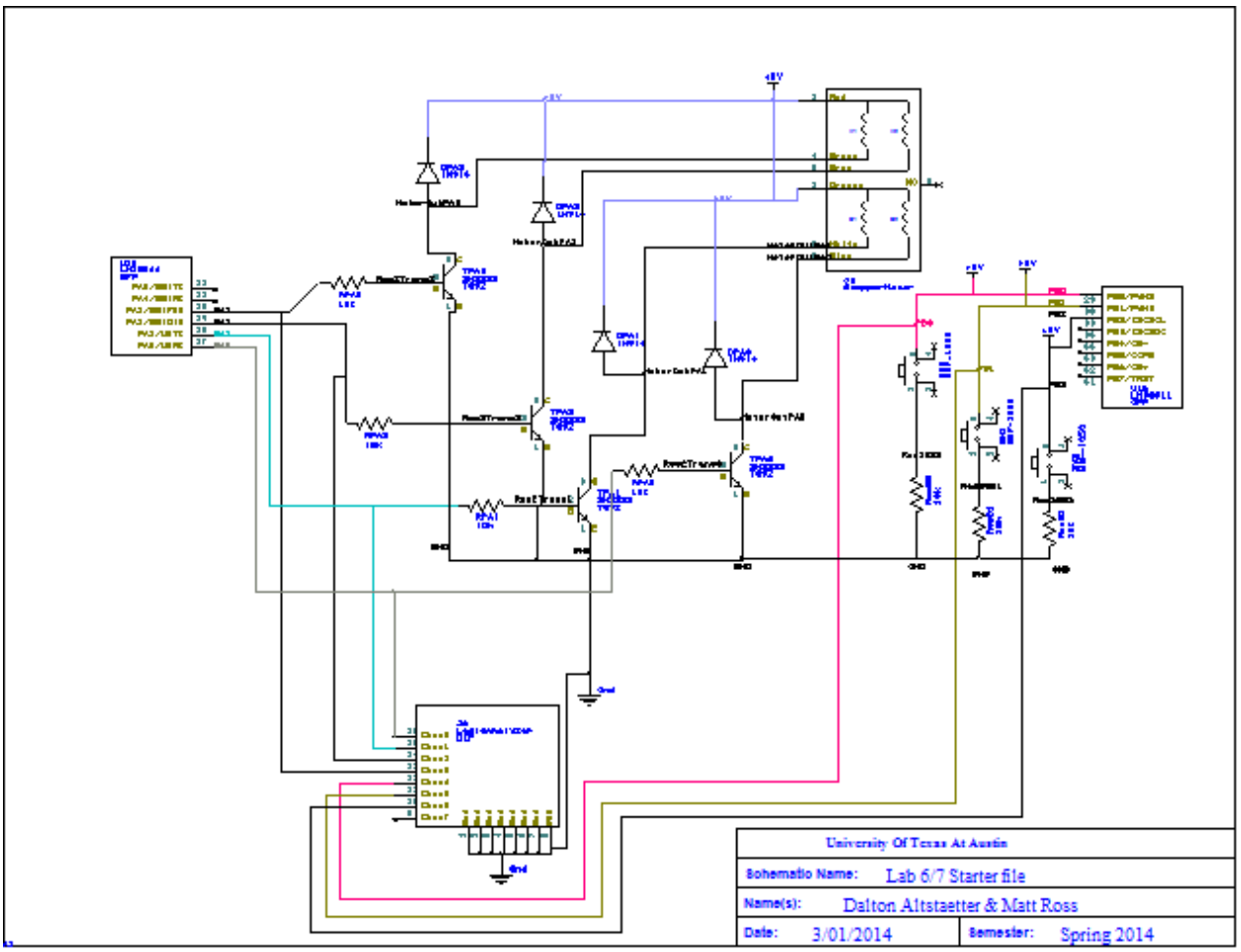
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AVDD33	37, 40, 42, 45, 48	I	Analog supply voltage. (3.3 V)
ALARM_SDO	34	O	1.8V CMOS output for ALARM condition. The ALARM output functionality is defined through the CONFIG6 register. Default polarity is active low, but can be changed to active high via CONFIG0 **alarm_pol** control bit. Optionally, it can be used as the uni-directional data output in 4-pin serial interface mode (CONFIG 23 **sif4_ena** = '1').
BIASJ	43	O	Full-scale output current bias. For 20mA full-scale output current, connect a 960Ω resistor to GND.
CLKVDD18	1, 35	I	Internal clock buffer supply voltage. (1.8 V) It is recommended to isolate this supply from DACVDD18 and DIGVDD18.
D[7...0]P	9, 11, 13, 15, 21, 23, 25, 27	I	LVDS positive input data bits 0 through 7. Each positive/negative LVDS pair has an internal 100 Ω termination resistor. Data format relative to DATACLKP/N clock is Double Data Rate (DDR) with two data transfers per DATACKP/N clock cycle. Dual channel 16-bit data is transferred byte-wide on this single 8-bit data bus using FRAMEP/N as a frame strobe indicator. D7P is most significant data bit (MSB) – pin 9 D0P is least significant data bit (LSB) – pin 27 The order of the bus can be reversed via CONFIG19 **rev** bit.
D[7...0]N	10, 12, 14, 16, 22, 24, 26, 28	I	LVDS negative input data bits 0 through 15. (See D[7:0]P description above) D7N is most significant data bit (MSB) – pin 10 D0N is least significant data bit (LSB) – pin 28
DACCLKP	3	I	Positive external LVPECL clock input for DAC core with a self-bias of approximately CLKVDD18/2.
DACCLKN	4	I	Complementary external LVPECL clock input for DAC core. (see the DACCLKP description)
DACVDD18	2, 36	I	DAC core supply voltage. (1.8 V) It is recommended to isolate this supply from CLKVDD18 and DIGVDD18.

Mechanical PCB Drawings




TPA1
TPA2
TPA3
TPA0
2N2222
GND
Power
Reset
JTAG
Battery
+7.4v
+3.3V
U1
Y1
6MHz
SW1
SW2
SW0
DPA2
DPA3
1N914
EE445L Design Lab
Dalton
Altstaetter
Matt
Ross
University of Texas
LM3S811
T.A. Zicheng Li


University Of Texas At Austin
Schematic Name: Lab 6/7 Starter file
Name(s): Dalton Altstaetter & Matt Ross
Date: 3/01/2014
Semester: Spring 2014

MEASUREMENT DATA

Bill of Materials

Component	Package	Price	Manuf	Man Part No	Ref Name	Qty	Estimated Current
0.25Wresistor	DIP				GPIO Res	7	0.5 mA
0.125Wresistor	DIL				R2 R3	2	0.33 mA
1N914	MISC				Diode	4	5.41 A
2N2222	TO92				Transistor	4	111 mA
B3F-1050	DIP				Switch	4	0.5 mA
Ceramic	C				Capacitor	7	0
Header2	SIP				J2	1	0
JTAG	USER		AllElectronics	DHS-40	J1	1	
LEDT1.75	SIP				Power	1	1.8 mA
LM3S811	QFP				U1	1	
LM2937ET-3.3	TO220				U2	1	0
LogicAnalyzer	DIP				J6	1	
Mammond1593Y	MISC				Box1	1	
StepperMotor	SIL7				J3	1	300 mA
tantalum	C				C2 C10 C12	3	0
testpoint	SIP				GND	1	
	SIP		+3.3V		TP2	1	
	SIP		+7.4v		Battery	1	
XTAL	DSC				Y1	1	
Battery		8.75	Panasonic	BR-A	Battery	1	500 mA
Box		5.42			77347-501-028	1	
Total						45	

Battery = 4 * 500mA = 2000mAh

ANALYSIS AND DISCUSION

Load our lab4 code. Plug in the battery and stepper motor. Test the functionality of each switch.