McMaster University

Instruction Scheduling - A Complicated Mess

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Instruction Scheduling

Problem: Given a set of instructions and dependencies, designate an order (find a *schedule*) satisfying the dependencies and optimizing performance

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Known **NP-Complete** problem, practically solved by

- Heuristics
- Approximation Algorithms

Types of Scheduling

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- **Basic Block:** break code into blocks within branches **(most commonly performed scheduling)**
- **Global Scheduling:** schedule across basic block boundaries
- **Modulo Scheduling:** an algorithm to increase pipelining of loops by interleaving different iterations
- **Trace Scheduling:** tries to optimize control flow by predicting routes taken on branches

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Classic RISC Pipeline

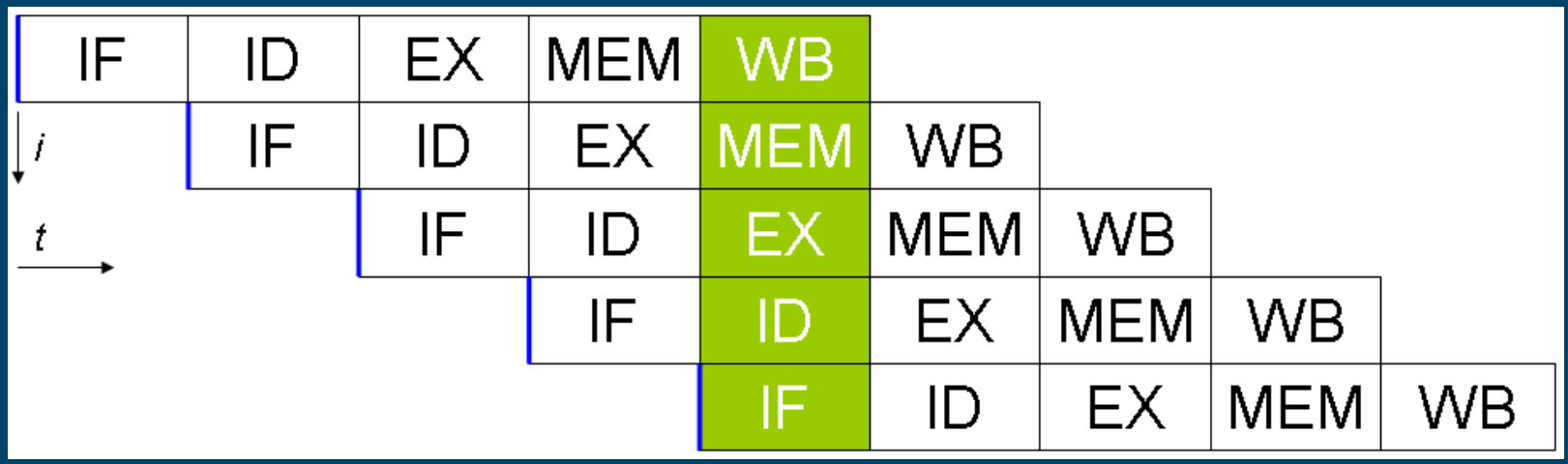

Figure: Example Pipeline

SuperScaler Pipelining

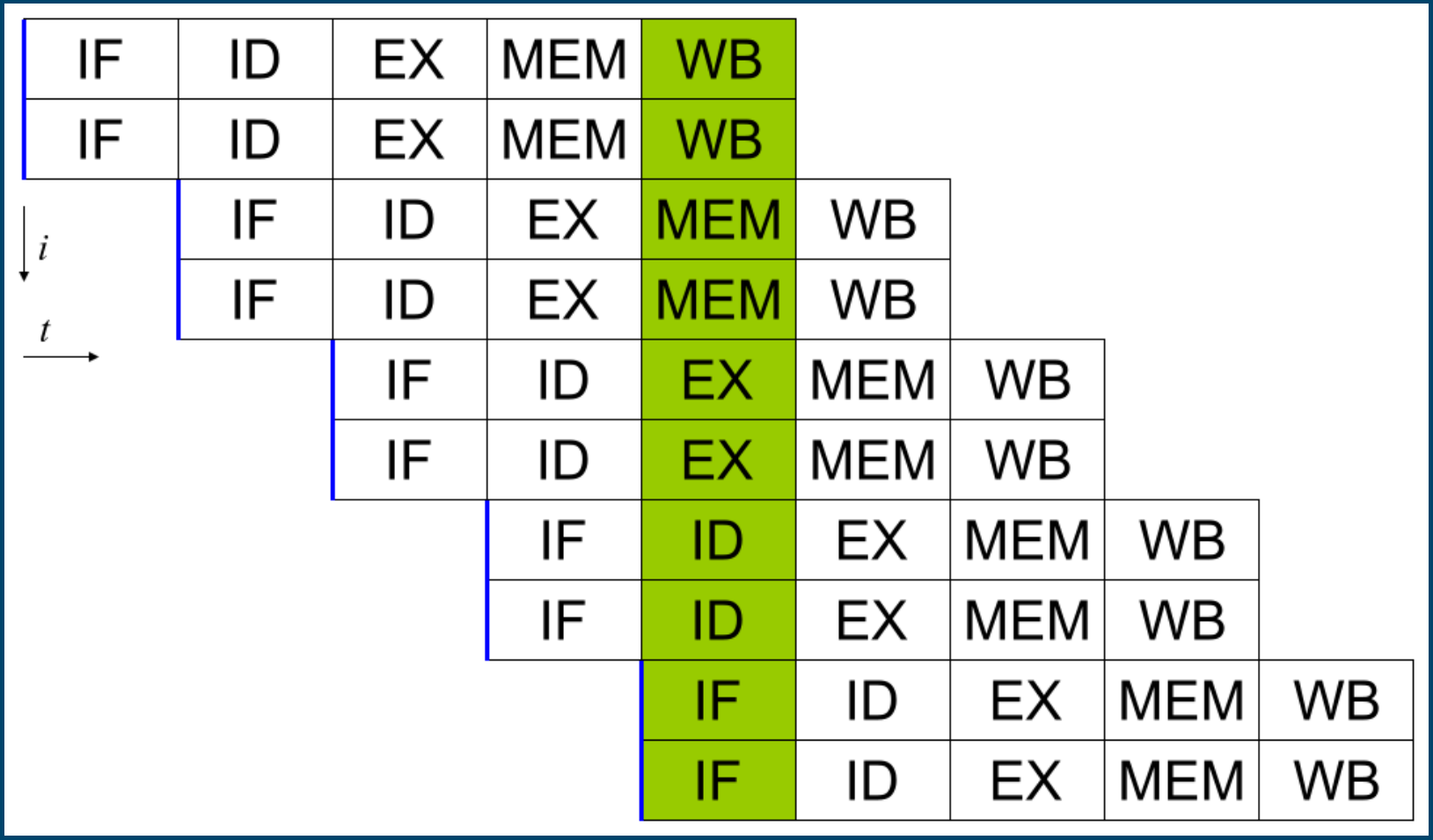

Figure: Example SuperScaler Pipeline

Hazards

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  - read after write (RAW)
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- **Structural Hazards** - occurs when an aspect of hardware is accessed at the same time

- **Control Hazards** - caused by branching, next instruction unknown

Pipeline Stalls / Bubbles

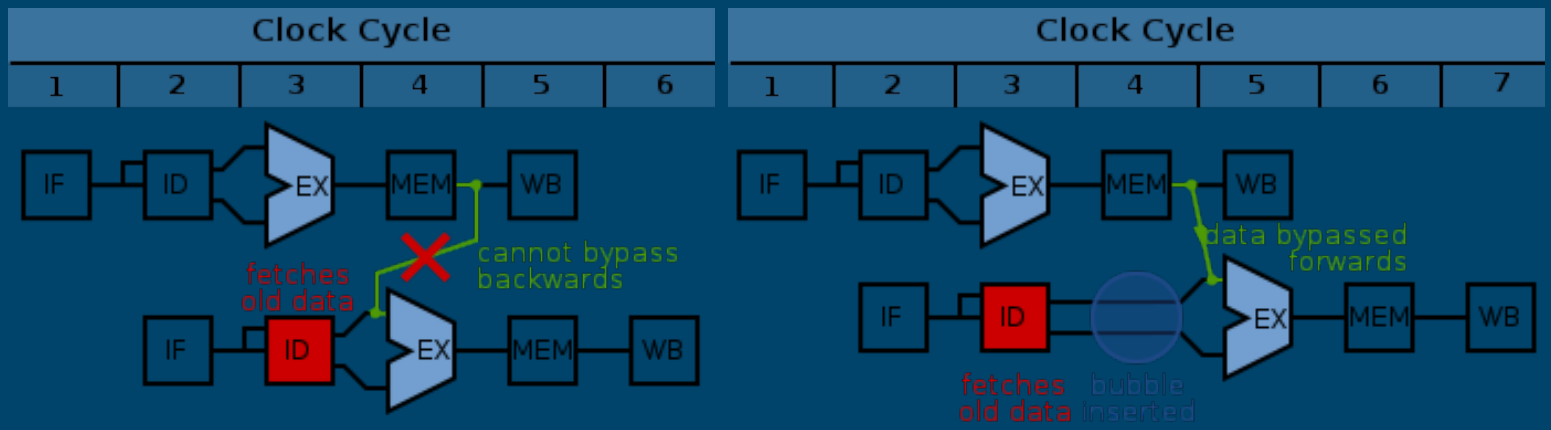

Figure: Pipeline Stall

A **Ideal Schedule** contains NO bubbles (often not possible)

Out-of-order Execution

1. Instruction fetch
2. Dispatch to instruction queue
3. Instruction waits until its input is available, then allowed to leave queue (in whatever order)
4. Instruction is executed
5. Results are queued
6. Only after all older instructions have their results written back to registers, the instruction's result is written back to registers

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Register Allocation

Problem: Given a schedule, assign registers keeping in mind

- limited # of registers
- can't rewrite a register until consumed by dependent instructions

Once again, known **NP-Complete** problem. Practically solved by using non-optimal **Graph Coloring** problems

Graph Coloring

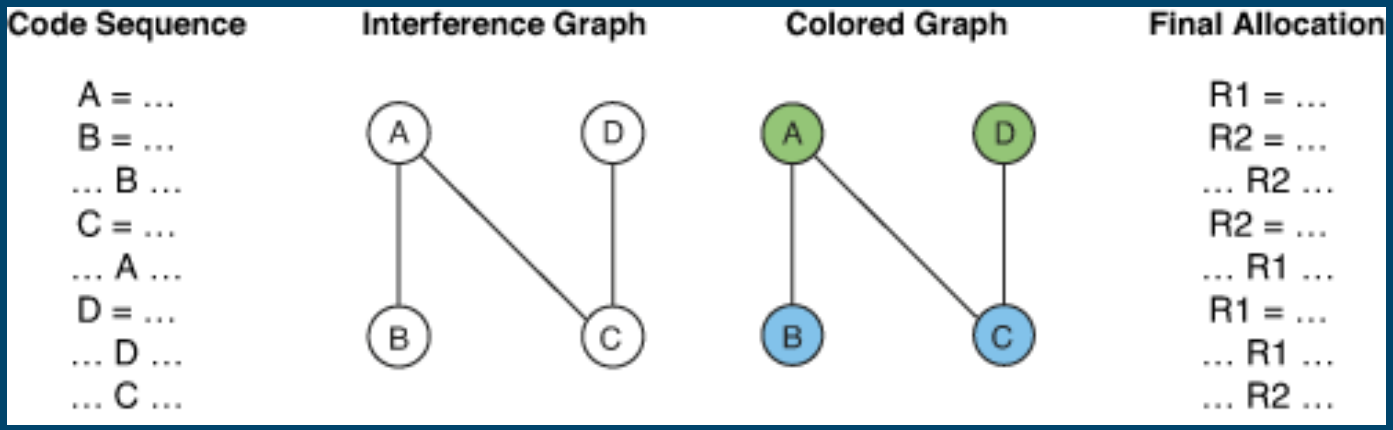

Figure: Register Allocation via Graph Coloring

Find a **k-Coloring** for the interference graph, where $k = \#$**Registers**

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- What if a **k-Coloring** can't be found? Must **Spill** memory
- Simply insert new **Load / Store** instructions as needed
- Potentially **creates new bubbles** in the pipeline, need to re-perform scheduling
- An **Ideal Schedule** has no spilling

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List Scheduling

Simple heuristic. Choose a **prioritized topological order** that

- Respects the edges in the data-dependence graph (**topological**
- Heuristic choice among options, e.g pick first the node with the longest path extending from that node **prioritized**

Most commonly used method for scheduling. Efficient but yields far less than optimal schedules

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- Many factors to consider when constructing a schedule (everything listed in this presentation and more!)
- Difficult (or more accurately impossible!) to consider all these aspects into a single choice heuristic
- Combinations of heuristics can be used, and multiple iterations performed, but each will usually undo the work of the other

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My Research

- Scheduling of pre-compiled binaries

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- Scheduling of pre-compiled binaries
- Since pre-compiled, my algorithm can afford to be **less efficient** and seek **near-optimal performance**
- Little effort has been made into **consideration of Register Allocation** (i.e preventing spilling) during scheduling

Relaxed Continuous Optimization based Scheduling

Per Instruction i, perform a relaxation of scheduled position to dispatch and completion times t_i,b_i

Objective Variables	t_i, b_i, f_i :	$\mathbb{R}$
Constants	II :	$\mathbb{R}$
Indicator Function	$\mathbb{IN}$:	$\mathbb{R} \longrightarrow \mathbb{R}$
	t_i :	dispatch time
	b_i :	completion time
	f_i :	FIFO use $0 \leq f_i \leq 1$
	II :	iteration interval $\frac{\#instructions}{dispatches/cycle}$

Relaxed Continuous Optimization based Scheduling

Hard Constraints

$$t_i + \epsilon \leq t_j \qquad \forall i, j \cdot i \rightarrow j \tag{1}$$

$$0 \leq t_i \leq b_i \leq \#\text{stages} \cdot \mathrm{II} \tag{2}$$

$$b_i + \epsilon \leq t_i + \mathrm{II} \tag{3}$$

Objective Function

$$\min \sum_i (b_i - t_i + f_i) + \text{Penalties} \tag{4}$$

Key Idea: Encode choice heuristics as penalties, adjust preference by between heuristics scaling

Relaxed Continuous Optimization based Scheduling

Other Key Idea: Need to construct penalty to prevent **Spilling**. Need to prevent clobbering of certain types of instructions

Solution: Indicator function to detect penalize clobbering

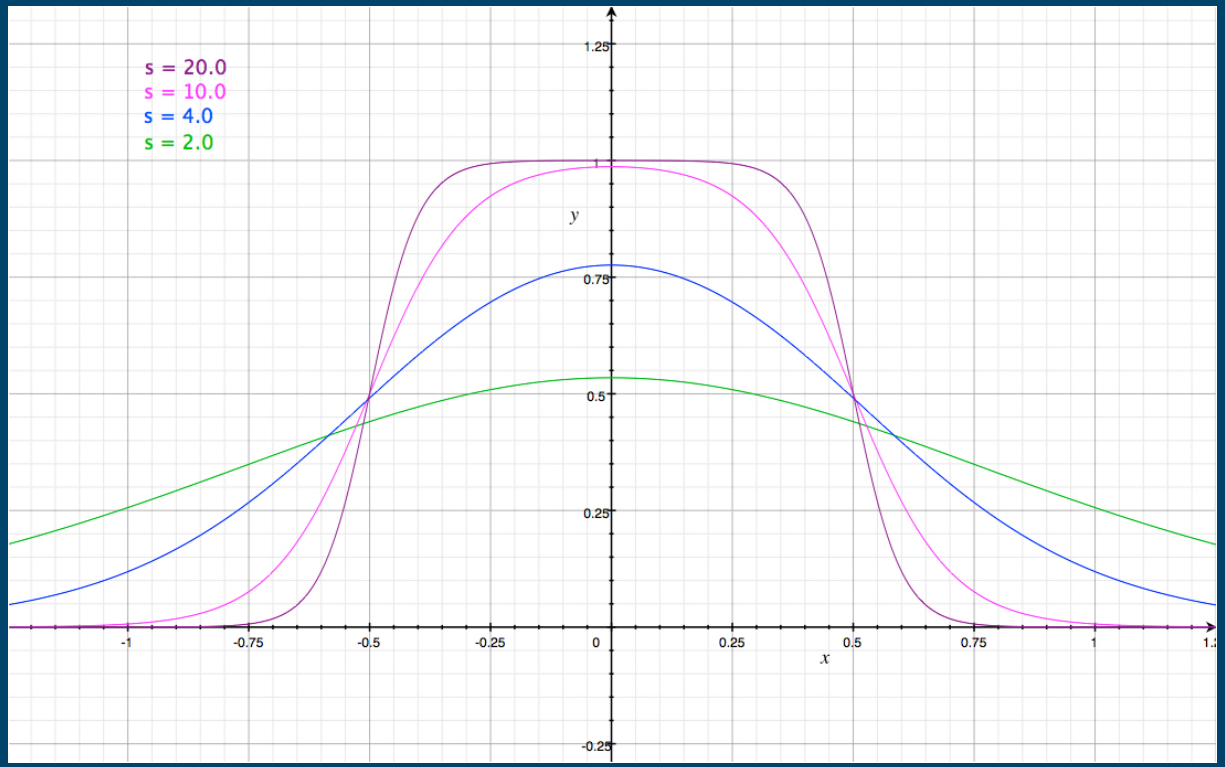

Figure: Altered Sigmoid Indicator Function

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Questions?