Chapter 1

PN Junctions

A **PN junction** is the junction between an N-type semiconductor and P-type semiconductor. Understanding the PN junction will set up us for understanding diodes, BJTs, and MOSFETs later. It seems like we draw it as two separate silicon crystals, but in actual practice the p and n regions are part of the same silicon crystal, accomplished by creating regions of different doping.

Plus ("+") signs represent majority holes while minus ("-") signs represent majority el ectrons. The following diagram is from Seda and Adel's *Microelectronic Circuits*.

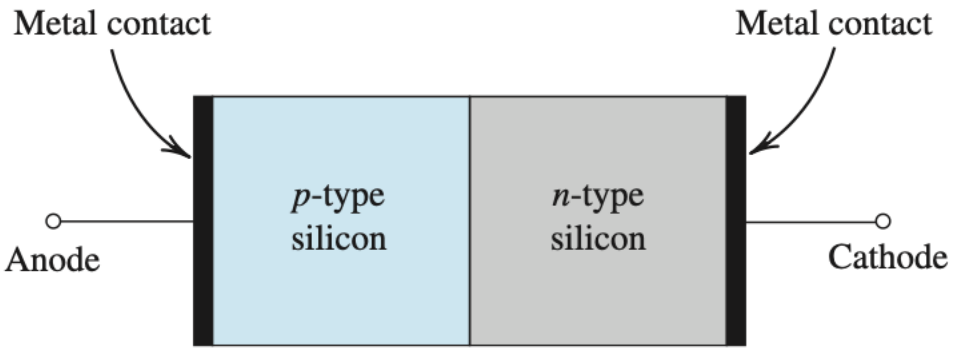


Figure 1.1: Simplified physical structure of the PN junction

1.1 Diffusion Current

Although it doesn't show it in the diagram, there minority holes generated by thermal ionization in the n-type material and there are minority electrons generated in the p-type material. Due to concentration difference of holes in the p region and the n region, holes diffuse across the junction from the p side to the n side. This results in **diffusion current,** I_D, whose direction is from the p to n side.

So current Damanic is wondering right now "if this stuff is diffusing then won't this entire block be the same mush at the end." Here we introduce the depletion region. Holes that diffuse across the junction into the n region recombine with majority electrons there. A charge is said to be **uncovered** when some of the bound positive charge is no longer neutralized by free electrons. This introduces the idea that at a region close to the junction, it is depleted of free electrons and contains unbound positive charge for the n region.

The left side of the PN junction (p region) will be negatively charged while the right side (n region) will be positively

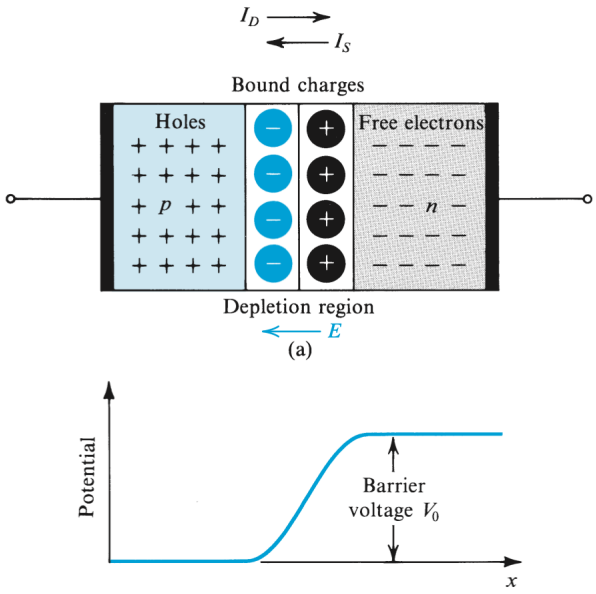


Figure 1.2: Top image shows PN-junction with bound charges and bottom image is potential along an axis perpendicular to the junction

charged. To sum it up, this is because at some point, electrons that diffuse across the junction into the p region will recombine with holes, and those holes will disappear leaving uncovered bound negative charge. Vice versa for holes diffusing into the n region.

From the figure above we see that the n region will be positively charged and the p side if negatively charged. This is the **depletion region**, or the **space-charge region** or **depletion layer**. There are no *mobile* charge carriers present here. Charges on both sides of the depletion region results in an electric field E. Here we introduce the idea that a larger barrier voltage results in a small number of carriers that can overcome this barrier. This leads to a decrease in magnitude of diffusion current since it is more difficult for holes to diffuse into the n region and electrons to diffuse into the p region. Referring again to figure 1.2, we see that V_0 is the barrier voltage. Therefore the diffusion current I_D has a strong relationship with V_0, the voltage drop across the depletion region.

1.2 Drift Current and Equilibrium

Recall that drift current is caused by electric fields and I_S is independent of the value of the depletion-layer voltage V_0. Under open-circuit conditions, there is no external current, so

$$I_D = I_S$$

This condition is maintained by V_0.

Analysis : I_S and I_D at Equilibrium

- V_O: barrier voltage
- I_S: drift current whose direction is from the n side to the p side of the junction
- I_D: diffusion current whose direction is from the p side to the n side of the junction

1. $I_D > I_S$: more bound charge is uncovered on both sides $\rightarrow$ the depletion layer widens (vertically)$\rightarrow$ V_0 increases $\rightarrow$ I_D decreases until $I_D = I_S$ (equilibrium)
2. $I_D < I_S$: uncovered charge decreases $\rightarrow$ depletion layer narrows (vertically) $\rightarrow$ V_0 decreases $\rightarrow$ I_D increases until $I_D = I_S$ (equilibrium)

Under the zero bias equilibrium condition (no external voltage is applied to the PN junction), does the diffusion and drift current "cancel" out here, meaning that current density is nearly zero. Their individual components are also equal here, i.e. hole/electron drift current is equal to hole/electron diffusion current, respectively.

$$J_n = 0 = qn_0\mu_n E_0 + qD_n \frac{dn_0}{dx}$$

V_0 has been referred to so far as barrier voltage boltage, but it's also called **junction built-in voltage**.

$$\phi_{bi} = V_{th} \ln\left(\frac{N_A N_D}{n_i^2}\right) = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Remember here that V_th is thermal voltage which is $\approx$ 26 mV at room temperature. ϕ_{bi} is typically 0.6 V to 0.9V for room temperature silicon. In the EE105 reader, ϕ_{bi} and V_{th} has the same meaning as V_0 and V_T, respectively, in the *Microelectronic Circuits* textbook. I'm writing down the EE105 reader notation here for clarity.

1. How we got from each graph

This graph shows a junction where $N_A > N_D$. If we heavily dope one side, the depletion region will exist almost entirely on the lightly doped side.

Here in figure 1.4, the electric fields in the depletion region are negative because positive charges are on the right and the negative charges are on the left, assuming zero fields in neutral P-region and N-regions. Key takeaways due to difference in doping levels in the N-type and P-type sides:

- Width of the depletion region is not symmetric
- Slope of the electric field is larger in one region than the other
- The negative peak of the electric field always occurs at the junction

Analysis : Gauss's Law

Gauss's Law states that the total electric flux out of a closed surface is equal to the charge enclosed by the permittivity. Electric flux is the electric field multiplied by the area of the surface projected in a plane and perpendicular to the field.

$$\oint_S \vec{E_n} \cdot \vec{ds} = \frac{1}{\varepsilon_0} Q_{inside}$$

1. finish this

By Gauss's Law, the total fixed charged in the N-region is the same as the total fixed charge in the P-region.

$$qN_A x_{p0} = qN_D x_{n0}$$

Here we'll derive the equations for depletion width, which are dependent on externally applied voltage, which are given by the following. The zero is for the zero bias case.

Depletion width on N-side: $x_{n_0} = \sqrt{\frac{2\epsilon_s \phi_{bi}}{qN_D}\left(\frac{N_A}{N_A+N_D}\right)}$

Depletion width on P-side: $x_{p_0} = \sqrt{\frac{2\epsilon_s \phi_{bi}}{qN_A}\left(\frac{N_D}{N_A+N_D}\right)}$

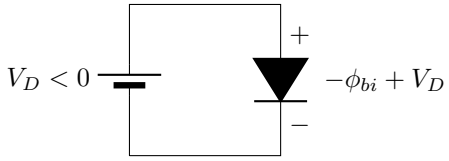
Built in potential: $\phi_{bi} \equiv \phi_n = \phi_p > 0$

Total depletion width $X_{dep_0} = x_{n_0} + x_{p_0} = \sqrt{\frac{2\epsilon_s \phi_{bi}}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)}$

1. derivation here

For the zero bias case (under thermal equilibrium), net current is zero. Diffusion current is very small since few carriers have enough energy to penetrate the barrier. Drift current is small since minority carriers are few.

1.3 Reverse Bias



The above section was discussing the PN junction at equilibrium. At equilibrium, the PN-junction doesn't draw any current. Under reverse bias like in figure above, meaning that a negative voltage is applied, charge will increase and the depletion region widens horizontally. We can rewrite the depletion width formulas from above as a function of V_D.

$$x_n(V_D) = \sqrt{\frac{2\epsilon_s(\phi_{bi}-V_D)}{qN_D}\left(\frac{N_A}{N_A+N_D}\right)} = x_{n_0}\sqrt{1-\frac{V_D}{\phi_{bi}}}$$

$$x_p(V_D) = \sqrt{\frac{2\epsilon_s(\phi_{bi}-V_D)}{qN_A}\left(\frac{N_D}{N_A+N_D}\right)} = x_{p_0}\sqrt{1-\frac{V_D}{\phi_{bi}}}$$

$$X_{dep_0} = x_n(V_D) + x_n(V_D) = \sqrt{\frac{2\epsilon_s(\phi_{bi}-V_D)}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)} = X_{dep_0}\sqrt{1-\frac{V_D}{\phi_{bi}}}$$

Keep these in mind:

- Minority drift current is independent of the barrier height (ϕ_{bi})
- Diffusion current is a strong exponential function of the barrier height

1.4 Forward Bias

This occurs when V_D is nonnegative. A forward bias results in a exponential increase in the number of carriers, which have enough energy to break the barrier. This results in an exponential increase in diffusion current. Drift current doesn't change with forward bias.

1. skipped small signal model for this
2. skipped a lot of practice problems for this too

1.5 Practice Problems

1. Show that
$$V_0 = \frac{1}{2}(\frac{q}{\epsilon_s})(\frac{N_A N_D}{N_A + N_D})W^2$$

2. Show that for a PN junction in which the p side is much more heavily dped than the n side (i.e. $N_A \gg N_D$) referred to as a p^+n diode. The following can be written as follows:
$$W \simeq \sqrt{\frac{2\epsilon_s}{qN_D}V_0}, \quad x_n \simeq W, \quad x_p \simeq \frac{W}{N_A/N_D}$$
$$Q_j \simeq AqN_DW, \quad Q_j \simeq A\sqrt{2\epsilon_s qN_D V_0}$$

3. For a Si PN junction that looks like this, where $N_A = 1 \times 10^{18}$ cm^{-3}and $N_D = 1 \times 10^{17}$ cm^{-3}. Given the built-in potential is 0. V and the relatively permittivity of Si is 12. No voltage is applied.
   (a) Draw the charge along the horizontal axis.
   (b) Draw the electric field along the horizontal axis. Label the critical points such as charge density, depletion width, and maximum electric field in your graphs.

4. Considering a PN junction where the n side is doped with $N_D = 10^{17}$ cm^{-3}and p side is doped with $N_A = 10^{20}$ cm^{-3}, $n_i = 10^{10}$ cm^{-3}, kT/q = 26 mV, μn = 100 cm^2/V $\cdot$ sat p side, μp = 400 cm^2/V $\cdot$ sat n side, L$_n$ = 2.3 μmat p side, and L$_p$ = 3.2 μmat n side, vacumn permittivity is $\epsilon_0 = 8.854 \times 10^{-12}$ C^2/ (N $\cdot$ m^2), the permittivity of silicon is $11.7\epsilon_0$. Area of the PN junction is 1 μm^2
   (a) Calculate the built-in potential.
   (b) Calculate the total depletion width at zero bias.
   (c) Draw the electric field profile at zero bias (You need to calculate the maximum electric field). The left-hand side is N and the right-hand side is P.
   (d) Calculate the depletion capacitance when the bias -1V.
   (e) Calculate the current when the bias is 1V.
   (f) Find out the small-signal resistance and diffusion capacitance at 1V Given $\tau = 1\mu$s.

1.6 Sources

- Sedra, Adel S., et al. Microelectronic Circuits. Oxford University Press, 2021: Specifically screenshots of the graphs I need to redo this when I learn how to use graphing/tikzpicture better in LaTex
- EE105 Reader
- Q1 and Q2 are excercises from Sedra, Adel chapter3
- Q3 from here is Q4 from EE105 HW6
- Q4 from here is Q1 from EE105 Hw7
- Explanation of Gauss's Law

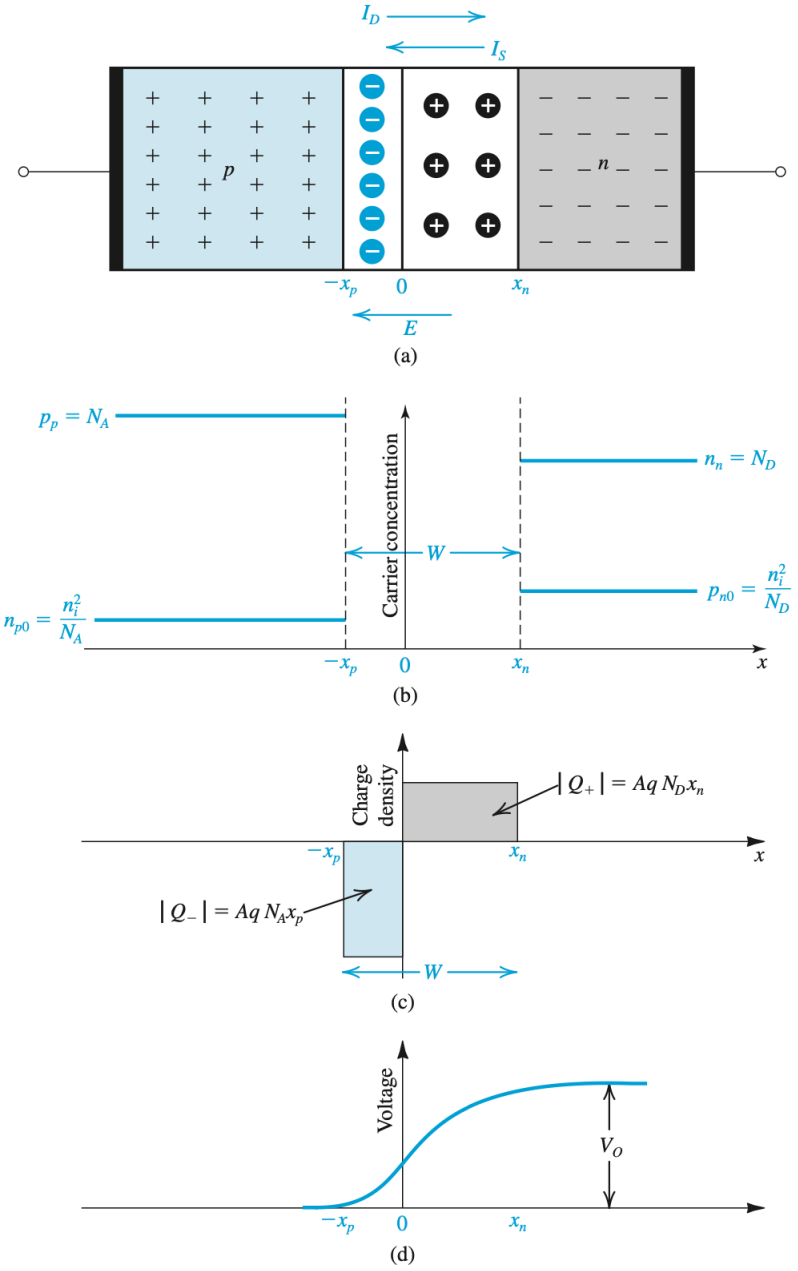


Figure 1.3: Graphs of (a) a PN junction (b) carrier concentrations (c) charge density (d) built in voltage V_0

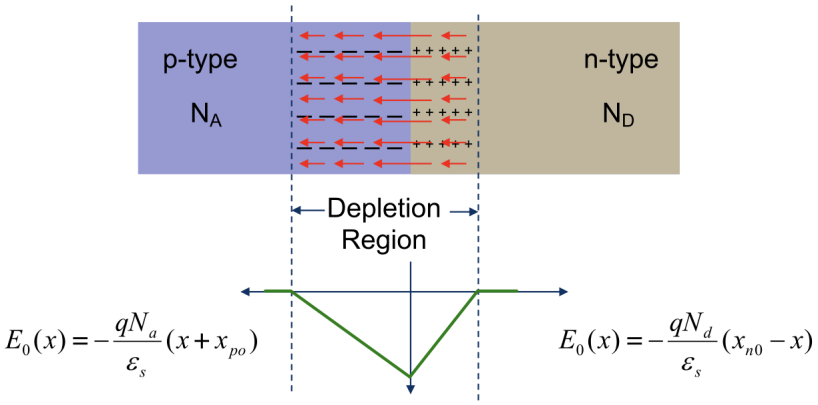


Figure 1.4: Graph of electric field of PN junction