Contents

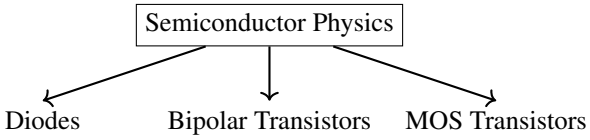
1. use this article to add to ch1 about doping
2. practice problems for ch1
3. practice problems for ch2
4. practice problems for ch3
5. finish up ch3 i burned out while trying to be thorough. p117 in reader, p152 in sedra
6. dead week planning
   (a) tuesday: finish pn junction, diodes, mosfets
   (b) Wedesnday: moscap, amplifiers maybe small signal model
7. todo for saturday
   (a) finish up mosfet and then move onto amplifiers and type up all the homework questions
   (b) make note sheet

Chapter 1

Charge Carriers and Doping

1.1 Introduction

We start learning about resistors, capacitors, and inductors from earlier courses such as EECS 16A and 16B. With more components like transistors, diodes, and op-amps (which are all based on semiconductors), we are able to expand upon circuit design. We need to understand semiconductor physics in order to understand how these components operate.



We can also redefine Ohm's Law which we know as ($V = IR$) as $J = \sigma \mathbf{E}$. We can also write resistance(R) and conductance(G) in terms of other variables

- J: current density, A/m^2 (Amperes per meter squared)
- σ: conductivity, S/m (Siemens per meter)
- $\mathbf{E}$: electric field, V/m (Volts per meter)

$R = \frac{R}{l} = \rho \frac{l}{A}$ and $G = R^{-1} = \sigma \frac{A}{l}$

- σ: conductivity
- ρ: resistivity

For collisions in gas, we focus on the idea that initial velocity and direction is lost/randomized after a few collisions. So, when we sum over the random velocities of the particles and average it, it comes out to zero. Average momentum gain is:

$$\bar{\mu} = \frac{\mathbf{E} q \tau}{M} = \mu \mathbf{E}, \quad \mu := \frac{q\tau}{M} = \frac{\bar{v}}{\mathbf{E}}$$

- μ: mobility, $m^2/(V \cdot s)$
- q: electric charge, 1.60×10^{-19}, Coulombs = Amperes/second
- τ: mean free time
- M: mass
- $\bar{v}$: average velocity

Different elements have a different number of outer shell electrons. For semiconductors like silicon, we can increase the temperature to increase its conductivity. Silicon atoms are arranged in a diamond structure and in general, the energy levels that an atom can occupy are discrete. The **valence band** electrons are at a lower energy state (bound to host atoms) while **conduction band** electrons are at a higher energy state and are "free" electrons. These electrons are free to move around the crystal and take part in conduction.

1.2 Conduction and Fermi Dirac Distribution

Thermal energy is on average about $\sim$ 26 eV at room temperature How large the **band-gap**, the gap between the conduction and valence band, determines how conductive a material is:

- Insulators: band gap $\sim$ 15 eV
  - Glass, rubber, oil, plastic, diamond
- Semiconductors: band gap $\sim 1eV$
  - Silicon = 1.12 eV
- Conductors: Not applicable due to overlapping conduction/valence bands

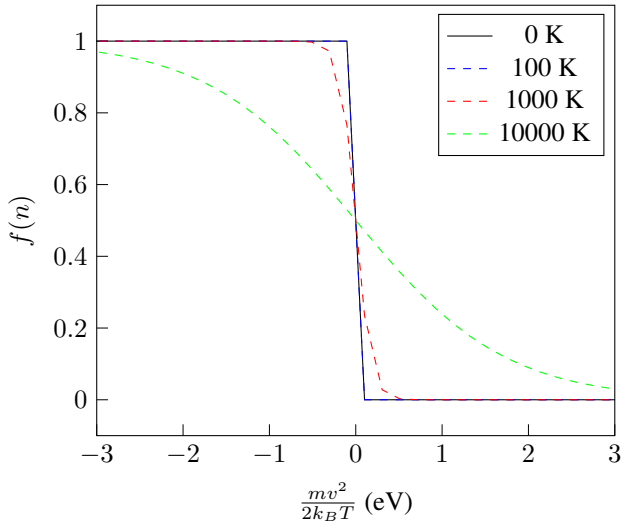
This band gap energy is the minumum energy required to break a covalent bond and generate an electron-hole pair.

Because electrons are a type of particle called a **fermion**, we can say that

$$f(E) = \frac{1}{e^{\frac{E-E_F}{k_B T}} + 1}$$

- $f(E)$: occupational probability of a state energy ϵ
- E: energy of the particle
- E_F: fermi energy, eV
- k_B: Boltzmann's constant, 1.380649×10^{-23} J/K (Joules per Kelvin), 8.62×10^{-5} eV/K
- T: temperature in Kelvin

The graph below is a plot of the Fermi-Dirac Distribution at different temperatures. We can use this plot to find the probability of the concentration of electrons ad holes at certain temperatures.



Ok so why is this graph significant. To repeat, we can relate the concentration of holes or electrons to the temperature of its surroundings. We see that for the plot for a high temperature, there is a greater probability of charge carriers having enough energy to cross into the conduction band.

Thermal generation occurs when sufficient thermal energy exist to break some covalent bonds, which results in a **free electron**. This free electron is now free to conduct electric current if an electric field is applied to the crystal. However, this leaves behind a net positive charge. **Holes** are positively charged carrers, which can also move around the crystal and are available to conduct electric current. As temperature increases, so do electron-hole pairs and the conductivity of the crystal.

Recombination is the process of free electrons and holes moving through the silicon crystal structure and electrons filling in some of the holes. The recombination rate is proportional to the number of free electrons and holes, which also determines the **thermal generation** rate.

At thermal equilibrium, $n = p = n_i$. We can alternatively express as

$$pn = n_i^2$$

- n: concentration of free electrons, cm^{-3}
- p: concentration of holes, cm^{-3}
- n_i: number of free electrons nd holes in a unit volume (cm^3) of intrinsic silicon at a given temperature

We can also write n_i as a function of temperature

$$n_i = BT^{3/2}e^{-E_G/2kT}$$

- B: material-dependent parameter, $7.3 \times 10^{15}\text{cm}^{-3}\text{K}^{-3/2}$ for Silicon
- T: temperature in K
- E_G: bandgap energy, 1.12 eV for silicon
- k, Boltzmann's constant

1.3 Doping

In a non-doped crystal like in the above texts, there will be equal concentrations of free electrons and holes from thermal generation. **Doping** is defined as introducing impurities inside a silicon crystal to adjust the carrier concentration. The following materials are commonly used:

- Group III elements: boron, aluminum, gallium $\rightarrow$ acceptors; increase holes
- Group IV elements: germanium and silicon
- Group V elements: phosphorus, arsenic, antimony $\rightarrow$ donors; increase free electrons

Doping with donors $\rightarrow$ **n type**.

Doping with acceptors $\rightarrow$ **p type**

Sometimes we assume that the number of electrons we add is much greater than the original free electrons that pure silicon had (10^{10} per cubic centimeter). This leads to the simplification that the number of free electrons in our silicon crystal is N_D, where N_D is the number of donor atoms that we add per cubic centimeter.

Analysis : Doping concentrations

Suppose we dope silicon with phosphorus, an acceptor. This means that four electrons from its outer shell will form a covalent bond with silicon. This results in one free electron, meaning that each phosphorus atom donates one free electron to the silicon. No holes are generated during this process. Usually, the concentration of donor atoms, N_D, is much greater htan n_i, so

$$n_n \simeq N_D$$

- n_n: for n-type silicon, concentration of free electrons
- p_n: for n-type silicon, concentratation of holes
- N_D: donor doping concentration
- N_A: acceptor doping concentration

n_n is determined by doping concentration, and independent of temperature, while p_n is determined by:

$$p_n n_n = n_i^2$$
$$p_n \simeq \frac{n_i^2}{N_D}$$

An analysis with boron, an acceptor, will yield similar conclusions with a change in variables.
If the concentration of donors/acceptors is greater than the other by a factor of at least 100, then we can say that $n/p = N_D/N_A$, respectively.

1.4 Compensated Semiconductor Material

We can dope a semiconductor with both acceptors and donors. A **compensated semiconductor material** has both acceptors and donors.

N-type material: $N_D > N_A$

$$n \approx N_D - N_A, \quad p \approx \frac{n_i^2}{N_D - N_A}$$

P-type material: $N_D < N_A$

$$p \approx N_A - N_D, \quad n \approx \frac{n_i^2}{N_A - N_D}$$

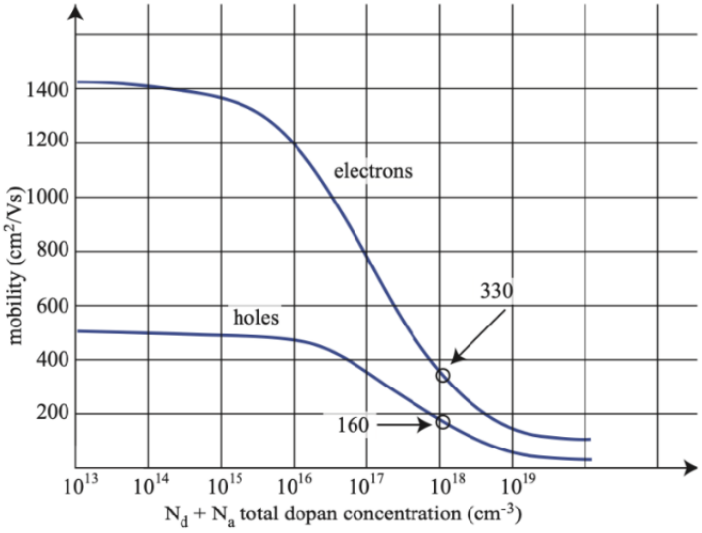
1.5 Practice Problems

1. Calculate the intrinsic carrier density n_i for silicon at $T = 50$ K and 350 K.

$$\begin{aligned} n_{i,1} &= BT^{3/2}e^{-E_G/2kT} \\ &= (7.3 \times 10^{15}\text{cm}^{-3}\text{K}^{-3/2})(50K)^{3/2}e^{-1.12eV/2(8.62\times10^{-5}eV/K)(50K)} \\ &= 9.63217875 \times 10^{-39}/\text{cm}^3 \\ n_{i,2} &= (7.3 \times 10^{15}\text{cm}^{-3}\text{K}^{-3/2})(350K)^{3/2}e^{-1.12eV/2(8.62\times10^{-5}eV/K)(350K)} \\ &= 4.15216354 \times 10^{11}/\text{cm}^3 \end{aligned}$$

2. Consider an n-type silicon for which the dopant concentration $N_D = 10^{17}$ cm^{-3}. Find the electron and hole concentrations at 350 K. Refer to previous example for the value of n_i at $T = 350$ K.
Since this is an n-type silicon,
$$n_n \simeq N_D = 10^{17}/\text{cm}^3$$
From this we can find the concentration of minority holes as
$$p_n \simeq \frac{n_i^2}{N_D} = \frac{(4.15 \times 10^{11})^2}{10^17} = 1.72 \times 10^6/\text{cm}^3$$

3. Here is a 1 μm long Si bar doped with 6×10^{15} cm^{-3}of As and 6×10^{15} cm^{-3}at 300 K. Assume $n_i =$ cm^{-3}. Answer the following questions (show the unit). Assume complete ionization. Use the given figure to find the mobility.



(a) Find the concentration of n and p.
Arsenic is a donor, meaning that it has 5 valence electrons in its outermost shell. $n \approx 6\times10^{15} - 4\times10^{15} = 2 \times 10^{15}$
$p = \frac{n_i^2}{n} = 5 \times 10^4\text{cm}^{-3}$

(b) Calculate its resistivity.
$$\rho = \frac{1}{q(\mu_n n + \mu_p p)}$$
Looking at the graph we see that at $N_A + N_D = 10^{16}$. $\mu_n \approx 1200$ cm^2/V $\cdot$ sand $\mu_p \approx$ cm^2/V $\cdot$ s. We can also simplify our equation above as
$$\rho \approx \frac{1}{q\mu_n n} = 2.6\ \Omega\ \text{cm}$$

(c) Find the current density when 1 V is applied across the 1 μm length direction.
$$J = \sigma E = \frac{E}{\rho} = \frac{1}{2.6 \times 10{-}4cm} \approx 3840\ \text{A/cm}^2$$

(d) If we keep increasing the voltage, will the current keep increasing?
No, due to velocity saturation.

1.6 Sources

- Razavi Electronics 1, Lec 1, Intro., Charge Carriers, Doping
- EE105 Reader
- Sedra, Adel S., et al. Microelectronic Circuits. Oxford University Press, 2021
- Engineering LibreTexts: The Fermi-Dirac Distribution
- Fermi-dirac distribution graph
- Q3 appeared as Q1 as EE105 HW6

Chapter 2

Drift and Diffusion Current

Total current flow is made up of drift current and diffusion current. If we apply an electric field E to a semiconductor crystal, then holes accelerate in the direction of E and free electrons accelerate in the opposite direction of E. While **drift current** is movement caused by electric fields, **diffusion current** is movement caused by variation in the carrier concentration.

2.1 Drift Current

$$v_{p-drift} = \mu_p E, \quad v_{n-drift} = -\mu_n E$$

- E: electric field, V/cm
- $v_{p-drift}$: drift velocity of holes, cm/s
- $v_{n-drift}$: drift velocity of electrons, cm/s
- μ_p: hole mobility, cm^2/V $\cdot$ s, 480 cm^2/V $\cdot$ s for intrinsic silicon
- μ_n: electron mobility, cm^2/V $\cdot$ s, 1350 cm^2/V $\cdot$ s for intrinsic silicon

Current density is the current per unit cross-sectional area

$$J_p = qn\mu_p E, \quad J_n = qn\mu_n E$$

Total drift current density is

$$J = J_p + J_n = q(p\mu_p + n\mu_n)E = \sigma E$$

Via pattern matching, we can see that conductivity σ is given by $\sigma = q(p\mu_p + n\mu_n)$ and resistivity is the inverse of this.

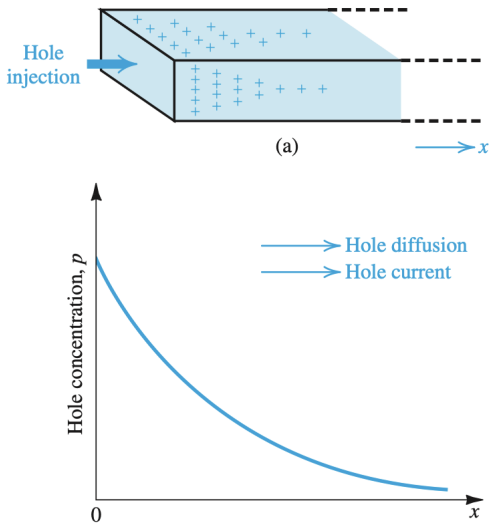
2.2 Diffusion Current

Diffusion current is the diffusion of charge carriers that give rose to a net flow of charge fro a region of high concentration to a region of low concentration. This implies that we can have current without voltage. We can write the current density as a function of the **concentration gradient** (slope of the concentration profile) at any point such that:

$$J_p = -qD_p \frac{dp(x)}{dx}, \quad J_n = qD_n \frac{dn(X)}{dx}$$

- J_p, J_n: hole/electron-current density, A/cm^2
- q: magnitude of the electron charge
- D_p, D_n: diffusion constant or diffusivity of holes/electrons. For intrinsic silicon, $D_p = 12$ cm^2/s and $D_n = 35$ cm^2/s
- $p(x), n(x)$: hole/electron concentration at point x. Note that if $\frac{dp(x)}{dx} < 0$, J_p ends up being positive.

This equation shows that current density is proportional to the slope of the concentration. The image below shows a bar of silicon and an injection of holes on the left side, which will result in hole diffusion current in the same direct (positive direction of x)



Suppose we fill a gas chamber that is divided into two sections with a gases of temperature T on one side. If we remove this divider, the gas will fill the entire volume of the new chamber. This occurs due to the concentration gradient. If the gas molecules here were charged, there would be a net current flow.

Analysis : Einstein Relationship

The following equation is known as the **Einstein relationship**:

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = V_T = \frac{kT}{q}$$

- V_T: thermal voltage; at $T \simeq 300$ K, $V_T = 25.9$ mV

We see that the diffusion constant is related to the mobility.

Total current will be given by the sum of drift and diffusion currents. In resistors, since the carrier is approximately uniform, diffusion current is nearly zero.

$$J^n = J^n_{drift} + J^n_{diff} = q\mu_n nE + qD_n \frac{dn}{dx}$$

2.3 Practice Problems

1. A uniform bar of n-type silicon of 2-μm length has a voltage of 1 V applied across it. If $N_D = 10^{16}$ cm^{-3}and $\mu_n = 1350$ cm^2/V $\cdot$ s, find (a) the electron drift velocity, (b) the time it takes an electron to cross the 2-μm

length, (c) the drift-current density, and the (d) drift current in the case that the silicon bar has a cross-sectional area of 0.25 μm^2.

(a) TODO: finish out this question

2. A general relationship for the current density carried out by holes of density p is $J = qpv$, where q is the electronic charge and v is the hole velocity.

   (a) Find the velocity of holes, $v(x)$, that are moving only by diffusion if they have a density distribution of $p(x) = p_0 e^{-x/l}$. The electric field is zero.

   (b) What would be the electric field that would lead to a hole drift velocity equal to that of the diffusion velocity in part(a)? Use Einstein's relation to answer this question.

   (c) At 300 K, what is the value of l to make the ecltric field in part (b) be 1000 V/cm?

2.4 Sources

- Sedra, Adel S., et al. Microelectronic Circuits. Oxford University Press, 2021
- EE105 Reader
- Q2 fro here is Q2 from EE105 HW6

Chapter 3

PN Junctions

A **PN junction** is the junction between an N-type semiconductor and P-type semiconductor. Understanding the PN junction will set up us for understanding diodes, BJTs, and MOSFETs later. It seems like we draw it as two separate silicon crystals, but in actual practice the p and n regions are part of the same silicon crystal, accomplished by creating regions of different doping.

Plus ("+") signs represent majority holes while minus ("-") signs represent majority el ectrons. The following diagram is from Seda and Adel's *Microelectronic Circuits*.

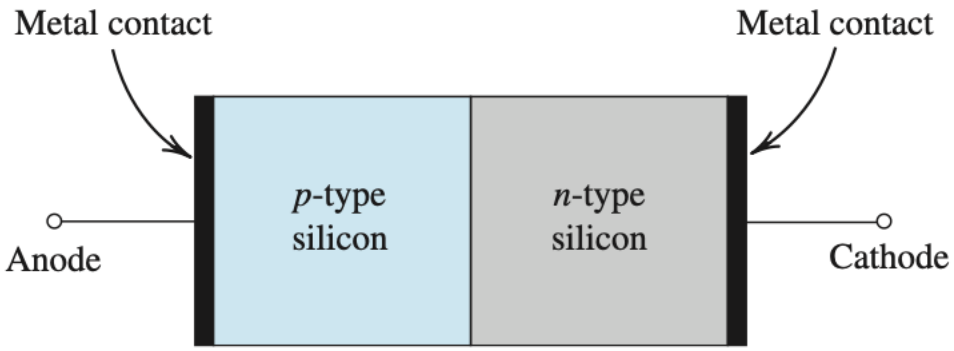


Figure 3.1: Simplified physical structure of the PN junction

3.1 Diffusion Current

Although it doesn't show it in the diagram, there minority holes generated by thermal ionization in the n-type material and there are minority electrons generated in the p-type material. Due to concentration difference of holes in the p region and the n region, holes diffuse across the junction from the p side to the n side. This results in **diffusion current,** I_D, whose direction is from the p to n side.

So current Damanic is wondering right now "if this stuff is diffusing then won't this entire block be the same mush at the end." Here we introduce the depletion region. Holes that diffuse across the junction into the n region recombine with majority electrons there. A charge is said to be **uncovered** when some of the bound positive charge is no longer neutralized by free electrons. This introduces the idea that at a region close to the junction, it is depleted of free electrons and contains unbound positive charge for the n region.

The left side of the PN junction (p region) will be negatively charged while the right side (n region) will be positively

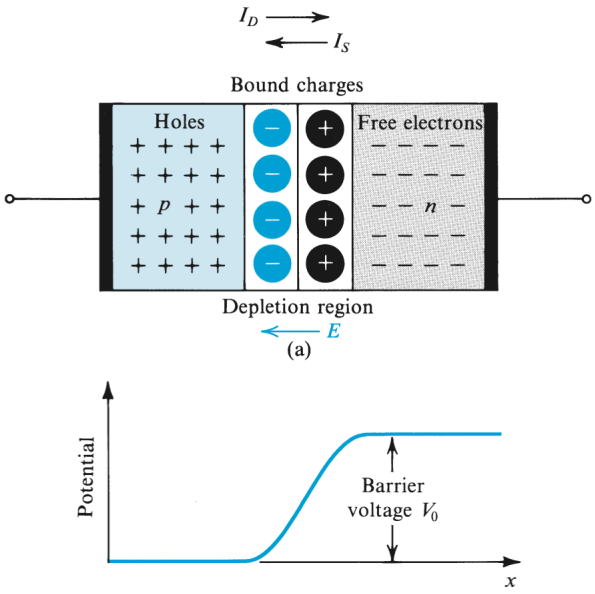


Figure 3.2: Top image shows PN-junction with bound charges and bottom image is potential along an axis perpendicular to the junction

charged. To sum it up, this is because at some point, electrons that diffuse across the junction into the p region will recombine with holes, and those holes will disappear leaving uncovered bound negative charge. Vice versa for holes diffusing into the n region.

From the figure above we see that the n region will be positively charged and the p side if negatively charged. This is the **depletion region**, or the **space-charge region** or **depletion layer**. There are no *mobile* charge carriers present here. Charges on both sides of the depletion region results in an electric field E. Here we introduce the idea that a larger barrier voltage results in a small number of carriers that can overcome this barrier. This leads to a decrease in magnitude of diffusion current since it is more difficult for holes to diffuse into the n region and electrons to diffuse into the p region. Referring again to figure 3.2, we see that V_0 is the barrier voltage. Therefore the diffusion current I_D has a strong relationship with V_0, the voltage drop across the depletion region.

3.2 Drift Current and Equilibrium

Recall that drift current is caused by electric fields and I_S is independent of the value of the depletion-layer voltage V_0. Under open-circuit conditions, there is no external current, so

$$I_D = I_S$$

This condition is maintained by V_0.

Analysis : I_S and I_D at Equilibrium

- V_O: barrier voltage
- I_S: drift current whose direction is from the n side to the p side of the junction
- I_D: diffusion current whose direction is from the p side to the n side of the junction

1. $I_D > I_S$: more bound charge is uncovered on both sides → the depletion layer widens (vertically)→ V_0 increases → I_D decreases until $I_D = I_S$ (equilibrium)
2. $I_D < I_S$: uncovered charge decreases → depletion layer narrows (vertically) → V_0 decreases → I_D increases until $I_D = I_S$ (equilibrium)

Under the zero bias equilibrium condition (no external voltage is applied to the PN junction), does the diffusion and drift current "cancel" out here, meaning that current density is nearly zero. Their individual components are also equal here, i.e. hole/electron drift current is equal to hole/electron diffusion current, respectively.

$$J_n = 0 = qn_0\mu_n E_0 + qD_n\frac{dn_0}{dx}$$

V_0 has been referred to so far as barrier voltage boltage, but it's also called **junction built-in voltage**.

$$\phi_{bi} = V_{th}\ln\left(\frac{N_A N_D}{n_i^2}\right) = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Remember here that V_th is thermal voltage which is $\approx$ 26 mV at room temperature. ϕ_{bi} is typically 0.6 V to 0.9V for room temperature silicon. In the EE105 reader, ϕ_{bi} and V_{th} has the same meaning as V_0 and V_T, respectively, in the *Microelectronic Circuits* textbook. I'm writing down the EE105 reader notation here for clarity.

1. How we got from each graph

This graph shows a junction where $N_A > N_D$. If we heavily dope one side, the depletion region will exist almost entirely on the lightly doped side.

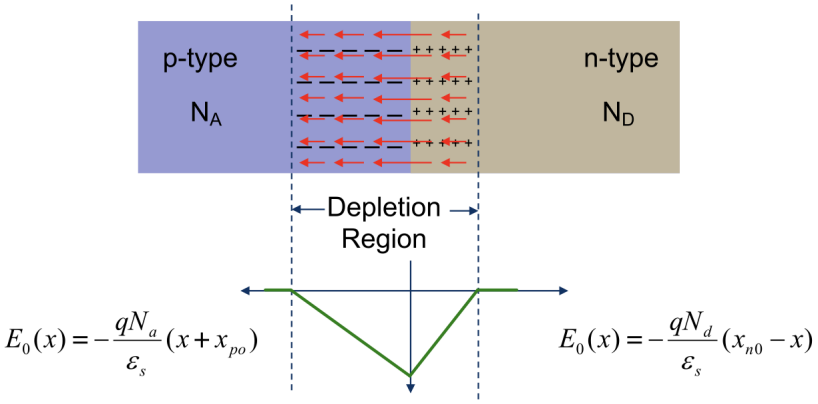


Figure 3.4: Graph of electric field of PN junction

Here in figure 3.4, the electric fields in the depletion region are negative because positive charges are on the right and the negative charges are on the left, assuming zero fields in neutral P-region and N-regions. Key takeaways due to difference in doping levels in the N-type and P-type sides:

- Width of the depletion region is not symmetric
- Slope of the electric field is larger in one region than the other
- The negative peak of the electric field always occurs at the junction

Analysis : Gauss's Law

Gauss's Law states that the total electric flux out of a closed surface is equal to the charge enclosed by the permittivity. Electric flux is the electric field multiplied by the area of the surface projected in a plane and perpendicular to the field.

$$\oint_S \vec{E_n} \cdot \vec{ds} = \frac{1}{\varepsilon_0} Q_{inside}$$

1. finish this

By Gauss's Law, the total fixed charged in the N-region is the same as the total fixed charge in the P-region.

$$qN_A x_{p0} = qN_D x_{n0}$$

Here we'll derive the equations for depletion width, which are dependent on externally applied voltage, which are given by the following. The zero is for the zero bias case.

Depletion width on N-side: $x_{n_0} = \sqrt{\frac{2\epsilon_s \phi_{bi}}{qN_D}\left(\frac{N_A}{N_A+N_D}\right)}$

Depletion width on P-side: $x_{p_0} = \sqrt{\frac{2\epsilon_s \phi_{bi}}{qN_A}\left(\frac{N_D}{N_A+N_D}\right)}$

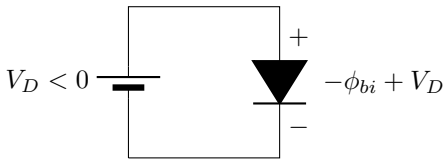
Built in potential: $\phi_{bi} \equiv \phi_n = \phi_p > 0$

Total depletion width $X_{dep_0} = x_{n_0} + x_{p_0} = \sqrt{\frac{2\epsilon_s \phi_{bi}}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)}$

1. derivation here

For the zero bias case (under thermal equilibrium), net current is zero. Diffusion current is very small since few carriers have enough energy to penetrate the barrier. Drift current is small since minority carriers are few.

3.3 Reverse Bias



The above section was discussing the PN junction at equilibrium. At equilibrium, the PN-junction doesn't draw any current. Under reverse bias like in figure above, meaning that a negative voltage is applied, charge will increase and the depletion region widens horizontally. We can rewrite the depletion width formulas from above as a function of V_D.

$$x_n(V_D) = \sqrt{\frac{2\epsilon_s(\phi_{bi}-V_D)}{qN_D}\left(\frac{N_A}{N_A+N_D}\right)} = x_{n_0}\sqrt{1-\frac{V_D}{\phi_{bi}}}$$

$$x_p(V_D) = \sqrt{\frac{2\epsilon_s(\phi_{bi}-V_D)}{qN_A}\left(\frac{N_D}{N_A+N_D}\right)} = x_{p_0}\sqrt{1-\frac{V_D}{\phi_{bi}}}$$

$$X_{dep_0} = x_n(V_D) + x_n(V_D) = \sqrt{\frac{2\epsilon_s(\phi_{bi}-V_D)}{q}(\frac{1}{N_A}+\frac{1}{N_D})} = X_{dep_0}\sqrt{1-\frac{V_D}{\phi_{bi}}}$$

Keep these in mind:

- Minority drift current is independent of the barrier height (ϕ_{bi})
- Diffusion current is a strong exponential function of the barrier height

3.4 Forward Bias

This occurs when V_D is nonnegative. A forward bias results in a exponential increase in the number of carriers, which have enough energy to break the barrier. This results in an exponential increase in diffusion current. Drift current doesn't change with forward bias.

1. skipped small signal model for this
2. skipped a lot of practice problems for this too

3.5 Practice Problems

1. Show that
$$V_0 = \frac{1}{2}(\frac{q}{\epsilon_s})(\frac{N_A N_D}{N_A+N_D})W^2$$
2. Show that for a PN junction in which the p side is much more heavily dped than the n side (i.e. $N_A \gg N_D$) referred to as a p^+n diode. The following can be written as follows:
$$W \simeq \sqrt{\frac{2\epsilon_s}{qN_D}V_0}, \quad x_n \simeq W, \quad x_p \simeq \frac{W}{N_A/N_D}$$
$$Q_j \simeq AqN_DW, \quad Q_j \simeq A\sqrt{2\epsilon_s qN_D V_0}$$
3. For a Si PN junction that looks like this, where $N_A = 1\times10^{18}$ cm^{-3}and $N_D = 1\times10^{17}$ cm^{-3}. Given the built-in potential is 0. V and the relatively permittivity of Si is 12. No voltage is applied.

   (a) Draw the charge along the horizontal axis.
   (b) Draw the electric field along the horizontal axis. Label the critical points such as charge density, depletion width, and maximum electric field in your graphs.

4. Considering a PN junction where the n side is doped with $N_D = 10^{17}$ cm^{-3}and p side is doped with $N_A = 10^{20}$ cm^{-3}, $n_i = 10^{10}$ cm^{-3}, kT/q = 26 mV, μn = 100 cm^2/V $\cdot$ sat p side, μp = 400 cm^2/V $\cdot$ sat n side, L$_n$ = 2.3 μmat p side, and L$_p$ = 3.2 μmat n side, vacumn permittivity is $\epsilon_0 = 8.854\times10^{-12}$ C^2/ (N $\cdot$ m^2), the permittivity of silicon is 11.7ϵ_0. Area of the PN junction is 1 μm^2

   (a) Calculate the built-in potential.
   (b) Calculate the total depletion width at zero bias.
   (c) Draw the electric field profile at zero bias (You need to calculate the maximum electric field). The left-hand side is N and the right-hand side is P.
   (d) Calculate the depletion capacitance when the bias -1V.
   (e) Calculate the current when the bias is 1V.
   (f) Find out the small-signal resistance and diffusion capacitance at 1V Given $\tau = 1\mu$s.

3.6 Sources

- Sedra, Adel S., et al. Microelectronic Circuits. Oxford University Press, 2021: Specifically screenshots of the graphs I need to redo this when I learn how to use graphing/tikzpicture better in LaTex
- EE105 Reader
- Q1 and Q2 are excercises from Sedra, Adel chapter3
- Q3 from here is Q4 from EE105 HW6
- Q4 from here is Q1 from EE105 Hw7
- Explanation of Gauss's Law

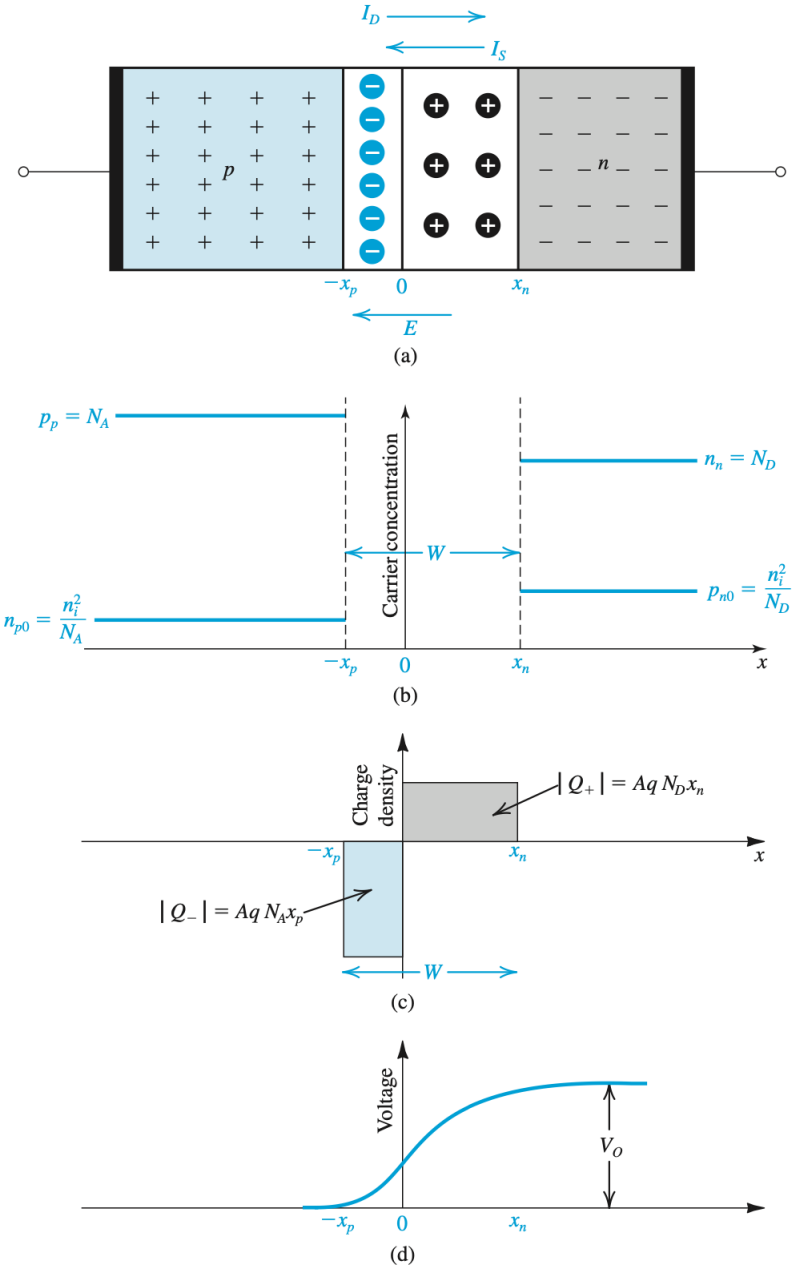


Figure 3.3: Graphs of (a) a PN junction (b) carrier concentrations (c) charge density (d) built in voltage V_0

Chapter 4

MOS Capacitor

The MOS in MOS capacitor stands for Metal-Oxide-Silicon. Sometimes the S is also written as substrate in other places. Understanding threshold voltage here for a MOS-CAP is useful for also understanding MOSFETs in a later chapter.

- Metal: usually this ia heavily doped polysilicon (Poly-Si) layer doped with n^+ or p^+, due to high temperature processing for aluminum
- Oxide: SiO_2 where $\epsilon_{ox} = 3.9\epsilon_0$, can be any insulator actually
- Substrate: $\epsilon_s = 11.7\epsilon_0$; NMOS capacitor $\rightarrow$ P-type substrate, PMOS capacitor $\rightarrow$ N-type substrate

4.1 MOSCAP at Equilibrium

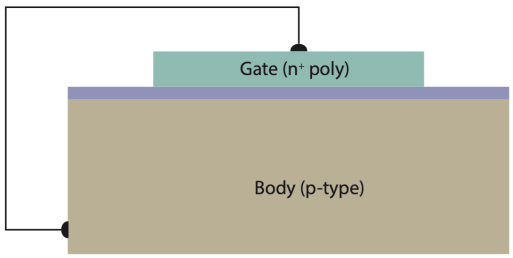


Figure 4.1: MOS CAP with gate and body shorted in equilibrium

In equilibrium , the gate and body, which are the terminals where voltage is applied, are shorted like in fig 4.1. Under thermal equilibrium, there is no current flow, so an N type polysilicon gate will rise to a higher potential than the P type substrate like in a PN junction (previous chapter is relevant here). We also assume that the material used to short the body and the gate is made of the gate material, so it looks more like this.

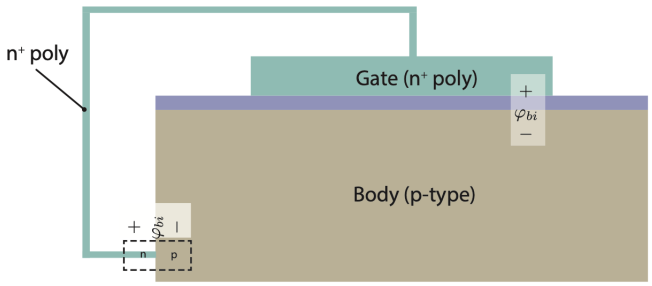


Figure 4.2: There is a ϕ_{bi} from across the PN junction that leads to potential drop across the oxide

Potential of the P type region substrate: $\phi_p = -(\frac{kT}{q}) \ln\left(\frac{N_A}{n_i}\right)$

Potential of the N type gate: $\phi_{poly,n+} = (\frac{kT}{q}) \ln\left(\frac{N_{d,poly}}{n_i}\right)$

Built in potential, NMOS Cap: $\phi_{bi} = \phi_{poly,n+} - \phi_p$

In practice, real wires made of metal like aluminum or copper are used to connect the gate to the body. At the body side, this metal is connected to a heavily doped p^+ region. The **flatband voltage**, V_{FB}, is defined as the gate to body voltage that results in net zero charge and zero fields in the MOSCAP structure. The name comes from the observation that energy bands are flat whe the charge on the gate goes to zero and the depletion region disappears.

$$V_{FB} = -\phi_{bi} = -(\phi_{n^+} - \phi_p)$$

Due to the difference in materials that make up the gate and body, we have an electric field from the gate to the body.

4.2 Regions of Operation

There are three regions of operation: accumulation, depletion, and inversion.

4.2.1 Accumulation

The MOSCAP operates under accumulation when $V_{GB} < V_{FB}$. V_{GB} is the gate to body voltage. This looks like a parallel plate capacitor where there are many electrons and holes to charge up the plates. Negative charges/electrons can flow into the gate and holes will **accumulate** on the surface of the device. This is because negative bias attracts holes to reside under the gate.

4.2.2 Depletion

The MOSCAP operates under depletion when $V_{GB} > V_{FB}$. An artificial depletion region is formed if you apply a voltage to the gate of the MOS CAP. When this happens we are in depletion mode. This is similar to the MOS CAP being in equilibrium.

4.2.3 Inversion

The MOSCAP operates under inversion when $V_{GB} = V_{FB}$.

1. might be a good idea to expand on this

4.3 Practice Problems

1. For a MOSCAP with a p-type substrate. Given $V_{FB} = -0.53$ V, $N_A = 10^{17}$ cm^{-3}, oxide (SiO_2 $\epsilon_{ox} = 4\epsilon_0$) thickness of 3nm, and Silicon $\epsilon_{Si} = 12\epsilon_0$. At 300K and $n_i = 10^{10}$ cm^{-3}. The right-hand side is the semiconductor.

   (a) What is the condition for inversion to happen? Do not just answer $V > V_T$.
   For inversion to happen, the gate-base voltage is greater than the threshold voltage of the MOSCAP $V_{GB} > V_T$. This happens because the depletion region stops growing as the gate voltage is increased due to surface potential increasing. Surface potential will increase until the electron density at the surface equals the background ion density. This then leads to the surface effectively becoming an N-type.

   (b) Qualitatively draw the charge, electric field, and potential at accumulation.

   (c) Qualitatively draw the charge, electric field, and potential at depletion.

   (d) Qualitatively draw the charge, electric field, and potential at inversion.

   (e) Calculate the surface potential at the threshold. Hint: $n = \frac{n_i^2}{N_A} e^{\frac{q\phi_s}{kT}}$
   We see here that surface potential is half of the body potential.

$$\begin{aligned}\phi_S &= 2\phi_B \\ &= 2(\frac{kT}{q}) \ln\left(\frac{N_A}{n_i}\right) \\ &= 2(0.026\text{V}) \ln\left(\frac{10^{17}\text{cm}^{-3}}{10^{10}\text{cm}^{-3}}\right) \\ &= 0.838\text{V}\end{aligned}$$

   (f) Calculate the depletion width and depletion charge density at the threshold. Hint: $W_D = \sqrt{\frac{2\epsilon_{Si}\phi_s}{qN_A}}$

$$W_D$$

   (g) The threshold voltage can be computed by summing up the flat-band voltage, the voltage across the oxide, and the surface potential at the threshold. Please calculate the threshold voltage.

2. For a MOSCAP with a n-type substrate, given $N_D = 10^{17}$ cm^{-3}, oxide (SiO_2 $\epsilon_{ox} = 4\epsilon_0$) thickness of 3nm, and Silicon $\epsilon_{Si} = 12\epsilon_0$. The right hand side is the semiconductor.

   (a)

4.4 Sources

-

Chapter 5

MOSFETs

A transistor comes from the two words **trans**conductance res**istor**. MOSFET stands for MOS field effect transistor since we are taking the MOS CAP and adding two extra diffusion regions. Most of the EE105 reader spents time on the NMOS device since most of the concepts can be carried over into analyzing the PMOS device too. A MOSFET is a three terminal device, so we are moving on form the junction diode, a basic two terminal device

Part of the motivation for learning about MOSFETs is for building a current source and also for voltage amplification. If we are able to form a voltage controlled current source, we can build a voltage amplifier.

5.1 Structure

- n^+: heavily doped n-type silicon
- n^-: lightly doped n-type silicon
- V_t: threshold voltage
- V_T: thermal voltage
- L: channel length

In figure 5.1, we see that the NMOS transistor has the gate, source, drain, and substrate/body terminal, as indicated by the first letters of each terminal. From its physical structure, we notice that a MOSFET is a symmetrical device and that the substrate forms a PN junction with the source and drain regions.

At zero gate voltage, we see that there are two back to back diodes in series between drain and source. One from the PN junction formed between the n^+ drain region and the p type substrate and the other from the n^+ source region and the p type substrate. These diodes prevent current conduction from drain to source when a voltage v_{ds} is applied.

5.2 NMOS: Current conduction

Suppose you ground the source and drain and $v_g > 0$. A positive gate voltage causes free holes to be repelled to the region of the substrate under the gate into the substrate. This leaves a **carrier-depletion region**. A positive gate voltage also attracts electrons from the n^+ source and drain regions to the channel region. Show in figure 5.2

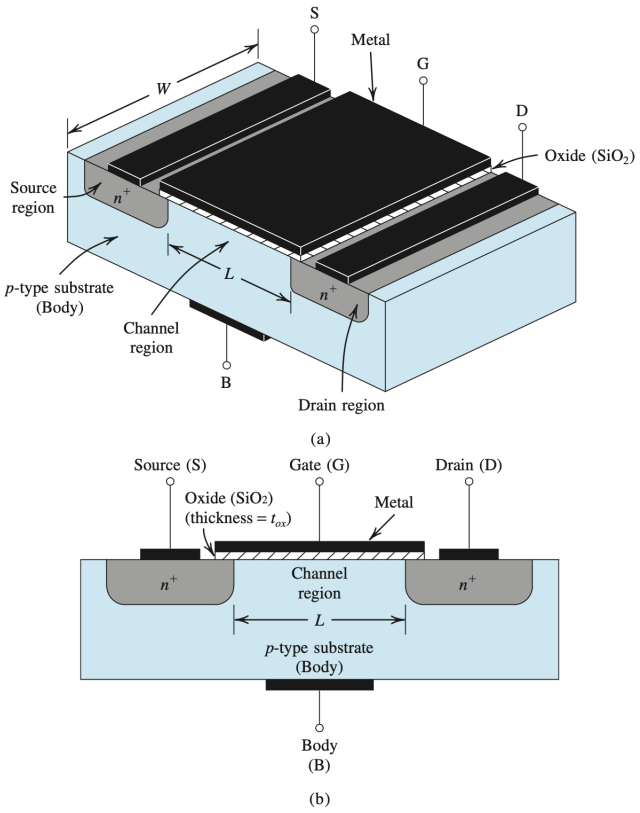


Figure 5.1: Physical structure of the NMOS transistor and a cross section view

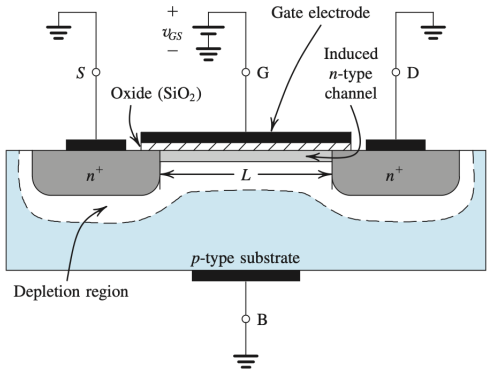


Figure 5.2: Positive voltage applied to the gate. An n channel is induced at the top of the substrate beneath the gate

We see that a **channel** is formed for current flow from the drain to source. **Threshold voltage** is also defined as the value of $v_{GS}$where a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel. **Overdrive voltage**, or **effective voltage** is the excess of v_{GS}over V_t.

$$v_{gs} - V_t \equiv v_{ov}$$

As v_{OV}increases, so does the magnitude of the channel charge. If drawn out, this looks like the an increase in the depth/deepness of the channel.

Another thing to keep in mind here is the **oxide capacitance**.

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

- C_{ox}: capacitance of the parallel-plate capacitor per unit gate area, F/m^2
- ϵ_{ox}: permittivity of silicon dioxide; $\epsilon_{ox} = 3.9\epsilon_0 = 3.45 \times 10^{-11}$ F/m
- t_{ox}: oxide thickness, determined by process technology

Analysis : Deriving i_D for small v_{DS}

We start by applying a small $v_{DS}$and v_{GS}greater than its threshold voltage. i_D is the current that Since i_D is the charge per unit channel length,

$$\frac{\mid Q \mid}{\text{unit channel length}} = C_{ox} W v_{OV}$$

We also know that channel conductance is proportional to the overdrive voltage, or $v_{GS} - V_t$. This means that current in the channel, i_D, is proportional to$(v_{GS} - V_t)$. v_{DS}also establishes an electric field E across the length of the channel given by:

$$\mid E \mid = \frac{v_{DS}}{L}$$

An electric field causes channel electrons to drift towards the drain with a velocity of:

$$\text{Electron drift velocity} = \mu_n \mid E \mid = \mu_n \frac{v_{DS}}{L}$$

Remembering that current is the rate of charged particles, then we find current by multiplying charge per unit channel length by the electron drift velocity.

$$i_D = [(\mu_n C_{ox})(\frac{W}{L})v_{OV}]v_{DS} = [(\mu_n C_{ox})(\frac{W}{L})(v_{GS} - V_t)]v_{DS}$$

Conductance of the channel is given by:

$$g_{DS} = (\mu_n C_{ox})(\frac{W}{L})v_{OV} = (\mu_n C_{ox})(\frac{W}{L})(v_{GS} - V_t)$$

Process transconductance parameter is given by:

$$K'_n = \mu_n C_{ox}$$

For a small v_{DS}, the MOSFET behaves with a linear resistance r_{DS} given by

$$r_{DS} = \frac{1}{g_{DS}} = \frac{1}{(\mu_n C_{ox})(W/L)v_{OV}}$$

If we increase v_{DS}, the depletion region will widen at the depletion region as a result of the increased v_{DS}that makes the channel shallower near the drain. This is reflected in the formula for i_D. We'll see that the channel looks more like a tapered shape, where it's deepest at the source end (proportional to v_{OV}) and shallowest at the drain end (proportional to v_{OV}- v_{DS}). Shown in figure 5.3.

$$i_D = \mu_n C_{ox}(\frac{W}{L})(V_{OV} - \frac{1}{2}v_{DS})v_{DS}$$

Figure 5.4 shows the drain current for different regions. Increasing v_{DS}beyond v_{OV}has no affect on the channel shape and charge. This is when the transistor enters saturation and the channel region resembles a right triangle with the deepest part being close to the source.

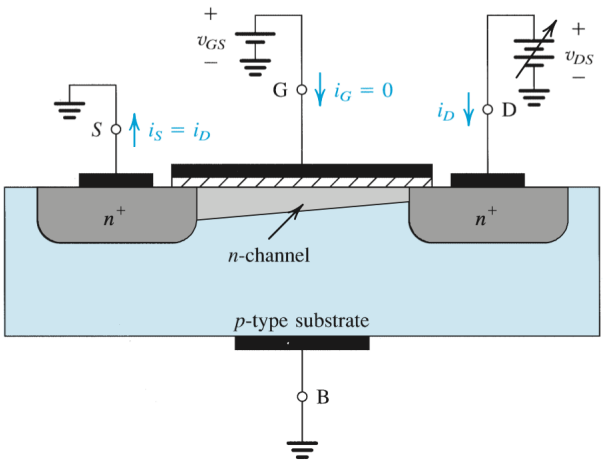


Figure 5.3: Operation of the enhancement NMOS transistor as $v_{DS}$is increased

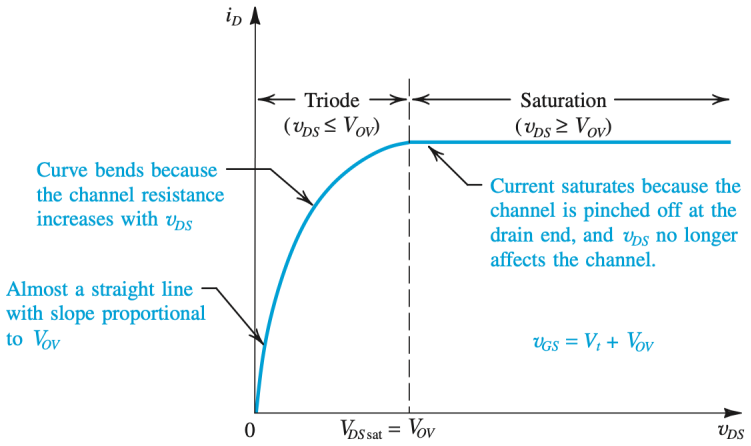


Figure 5.4: Operation of the enhancement NMOS transistor in different regions

5.3 PMOS: Structure and Current conduction

To conduct current here, we need to apply a negative voltage between the gate and the source. This is because the current here is carried by holes (current goes in the same direction as the holes, contrastingly from when current is carried by electrons) and flows from the source to the drain. If we had to compare the NMOS cross section with the PMOS cross section, then we would notice that the substrate type for a PMOS transistor is an n-type substrate with p^+-type wells for the source and drain, while this is switched for a NMOS transistor (p-type substrate with n^+-type wells for source and drain). We'll also notice that the direction of current is flowing from opposite wells.

- $k'_p = \mu_p C_{ox}$: process transconductance parameter for PMOS
- mu_p: mobility of the holes in the induced
- $k_p = k'_p(W/L)$: transistor transconductance parameter

Typically, NMOS transistors have greater gain and speed of operations than PMOS devices. Electron mobility μ_n is higher by factor of 2 to 4 than the hole mobility μ_p. The following attached PDF was something found online but sums up everything pretty nicely in a funny style.

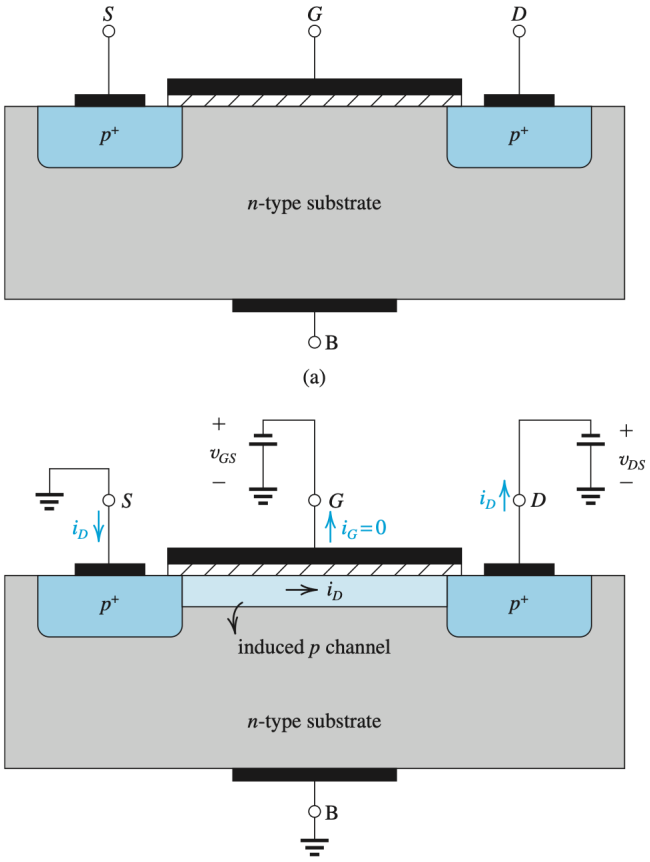


Figure 5.5: Physical structure of the PMOS structure and side view

5.4 Large and Small Signal Equivalent Models

Large signal equivalent model of an n-channel MOSFET operating in the saturation region

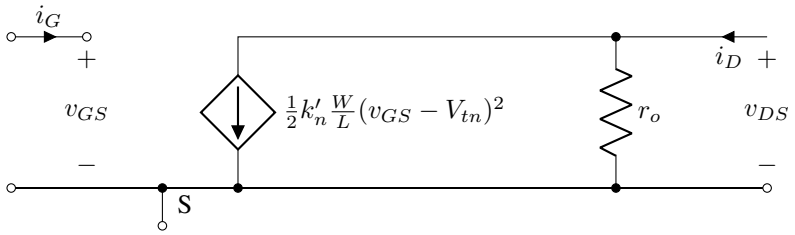


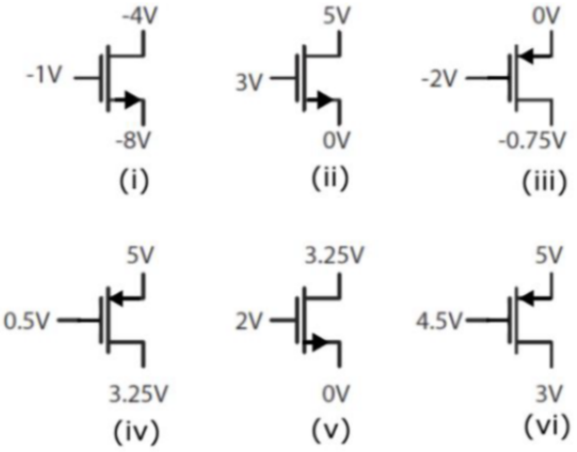
Figure 5.6: Large signal model operating in saturation drawn with outputresistance r_o

Future chapters will talk about the BJT (bipolar junction transistor).

- MOSFETs can be made smaller than BJTs
- MOSFET manufacturing process is relatively simpler and requires comparatively little powers
- MOSFETs generate less heat
- BJT better for current amplification circuits
- BJT low on-state voltage drop and low conduction loss
- BJT preferred in high power applications due to higher power handling; MOSFET preferred for low power applications

5.5 Practice Problems

1. Find the region of operation for the following transistors. You may use $V_{tn} = 0.9$V and $|V_{tp} = 1$V. The operation condition of NMOS is also shown. PMOS is conducted by holes which is opposite to NMOS so the voltage polarity is different.



Region of operation	Condsitions	i_{DS}
Cut-off	v_{GS}< V_T	$i_{DS}\sim$ 0A
Linear/Triode	$V_{GS} > V_T, V_{DS} < V_{GS} - V_T$	i_{DS}= $\frac{W}{L}\mu_n C_{ox}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}$
Saturation:	$V_{GS} > V_T, V_{DS} > V_{GS} - V_T$	i_{DS}= $\frac{W}{L}\frac{\mu_n C_{ox}}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$

(a) We identify this transistor as a NMOS transistor due to the direction of the arrow. In a NMOS transistor, current flows from drain to source due to electrons being the charge carriers in the NMOS transistor. v_{GS}= $v_G - v_S$ = 7V and v_{DS}= $v_D - v_S = -4 - (-8) - 4$V. This transistor is in the linear/triode region.

(b) v_{GS}= 3V and v_{DS}= 5V. This transistor is in the saturation region.

(c) This is a PMOS transistor. In a PMOS transistor, current flows from source to drain. $|v_{GS}| = 2$V and $|v_{DS}| = 0.75$V. This is in the linear/triode region.

(d) $|v_{GS}| = 4.5$V and $|v_{DS}| = |3.25 - 5| = 1.75$V. This is in the linear/triode region.

(e) $v_{GS} = 2$V and $v_{DS} = 3.25 - 0 = 3.25$V. This is in the saturation region.

(f) $|v_{GS}| = |4.5 - 5| = 0.5$V. This is in the cutoff region.

2. An ideal N-channel MOSFET has the following parameters: $W = 100\ \mu$m, $L = 1\ \mu$m, $t_{ox} = 15$ nm, the oxide relative permittivity is 4, the silicon relative permittivity is 12, $N_A = 10^{15}$ cm^{-3}, $n_i = 10^{10}$ cm^{-3}, $V_{FB} = -0.2$ V, $\mu_n = 300$ cm^2/V $\cdot$ sat 300K. $\lambda = 0$.

   (a) Find the threshold voltage.
   Threshold voltage is given by the following formula:

$$\phi_B = \frac{kT}{q}\ln\frac{N_A}{n_i} = 0.026V\ln\left(\frac{10^{15}\text{cm}^{-3}}{10^{10}\text{cm}^{-3}}\right) = 0.2993\ldots V$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{4(8.854\times10^{-14}\text{F/cm})}{15\text{nm}} = 3.54\times10^{-7}\text{F/cm}^2$$

$$V_t = V_{FB} + 2\phi_B + \frac{\sqrt{2q\epsilon_s N_A 2\phi_B}}{C_{ox}}$$

$$= -0.2 + 2(0.299) + \frac{2(12)(8.854\times10^{14}\text{F/cm})(1.602\times10^{-19}C)(10^{15}\text{cm}^{-3})(2)(0.2993V)}{3.54\times10^{-7}\text{F/cm}^2}$$

$$= 0.44\text{V}$$

   (b) What is the minumum v_{DS}value for the MOSFET to be at saturation region at v_{GS}= 2V.
   For the MOSFET to remain in saturation, v_{DS}= v_{GS}- V_tn, so

$$V_{DS} - V_{DS} - V_{tn} = 2 - 0.44 = 1.56\text{V}$$

   (c) Find the channel resistance at v_{GS}= 2V and v_{DS}= 0.01 V.
   Channel resistance is given by calculating what $i_{DS}$is given that we know $v_{DS}$is.

$$R_{ch} = \frac{V_{DS}}{I_{DS}} = \frac{0.01V}{\frac{W}{L}\mu_n C_{ox}(V_{GS}-V_T)V_{DS}}$$

$$= \frac{1}{300\times100\times3.54\times10^{-7}\times1.56}$$

$$= 60.36\Omega$$

   (d) Find I_D at v_{GS}= 2V and v_{DS}= 1V.
   At these values, the transistor is in the linear/triode region, so

$$I_D = \frac{\mu_n W}{L}C_{ox}((v_{GS}-V_{tn})v_{DS} - \frac{v_{DS}^2}{2})$$

$$= 300\times100\times3.54\times10^{-7}(2-0.44)(1-\frac{1^2}{2})$$

$$= 0.011A$$

   (e) Find I_D at v_{GS}= 2V and v_{DS}= 2V.
   At these values, the transistor is in the saturation region.

$$I_D = \frac{\mu_n W}{2L}C_{ox}(v_{gs}-v_t)^2$$

$$= \frac{300}{2}\times100\times3.54\times10^{-7}\times(2-0.44)^2$$

$$= 0.013A$$

3. A circuit designer intending to operate a MOSFET in saturation is considering the effect of changing the device dimensions and operating voltages on the drain current I_D. Specifically, by what factor does I_D change in each of the following cases?

   (a) The channel length is doubled.
   The problem says that the MOSFET is in saturation. I_D in saturation is

   $$I_D = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})(v_{GS} - V_{tn})^2$$

   From the above equation, we see that I_D is inversely proportional to channel length. So, if channel length is doubled then I_D will be halved.

   (b) The channel width is doubled.
   I_D will be doubled (refer to equation for I_D in saturation above).

   (c) The overdrive voltage is doubled.
   Overdrive voltage is equal to v_{GS}- V_t, so I_D will quadruple if the overdrive voltage is doubled.

   (d) The drain to source voltage is doubled.
   If we doubled v_{DS}, there will be no effect on the drain current since v_{DS}already reaches overdrive voltage drain current saturates and remains constant.

   (e) Changes (a), (b), (c), and (d) are made simultaneously.
   Simultaneously doing change (a) and change (b) results in the current remaining constant. Double the overdrive voltage results in drain current quadrupling while (d) will not change drain current so the drainc current will stay

   (f) Which of these changes might cause the MOSFET to leave the saturation region?
   Decreasing v_{DS}may cause this since this may change the channel underneath.

5.6 Sources

- copy patse the sources from earlier chapters