Chapter 1

MOSFETs

A transistor comes from the two words **trans**conductance res**istor**. MOSFET stands for MOS field effect transistor since we are taking the MOS CAP and adding two extra diffusion regions. Most of the EE105 reader spents time on the NMOS device since most of the concepts can be carried over into analyzing the PMOS device too. A MOSFET is a three terminal device, so we are moving on form the junction diode, a basic two terminal device

Part of the motivation for learning about MOSFETs is for building a current source and also for voltage amplification. If we are able to form a voltage controlled current source, we can build a voltage amplifier.

1.1 Structure

- n^+: heavily doped n-type silicon
- n^-: lightly doped n-type silicon
- V_t: threshold voltage
- V_T: thermal voltage
- L: channel length

In figure 1.1, we see that the NMOS transistor has the gate, source, drain, and substrate/body terminal, as indicated by the first letters of each terminal. From its physical structure, we notice that a MOSFET is a symmetrical device and that the substrate forms a PN junction with the source and drain regions.

At zero gate voltage, we see that there are two back to back diodes in series between drain and source. One from the PN junction formed between the n^+ drain region and the p type substrate and the other from the n^+ source region and the p type substrate. These diodes prevent current conduction from drain to source when a voltage v_{ds} is applied.

1.2 NMOS: Current conduction

Suppose you ground the source and drain and $v_g > 0$. A positive gate voltage causes free holes to be repelled to the region of the substrate under the gate into the substrate. This leaves a **carrier-depletion region**. A positive gate voltage also attracts electrons from the n^+ source and drain regions to the channel region. Show in figure 1.2

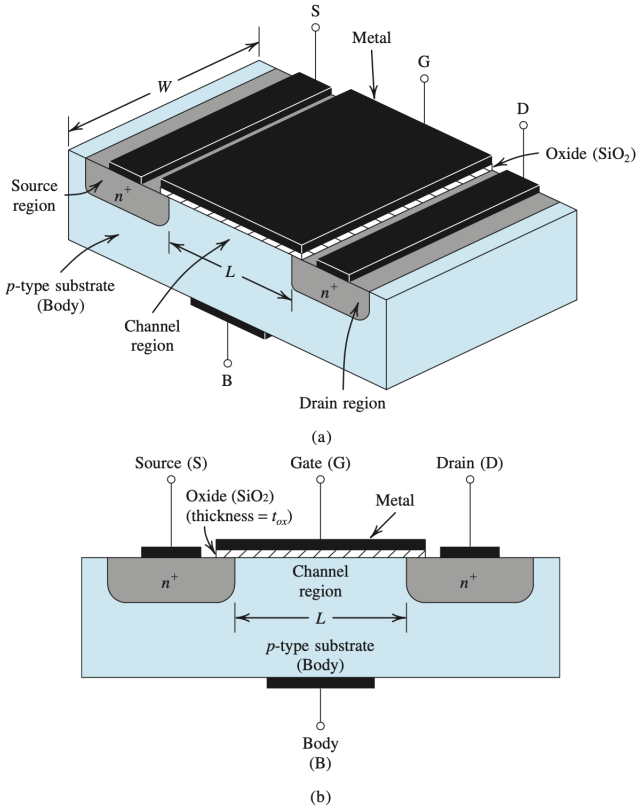


Figure 1.1: Physical structure of the NMOS transistor and a cross section view

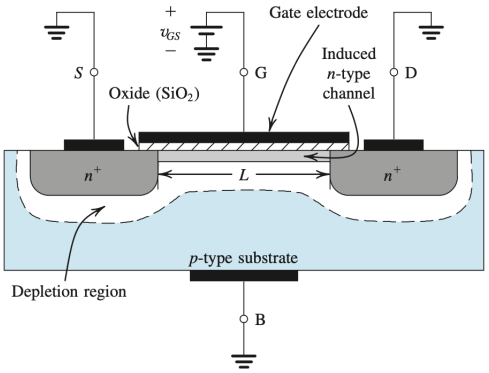


Figure 1.2: Positive voltage applied to the gate. An n channel is induced at the top of the substrate beneath the gate

We see that a **channel** is formed for current flow from the drain to source. **Threshold voltage** is also defined as the value of $v_{GS}$where a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel. **Overdrive voltage**, or **effective voltage** is the excess of v_{GS}over V_t.

$$v_{gs} - V_t \equiv v_{ov}$$

As v_{OV}increases, so does the magnitude of the channel charge. If drawn out, this looks like the an increase in the depth/deepness of the channel.

Another thing to keep in mind here is the **oxide capacitance**.

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

- C_{ox}: capacitance of the parallel-plate capacitor per unit gate area, F/m^2
- ϵ_{ox}: permittivity of silicon dioxide; $\epsilon_{ox} = 3.9\epsilon_0 = 3.45 \times 10^{-11}$ F/m
- t_{ox}: oxide thickness, determined by process technology

Analysis : Deriving i_D for small v_{DS}

We start by applying a small $v_{DS}$and v_{GS}greater than its threshold voltage. i_D is the current that Since i_D is the charge per unit channel length,

$$\frac{\mid Q \mid}{\text{unit channel length}} = C_{ox} W v_{OV}$$

We also know that channel conductance is proportional to the overdrive voltage, or $v_{GS}-V_t$. This means that current in the channel, i_D, is proportional to$(v_{GS}-V_t)$. v_{DS}also establishes an electric field E across the length of the channel given by:

$$\mid E \mid = \frac{v_{DS}}{L}$$

An electric field causes channel electrons to drift towards the drain with a velocity of:

$$\text{Electron drift velocity} = \mu_n \mid E \mid = \mu_n \frac{v_{DS}}{L}$$

Remembering that current is the rate of charged particles, then we find current by multiplying charge per unit channel length by the electron drift velocity.

$$i_D = [(\mu_n C_{ox})(\frac{W}{L})v_{OV}]v_{DS} = [(\mu_n C_{ox})(\frac{W}{L})(v_{GS} - V_t)]v_{DS}$$

Conductance of the channel is given by:

$$g_{DS} = (\mu_n C_{ox})(\frac{W}{L})v_{OV} = (\mu_n C_{ox})(\frac{W}{L})(v_{GS} - V_t)$$

Process transconductance parameter is given by:

$$K'_n = \mu_n C_{ox}$$

For a small v_{DS}, the MOSFET behaves with a linear resistance r_{DS} given by

$$r_{DS} = \frac{1}{g_{DS}} = \frac{1}{(\mu_n C_{ox})(W/L)v_{OV}}$$

If we increase v_{DS}, the depletion region will widen at the depletion region as a result of the increased v_{DS}that makes the channel shallower near the drain. This is reflected in the formula for i_D. We'll see that the channel looks more like a tapered shape, where it's deepest at the source end (proportional to v_{OV}) and shallowest at the drain end (proportional to v_{OV}- v_{DS}). Shown in figure 1.3.

$$i_D = \mu_n C_{ox}(\frac{W}{L})(V_{OV} - \frac{1}{2}v_{DS})v_{DS}$$

Figure 1.4 shows the drain current for different regions. Increasing v_{DS}beyond v_{OV}has no affect on the channel shape and charge. This is when the transistor enters saturation and the channel region resembles a right triangle with the deepest part being close to the source.

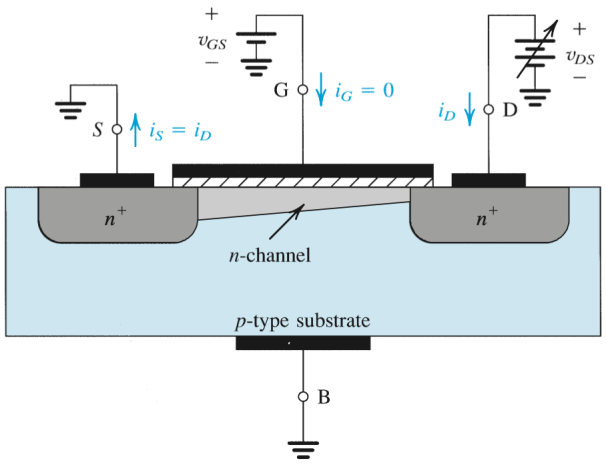


Figure 1.3: Operation of the enhancement NMOS transistor as $v_{DS}$is increased

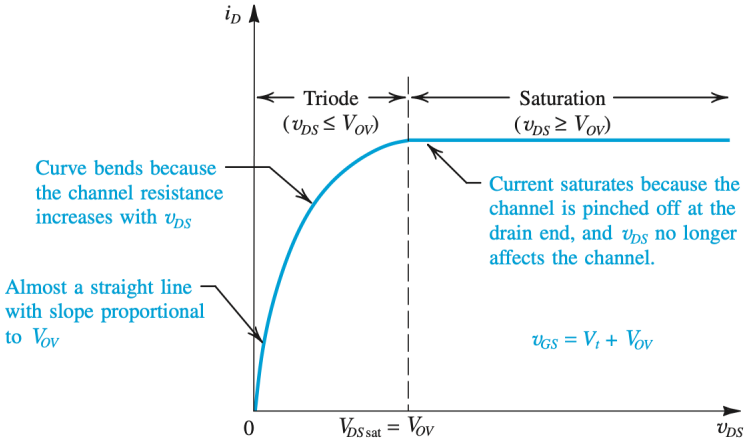


Figure 1.4: Operation of the enhancement NMOS transistor in different regions

1.3 PMOS: Structure and Current conduction

To conduct current here, we need to apply a negative voltage between the gate and the source. This is because the current here is carried by holes (current goes in the same direction as the holes, contrastingly from when current is carried by electrons) and flows from the source to the drain. If we had to compare the NMOS cross section with the PMOS cross section, then we would notice that the substrate type for a PMOS transistor is an n-type substrate with p^+-type wells for the source and drain, while this is switched for a NMOS transistor (p-type substrate with n^+-type wells for source and drain). We'll also notice that the direction of current is flowing from opposite wells.

- $k'_p = \mu_p C_{ox}$: process transconductance parameter for PMOS
- mu_p: mobility of the holes in the induced
- $k_p = k'_p(W/L)$: transistor transconductance parameter

Typically, NMOS transistors have greater gain and speed of operations than PMOS devices. Electron mobility μ_n is higher by factor of 2 to 4 than the hole mobility μ_p. The following attached PDF was something found online but sums up everything pretty nicely in a funny style.

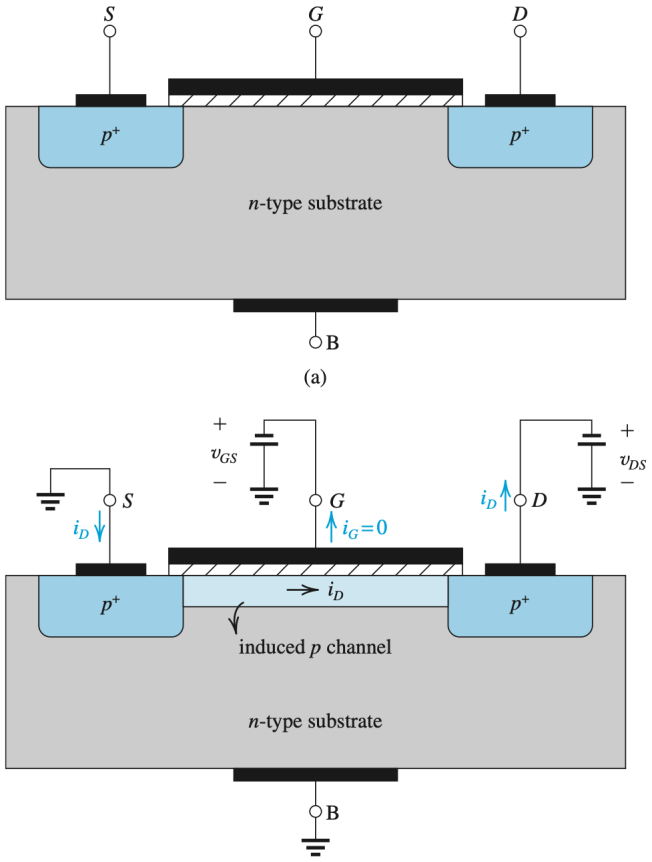


Figure 1.5: Physical structure of the PMOS structure and side view

1.4 Large and Small Signal Equivalent Models

Large signal equivalent model of an n-channel MOSFET operating in the saturation region

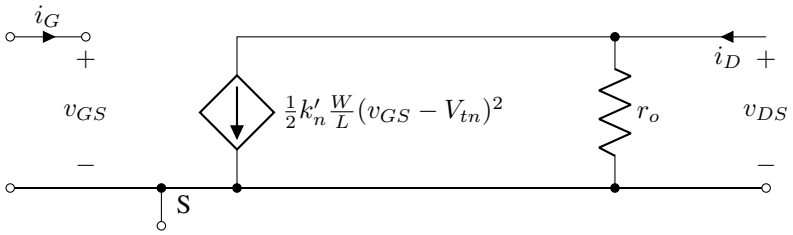


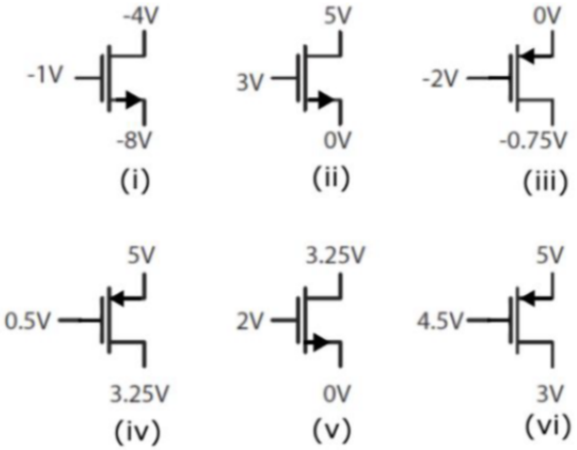
Figure 1.6: Large signal model operating in saturation drawn with outputresistance r_o

Future chapters will talk about the BJT (bipolar junction transistor).

- MOSFETs can be made smaller than BJTs
- MOSFET manufacturing process is relatively simpler and requires comparatively little powers
- MOSFETs generate less heat
- BJT better for current amplification circuits
- BJT low on-state voltage drop and low conduction loss
- BJT preferred in high power applications due to higher power handling; MOSFET preferred for low power applications

1.5 Practice Problems

1. Find the region of operation for the following transistors. You may use $V_{tn} = 0.9$V and $|V_{tp} = 1$V. The operation condition of NMOS is also shown. PMOS is conducted by holes which is opposite to NMOS so the voltage polarity is different.



Region of operation	Condsitions	i_{DS}
Cut-off	v_{GS}< V_T	$i_{DS}\sim$ 0A
Linear/Triode	$V_{GS} > V_T, V_{DS} < V_{GS} - V_T$	i_{DS}= $\frac{W}{L}\mu_n C_{ox}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}$
Saturation:	$V_{GS} > V_T, V_{DS} > V_{GS} - V_T$	i_{DS}= $\frac{W}{L}\frac{\mu_n C_{ox}}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$

(a) We identify this transistor as a NMOS transistor due to the direction of the arrow. In a NMOS transistor, current flows from drain to source due to electrons being the charge carriers in the NMOS transistor. v_{GS}= $v_G - v_S$ = 7V and v_{DS}= $v_D - v_S = -4 - (-8) - 4$V. This transistor is in the linear/triode region.

(b) v_{GS}= 3V and v_{DS}= 5V. This transistor is in the saturation region.

(c) This is a PMOS transistor. In a PMOS transistor, current flows from source to drain. $|v_{GS}| = 2$V and $|v_{DS}| = 0.75$V. This is in the linear/triode region.

(d) $|v_{GS}| = 4.5$V and $|v_{DS}| = |3.25 - 5| = 1.75$V. This is in the linear/triode region.

(e) $v_{GS} = 2$V and $v_{DS} = 3.25 - 0 = 3.25$V. This is in the saturation region.

(f) $|v_{GS}| = |4.5 - 5| = 0.5$V. This is in the cutoff region.

2. An ideal N-channel MOSFET has the following parameters: $W = 100\ \mu$m, $L = 1\ \mu$m, $t_{ox} = 15$ nm, the oxide relative permittivity is 4, the silicon relative permittivity is 12, $N_A = 10^{15}$ cm^{-3}, $n_i = 10^{10}$ cm^{-3}, $V_{FB} = -0.2$ V, $\mu_n = 300$ cm^2/V $\cdot$ sat 300K. $\lambda = 0$.

   (a) Find the threshold voltage.
   Threshold voltage is given by the following formula:

$$\phi_B = \frac{kT}{q}\ln\frac{N_A}{n_i} = 0.026V\ln\left(\frac{10^{15}\text{cm}^{-3}}{10^{10}\text{cm}^{-3}}\right) = 0.2993\ldots V$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{4(8.854\times10^{-14}\text{F/cm})}{15\text{nm}} = 3.54\times10^{-7}\text{F/cm}^2$$

$$V_t = V_{FB} + 2\phi_B + \frac{\sqrt{2q\epsilon_s N_A 2\phi_B}}{C_{ox}}$$

$$= -0.2 + 2(0.299) + \frac{2(12)(8.854\times10^{14}\text{F/cm})(1.602\times10^{-19}C)(10^{15}\text{cm}^{-3})(2)(0.2993V)}{3.54\times10^{-7}\text{F/cm}^2}$$

$$= 0.44\text{V}$$

   (b) What is the minumum v_{DS}value for the MOSFET to be at saturation region at v_{GS}= 2V.
   For the MOSFET to remain in saturation, v_{DS}= v_{GS}- V_tn, so

$$V_{DS} - V_{DS} - V_{tn} = 2 - 0.44 = 1.56\text{V}$$

   (c) Find the channel resistance at v_{GS}= 2V and v_{DS}= 0.01 V.
   Channel resistance is given by calculating what $i_{DS}$is given that we know $v_{DS}$is.

$$R_{ch} = \frac{V_{DS}}{I_{DS}} = \frac{0.01V}{\frac{W}{L}\mu_n C_{ox}(V_{GS}-V_T)V_{DS}}$$

$$= \frac{1}{300\times100\times3.54\times10^{-7}\times1.56}$$

$$= 60.36\Omega$$

   (d) Find I_D at v_{GS}= 2V and v_{DS}= 1V.
   At these values, the transistor is in the linear/triode region, so

$$I_D = \frac{\mu_n W}{L}C_{ox}((v_{GS}-V_{tn})v_{DS} - \frac{v_{DS}^2}{2})$$

$$= 300\times100\times3.54\times10^{-7}(2-0.44)(1-\frac{1^2}{2})$$

$$= 0.011A$$

   (e) Find I_D at v_{GS}= 2V and v_{DS}= 2V.
   At these values, the transistor is in the saturation region.

$$I_D = \frac{\mu_n W}{2L}C_{ox}(v_{gs}-v_t)^2$$

$$= \frac{300}{2}\times100\times3.54\times10^{-7}\times(2-0.44)^2$$

$$= 0.013A$$

3. A circuit designer intending to operate a MOSFET in saturation is considering the effect of changing the device dimensions and operating voltages on the drain current I_D. Specifically, by what factor does I_D change in each of the following cases?

   (a) The channel length is doubled.
   The problem says that the MOSFET is in saturation. I_D in saturation is

   $$I_D = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})(v_{GS} - V_{tn})^2$$

   From the above equation, we see that I_D is inversely proportional to channel length. So, if channel length is doubled then I_D will be halved.

   (b) The channel width is doubled.
   I_D will be doubled (refer to equation for I_D in saturation above).

   (c) The overdrive voltage is doubled.
   Overdrive voltage is equal to v_{GS}- V_t, so I_D will quadruple if the overdrive voltage is doubled.

   (d) The drain to source voltage is doubled.
   If we doubled v_{DS}, there will be no effect on the drain current since v_{DS}already reaches overdrive voltage drain current saturates and remains constant.

   (e) Changes (a), (b), (c), and (d) are made simultaneously.
   Simultaneously doing change (a) and change (b) results in the current remaining constant. Double the overdrive voltage results in drain current quadrupling while (d) will not change drain current so the drainc current will stay

   (f) Which of these changes might cause the MOSFET to leave the saturation region?
   Decreasing v_{DS}may cause this since this may change the channel underneath.

1.6 Sources

- copy patse the sources from earlier chapters