

*Dmell*

## Lab 2 Answer Sheet

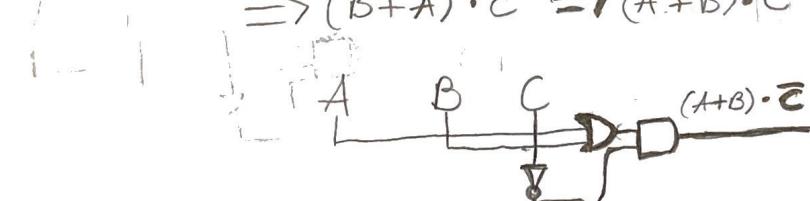
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 Date: 1/31/22

### PRELAB:

**Q1.** Read section 3.0 and fill in the truth table below for *lab2step1*. Then use it to construct the SOP expression and draw the resulting circuit using logic gates.

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

SOP Logic Expression:  $\overline{ABC} + \overline{AB}\overline{C} + \overline{A}\overline{B}\overline{C}$   
 $\Rightarrow \overline{BC}(A+\overline{A}) + \overline{AB}\overline{C} \Rightarrow \overline{BC}(1) + \overline{AB}\overline{C}$   
 $\Rightarrow \overline{BC} + \overline{AB}\overline{C} \Rightarrow (B+(\overline{B}\cdot A))\cdot \overline{C} \Rightarrow (B+A)\cdot \overline{C}$   
 $\Rightarrow (B+A)\cdot \overline{C} \Rightarrow (\overline{A}+\overline{B})\cdot \overline{C}$

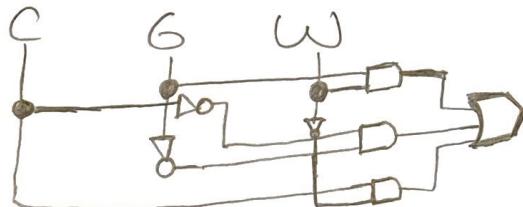


TA Initials: \_\_\_\_\_

Q2. Read section 4.0 and fill in the truth table below for *lab2step2*. Then use it to construct the SOP expression and draw the resulting circuit using logic gates.

Cabbage	Goat	Wolf	Alarm
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

SOP Logic Expression:  $\overline{C}\overline{G}\overline{W} + \overline{C}\overline{G}W + \overline{C}GW + C\overline{G}\overline{W} + C\overline{G}W + CGW$   
 $\Rightarrow \overline{C}\overline{G}(\overline{W}+W) + GW(\overline{C}+C) + C(\overline{W}(\overline{G}+G))$   
 Circuit Diagram:  $\Rightarrow \overline{C}\overline{G} + GW + CW$



TA Initials: \_\_\_\_\_

**LAB:**

3.0 Hardware results demonstrate a correct circuit. TA Initials: M.K.S

4.0 Hardware results demonstrate a correct circuit. TA Initials: M.K.S