Cpr E 281 LAB08
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Lab 8 Answer Sheet

Name and Std ID: [redacted] 053855830 Lab Section: 1

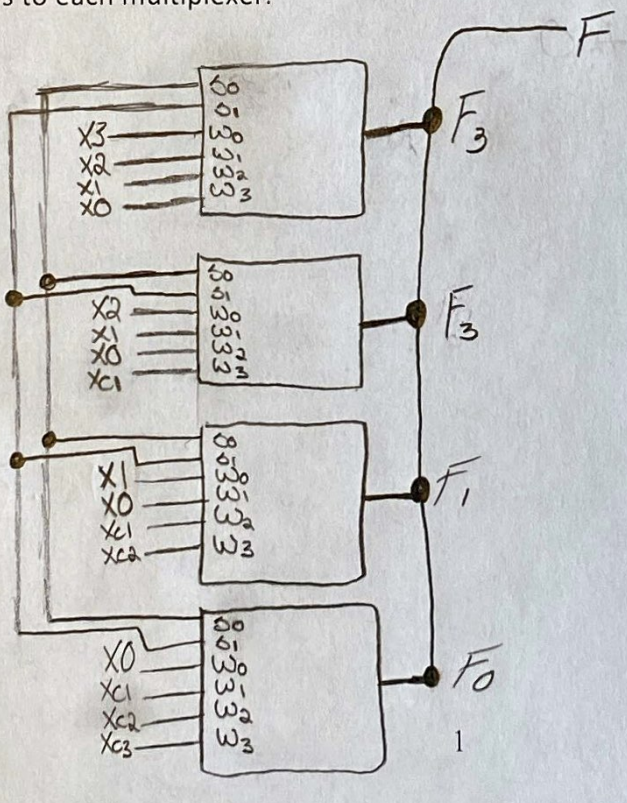
Date: 03/28/22

PRELAB:

Q1. Read section 2.2 and write the Verilog code for a 4-to-1 multiplexer.

```
module mux4to1 (w0,w1,w2,w3,S,F);
    input w0,w1,w2,w3,S[1:0];
    output F;
    reg F;
    always @(S[1:0])
    begin
        case({S[1:0]})
            2'b00: f=w0;
            2'b01: f=w1;
            2'b10: f=w2;
            2'b11: f=w3;
        endcase
    end
endmodule
```

Q2. Design a 4-bit shifter as described in Section 3.1 of the lab description. Sketch the block diagram for your design showing the multiplexers, the inputs, outputs and the selectors to each multiplexer.



Cpr E 281 LAB08
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Lab 8 Answer Sheet

Q3. Refer to Section 3.1 of the lab description and complete the following table before you come to the lab:

X3	X2	X1	X0	Xc1	Xc2	Xc3	S1	S0	F3	F2	F1	F0
1	0	0	1	1	1	0	0	1	0	0	1	1
1	1	1	0	0	0	0	1	1	0	0	0	0
1	1	1	0	0	1	1	0	0	1	1	1	0
1	1	0	1	0	1	0	1	0	0	1	0	1
1	0	1	1	0	1	1	0	1	0	1	1	0

x xo

TA Initials: _____

LAB:

2.4 Hardware results demonstrate a good circuit. TA Initials: M.K.S

3.1 ModelSim results demonstrate correct code. TA Initials: M.K.S.