Dan Mitchell

03/20/22 Homework 06

1)

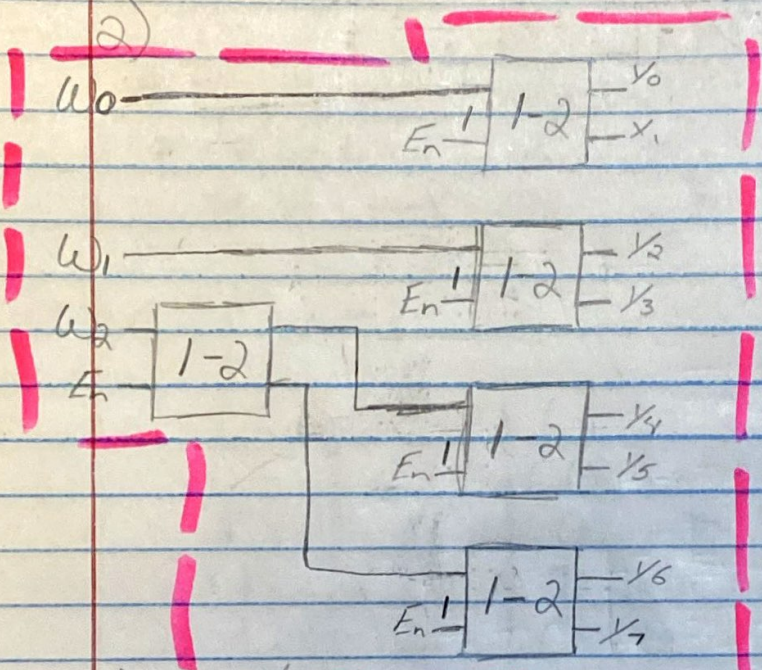
a. 5 decoders are necessary.

b. 9 decoders are necessary

c. 7 mux are necessary

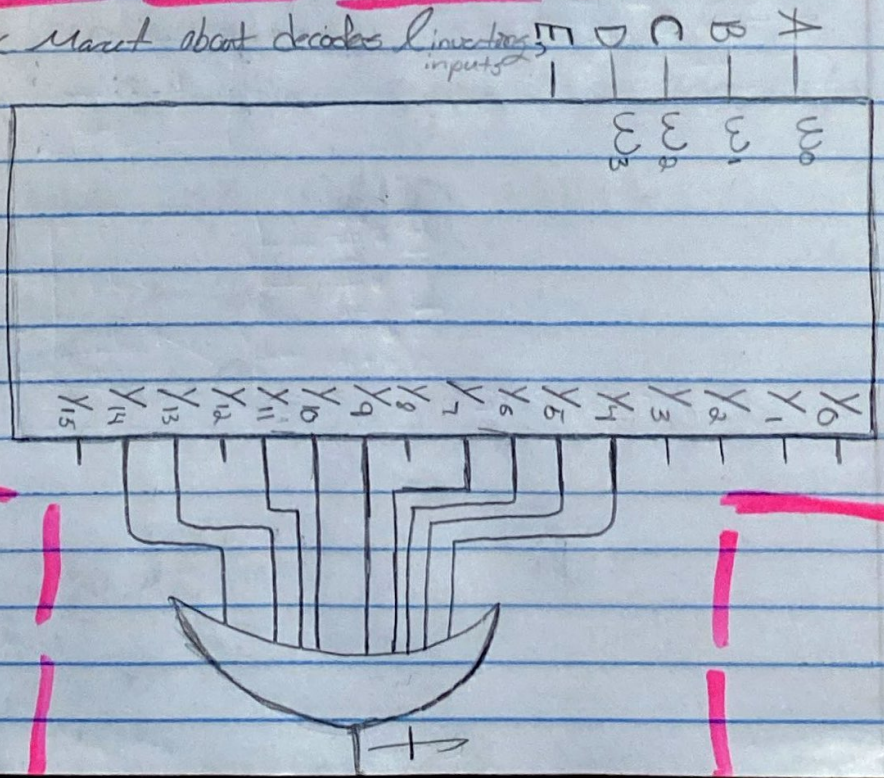
d. 8 mux are necessary

2)

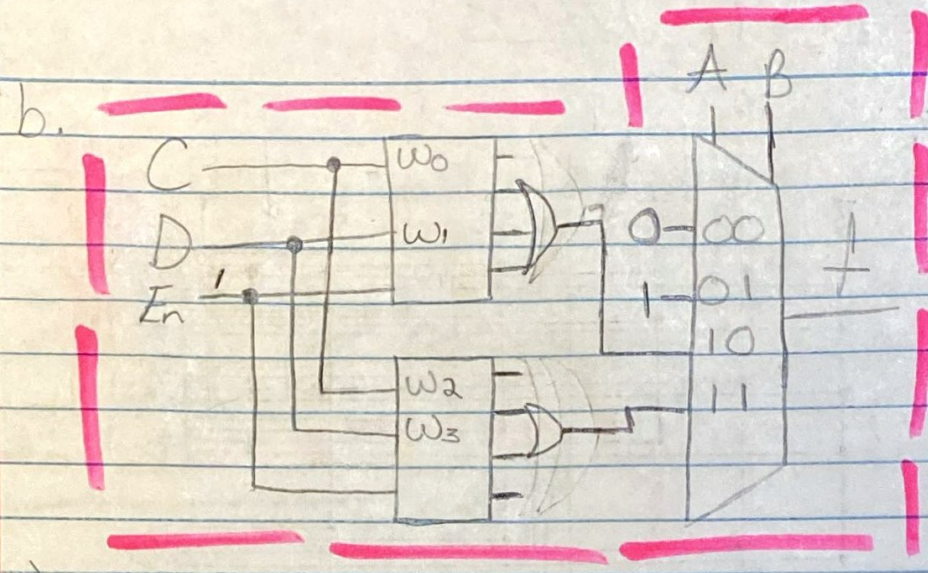


3)

a. *ask Marcel about decoders (inverting inputs)

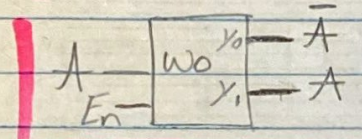


b.

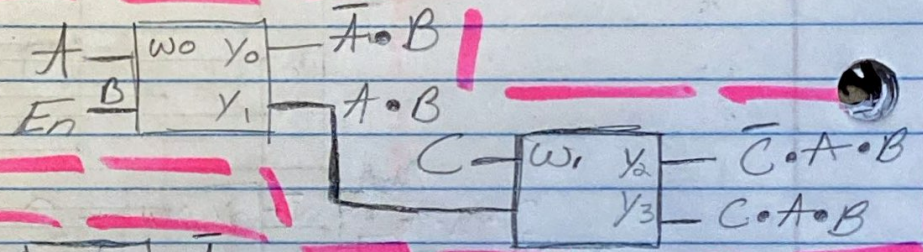

A B
C
D
En
1
W0
W1
W2
W3
0
1
00
01
10
11

4)

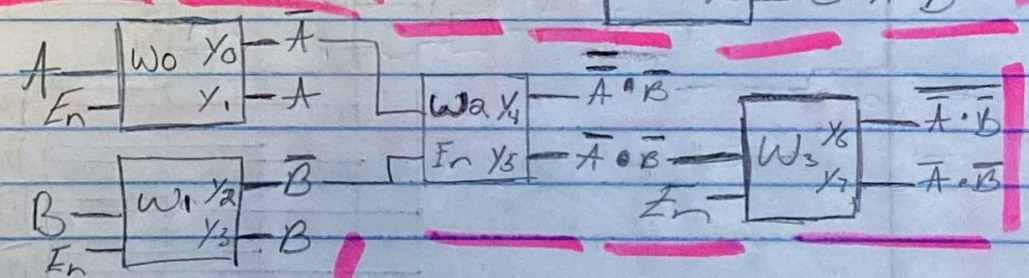
a.


A
En
W0
Y0
Y1
$\bar{A}$
A

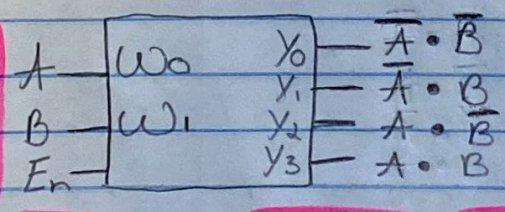
b.


A
B
En
W0
Y0
Y1
$\bar{A} \cdot B$
$A \cdot B$
C
W1
Y2
Y3
$\bar{C} \cdot A \cdot B$
$C \cdot A \cdot B$

C.


A
En
W0
Y0
Y1
$\bar{A}$
A
B
En
W1
Y2
Y3
$\bar{B}$
B
W2
Y4
En
Y5
$\bar{A} \cdot \bar{B}$
$\bar{A} \cdot \bar{B}$
W3
Y6
Y7
$\overline{\bar{A} \cdot \bar{B}}$
$\overline{\bar{A} \cdot \bar{B}}$
En

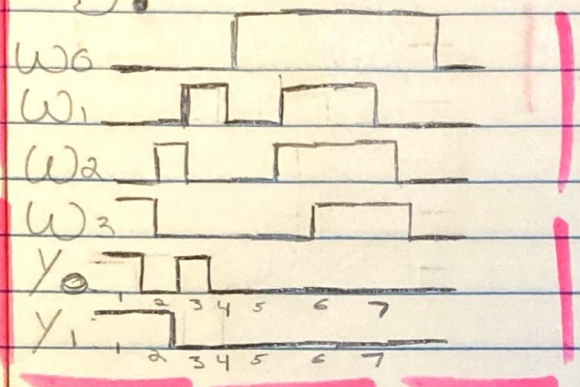
d.


A
B
En
W0
W1
Y0
Y1
Y2
Y3
$\bar{A} \cdot \bar{B}$
$\bar{A} \cdot B$
$A \cdot \bar{B}$
$A \cdot B$

5)

a. already solved

b.



* c. The 4-2 binary encoder's inputs are contrary to its input assumptions as binary encoders are one hot encoded, & these are multiple points in the timing diagram where more than one input is high.

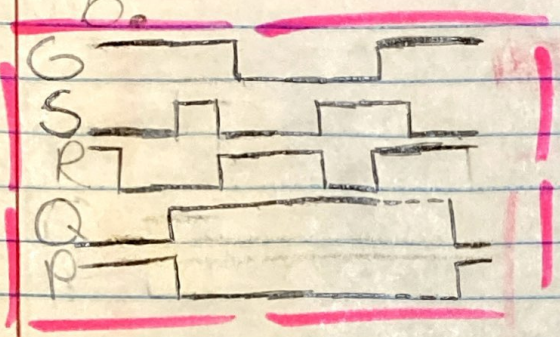
6)

clock → Q=1 set → Q=0 Reset

a.

G	S	R	Q	P
0	0	0	0/1	1/0
0	0	1	0/1	1/0
0	1	0	0/1	1/0
0	1	1	0/1	1/0
1	0	0	0/1	1/0
1	0	1	0	1
1	1	0	1	0
1	1	1	X	X

b.



* ---- denotes undesirable state