IOWA STATE UNIVERSITY

Lab 4 Answer Sheet

Name and Student ID: Dr. Small 053855830 **Lab Section:**

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PRELAB:

Q1. Consider the Verilog code in section 3.0. Briefly explain how the **always @** structure works. 'always @' is one of the procedural blocks in Verilog code. Statements inside an 'always @' block are executed sequentially.

Syntax: always @(event) statement or always @(event) begin statements end

Also used for combinational events, as done in section 3.0.

A continuous process that gets triggered & performs some action when a signal in its sensitivity list becomes active/changes.

- Procedural blocks require signals (such as outputs) to be declared as 'reg'.

Q2. Write the Verilog code for ***lab4step1***. Use the example code given in Section 3.0 and make the necessary changes.

```
module lab4step1(C,G,W,A);
    input C,G,W;
    output A;
    reg A;

    always @(C or G or W)
    begin
        case({C,G,W})
            3'b000: A='b1;
            3'b001: A='b1;
            3'b010: A='b0;
            3'b011: A='b1;
            3'b100: A='b1;
            3'b101: A='b0;
            3'b110: A='b1;
            3'b111: A='b1;
        endcase
    end
endmodule
```

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Q3. Read Section 4.0 and fill in the Truth Table for ***lab4step2***.

Inputs				Outputs		
M	T	H	P	E	F	AC
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	1	0	1
0	1	0	0	0	0	0
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	0	0	0
1	0	1	1	1	0	0
1	1	0	0	0	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	1	1	1