CPRE 281: HW 00 - [illegible]

1)

A) CAD - computer-aided definition
B) PLD - programmable logic device
C) FPGA - field-programmable gate array
D) ASIC - application-specific integrated circuit

2)

A) The implementation-testing-verification loop is relatively more expensive as you are actually implementing the new development & testing it, as opposed to only simulating the initial design. If the implementation does not meet specifications, correcting & reimplementing will be more expensive than redesigning.

B) Neither loop can be avoided for the following reasons: You can not implement a solution without designing one & ensuring that all specifications are met. Additionally, only simulating if your initial design meets the specifications does not truly ensure that it will succeed in the real world.

3)

A) $1111010_2 = 64+32+16+8+2 = \boxed{122}$

B) $1101_3 = 8+4+1 = \boxed{13}$

C) $1110_8 = 8^3 + 8^2 + 8 = 512+64+8 = \boxed{584}$

D) $123_{16} = 16^2 + (2 \cdot 16) + 3 = 256+32+3 = \boxed{291}$

E) $CAD_{16} = (16^2 \cdot 12) + (16 \cdot 10) + (13 \cdot 1) = 3072+160+13 = \boxed{3245}$

1 1 1 1 1
96 + 16 = 112 + 2 + 1

128 64 32 16 8 4 2 1

4)

OR: 2 7 1

010 111 001

A) $28_{10} = 11100_2$

B) $115_{10} = 1110011_2$

C) $127_{10} = 1111111_2$

D) $271_8 = (2 \cdot 64) + (7 \cdot 8) + 1 = 185 = 10111001_2$

E) $CODE_{16} = 12\ 0\ 13\ 14 = 1100000011011110_2$

$16^3\ 16^2\ 16^1\ 16^0$

1100 0000 1101 1110

5)

A) • $48_{16} = 01001000_2 = 72_{10} = H$

• $65_{16} = 01100101_2 = 101_{10} = e$

• $6C_{16} = 01101100_2 = 108_{10} = l$

• $6f_{16} = 01101111_2 = 111_{10} = o$

• $21_{16} = 00100001_2 = 33_{10} = !$

B) $[48_{16}\ 65_{16}\ 6c_{16}\ 6c_{16}\ 6f_{16}\ 21_{16}] = Hello!$

6) 1) M=1, S=0, R=0, T=0 takeout

2) M=1, S=0, R=1, T=1 takeout & delivery

3) M=0, S=1, R=1, T=1 delivery

4) M=0, S=0, R=1, T=1 delivery

5) M=1, S=1, R=1, T=1 delivery