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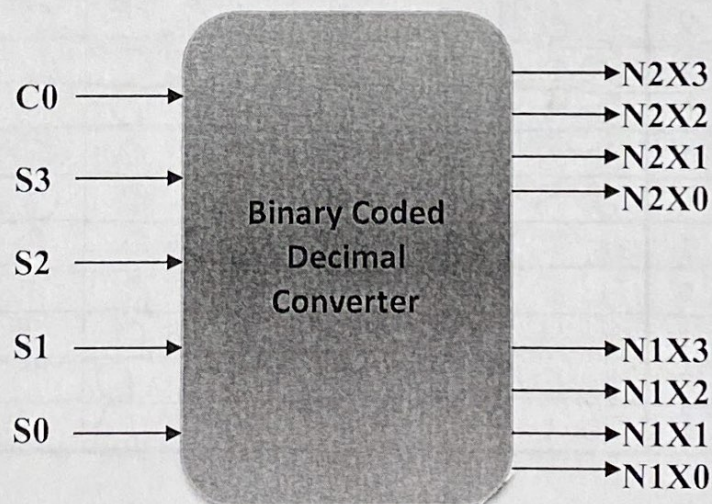
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**PRELAB:**

**Q1.** Add the following numbers then write them in decimal:

Binary numbers to add a3 a2 a1 a0 + b3 b2 b1 b0	Binary result C0 S3 S2 S1 S0	Decimal conversion N2 N1 (X3 X2 X1 X0) (X3 X2 X1 X0)
1001 + 0111	10000	16
1011 + 1001	10100	20
1110 + 0101	10011	19
0010 + 1110	10000	16
1101 + 1011	11000	24

**Q2.** Consider the five-bit binary result (C0, S3, S2, S1, S0) representation in the table above. We would like to represent each combination as its equivalent in two decimal digits, each of which can be represented in binary as shown in the following table. Finish filling in the following truth table.





## Lab 6 Answer Sheet

C0	S3	S2	S1	S0	Decimal	N2X3	N2X2	N2X1	N2X0	N1X3	N1X2	N1X1	N1X0
0	0	0	0	0	0 0	0	0	0	0	0	0	0	0
0	0	0	0	1	0 1	0	0	0	0	0	0	0	1
0	0	0	1	0	0 2	0	0	0	0	0	0	1	0
0	0	0	1	1	0 3	0	0	0	0	0	0	1	1
0	0	1	0	0	0 4	0	0	0	0	0	1	0	0
0	0	1	0	1	0 5	0	0	0	0	0	1	0	1
0	0	1	1	0	0 6	0	0	0	0	0	1	1	0
0	0	1	1	1	0 7	0	0	0	0	0	1	1	1
0	1	0	0	0	0 8	0	0	0	0	1	0	0	0
0	1	0	0	1	0 9	0	0	0	0	1	0	0	1
0	1	0	1	0	1 0	0	0	0	1	0	0	0	0
0	1	0	1	1	1 1	0	0	0	1	0	0	0	1
0	1	1	0	0	1 2	0	0	0	1	0	0	1	0
0	1	1	0	1	1 3	0	0	0	1	0	0	1	1
0	1	1	1	0	1 4	0	0	0	1	0	1	0	0
0	1	1	1	1	1 5	0	0	0	1	0	1	0	1
1	0	0	0	0	1 6	0	0	0	1	0	1	1	0
1	0	0	0	1	1 7	0	0	0	1	0	1	1	1
1	0	0	1	0	1 8	0	0	0	1	0	0	0	0
1	0	0	1	1	1 9	0	0	0	1	0	0	0	1
1	0	1	0	0	2 0	0	0	1	0	0	0	0	0
1	0	1	0	1	2 1	0	0	1	0	0	0	0	1
1	0	1	1	0	2 2	0	0	1	0	0	0	1	0
1	0	1	1	1	2 3	0	0	1	0	0	0	1	1
1	1	0	0	0	2 4	0	0	1	0	0	1	0	0
1	1	0	0	1	2 5	0	0	1	0	0	1	0	1
1	1	0	1	0	2 6	0	0	1	0	0	1	1	0
1	1	0	1	1	2 7	0	0	1	0	0	1	1	1
1	1	1	0	0	2 8	0	0	1	0	1	0	0	0
1	1	1	0	1	2 9	0	0	1	0	1	0	0	1
1	1	1	1	0	3 0	0	0	1	1	0	0	0	0
1	1	1	1	1	3 1	0	0	1	1	0	0	0	1



**Q3.** Find the logic expressions for N2X3, N2X2, N2X1, N2X0, N1X3, N1X2, N1X1, and N1X0 as a function of C0, S3, S2, S1 and S0:

N2X3 = 0

N2X2 = 0

$$\begin{aligned} N2X1 = & \overline{C_0} \overline{S_3} S_2 \overline{S_1} \overline{S_0} + \overline{C_0} \overline{S_3} S_2 S_1 \overline{S_0} + \overline{C_0} \overline{S_3} S_2 S_1 S_0 + \overline{C_0} \overline{S_3} S_2 \overline{S_1} S_0 \\ & + \overline{C_0} S_3 \overline{S_2} \overline{S_1} \overline{S_0} + \overline{C_0} S_3 \overline{S_2} \overline{S_1} S_0 + \overline{C_0} S_3 \overline{S_2} S_1 \overline{S_0} + \overline{C_0} S_3 \overline{S_2} S_1 S_0 \\ & + \overline{C_0} S_3 S_2 \overline{S_1} \overline{S_0} + \overline{C_0} S_3 S_2 \overline{S_1} S_0 + \overline{C_0} S_3 S_2 S_1 \overline{S_0} + \overline{C_0} S_3 S_2 S_1 S_0 \end{aligned}$$

$$\begin{aligned} N2X0 = & \overline{C_0} \overline{S_3} \overline{S_2} S_1 \overline{S_0} + \overline{C_0} \overline{S_3} \overline{S_2} S_1 S_0 + \overline{C_0} \overline{S_3} \overline{S_2} \overline{S_1} \overline{S_0} + \overline{C_0} \overline{S_3} \overline{S_2} \overline{S_1} S_0 + \overline{C_0} \overline{S_3} \overline{S_2} S_1 \overline{S_0} \\ & + \overline{C_0} \overline{S_3} \overline{S_2} S_1 S_0 + \overline{C_0} \overline{S_3} \overline{S_2} \overline{S_1} \overline{S_0} + \overline{C_0} \overline{S_3} \overline{S_2} \overline{S_1} S_0 + \overline{C_0} \overline{S_3} \overline{S_2} S_1 \overline{S_0} \\ & + \overline{C_0} \overline{S_3} \overline{S_2} S_1 S_0 + \overline{C_0} \overline{S_3} \overline{S_2} \overline{S_1} \overline{S_0} + \overline{C_0} \overline{S_3} \overline{S_2} \overline{S_1} S_0 + \overline{C_0} \overline{S_3} \overline{S_2} S_1 \overline{S_0} \end{aligned}$$

$$\begin{aligned} N1X3 = & \overline{C_0} \overline{S_3} \overline{S_2} \overline{S_1} \overline{S_0} + \overline{C_0} \overline{S_3} \overline{S_2} \overline{S_1} S_0 + \overline{C_0} \overline{S_3} \overline{S_2} S_1 \overline{S_0} + \overline{C_0} \overline{S_3} \overline{S_2} S_1 S_0 \\ & + \overline{C_0} S_3 \overline{S_2} \overline{S_1} \overline{S_0} + \overline{C_0} S_3 \overline{S_2} \overline{S_1} S_0 + \overline{C_0} S_3 \overline{S_2} S_1 \overline{S_0} + \overline{C_0} S_3 \overline{S_2} S_1 S_0 \end{aligned}$$

$$\begin{aligned} N1X2 = & \overline{C_0} \overline{S_3} S_2 \overline{S_1} \overline{S_0} + \overline{C_0} \overline{S_3} S_2 \overline{S_1} S_0 + \overline{C_0} \overline{S_3} S_2 S_1 \overline{S_0} + \overline{C_0} \overline{S_3} S_2 S_1 S_0 \\ & + \overline{C_0} S_3 \overline{S_2} \overline{S_1} \overline{S_0} + \overline{C_0} S_3 \overline{S_2} \overline{S_1} S_0 + \overline{C_0} S_3 \overline{S_2} S_1 \overline{S_0} + \overline{C_0} S_3 \overline{S_2} S_1 S_0 \end{aligned}$$

$$\begin{aligned} N1X1 = & \overline{C_0} \overline{S_3} \overline{S_2} S_1 \overline{S_0} + \overline{C_0} \overline{S_3} \overline{S_2} S_1 S_0 + \overline{C_0} \overline{S_3} S_2 \overline{S_1} \overline{S_0} + \overline{C_0} \overline{S_3} S_2 \overline{S_1} S_0 \\ & + \overline{C_0} \overline{S_3} S_2 S_1 \overline{S_0} + \overline{C_0} \overline{S_3} S_2 S_1 S_0 + \overline{C_0} S_3 \overline{S_2} \overline{S_1} \overline{S_0} + \overline{C_0} S_3 \overline{S_2} \overline{S_1} S_0 \\ & + \overline{C_0} S_3 \overline{S_2} S_1 \overline{S_0} + \overline{C_0} S_3 \overline{S_2} S_1 S_0 + \overline{C_0} S_3 S_2 \overline{S_1} \overline{S_0} + \overline{C_0} S_3 S_2 \overline{S_1} S_0 \end{aligned}$$

$$\begin{aligned} N1X0 = & \overline{C_0} \overline{S_3} \overline{S_2} S_1 \overline{S_0} + \overline{C_0} \overline{S_3} \overline{S_2} S_1 S_0 + \overline{C_0} \overline{S_3} S_2 \overline{S_1} \overline{S_0} + \overline{C_0} \overline{S_3} S_2 \overline{S_1} S_0 \\ & + \overline{C_0} \overline{S_3} S_2 S_1 \overline{S_0} + \overline{C_0} \overline{S_3} S_2 S_1 S_0 + \overline{C_0} S_3 \overline{S_2} \overline{S_1} \overline{S_0} + \overline{C_0} S_3 \overline{S_2} \overline{S_1} S_0 \\ & + \overline{C_0} S_3 \overline{S_2} S_1 \overline{S_0} + \overline{C_0} S_3 \overline{S_2} S_1 S_0 + \overline{C_0} S_3 S_2 \overline{S_1} \overline{S_0} + \overline{C_0} S_3 S_2 \overline{S_1} S_0 \\ & + \overline{C_0} S_3 S_2 S_1 \overline{S_0} + \overline{C_0} S_3 S_2 S_1 S_0 \end{aligned}$$



## Lab 6 Answer Sheet

Q4. Write the Verilog code for the Binary Coded Decimal Converter from Section 3.3 using the assign statement.

Example:

module

input ...

output ...

assign ...

endmodule

\* Using Kmaps on scratch paper: \*\*  $N2X3 = 0$   
\*\*  $N2X2 = 0$   
\*  $N2X1 = C0S2 + C0S3$   
\*  $N2X0 = \overline{C0}S3S1 + \overline{C0}S3S2 + S3S2S1 + C0S3\overline{S2}$   
\*  $N1X3 = \overline{C0}S3\overline{S2}S1 + C0S3\overline{S2}S1 + C0S3S2S1$   
\*  $N1X2 = \overline{C0}S3S2 + C0S2S1 + C0S2S1 + C0S3\overline{S2}$   
\*  $N1X1 = \overline{C0}S3S1 + \overline{S3}S2S1 + C0S3S2S1 + C0S3\overline{S2}S1 + C0S3S2S1$   
\* \*  $N1X0 = 0$

```

module bcDc(C0, S3, S2, S1, S0, N2X1, N2X0, N1X3, N1X2, N1X1);
    input C0, S3, S2, S1, S0;
    output N2X1, N2X0, N1X3, N1X2, N1X1;
    assign N2X1 = C0 & S2 | C0 & S3;
    assign N2X0 = ~C0 & S3 & S1 | ~C0 & S3 & S2 | S3 & S2 & S1 | C0 & ~S3 & ~S2;
    assign N1X3 = ~C0 & S3 & ~S2 & S1 | C0 & ~S3 & ~S2 & S1 | C0 & S3 & S2 & S1;
    assign N1X2 = ~C0 & ~S3 & S2 | ~C0 & S2 & S1 | C0 & ~S2 & S1 | C0 & S3 & ~S2;
    assign N1X1 = ~C0 & ~S3 & S1 | ~S3 & S2 & S1 | ~C0 & S3 & S2 & S1 |
    | C0 & ~S3 & ~S2 & S1 | C0 & S3 & ~S2 & S1;
endmodule

```

TA Initials: \_\_\_\_\_

LAB:

Hardware demonstrates a good design. TA Initials: \_\_\_\_\_