# Lab 2 Answer Sheet

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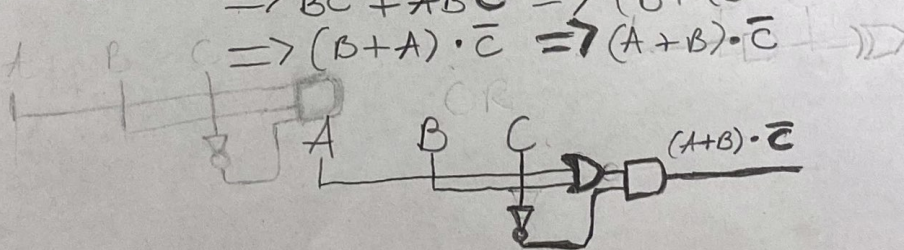
**Date:** 1/31/22

## PRELAB:

**Q1.** Read section 3.0 and fill in the truth table below for *lab2step1*. Then use it to construct the SOP expression and draw the resulting circuit using logic gates.

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

**SOP Logic Expression:** $\overline{A}B\overline{C} + A\overline{B}\overline{C} + AB\overline{C}$

$\Rightarrow B\overline{C}(A + \overline{A}) + A\overline{B}\overline{C} \Rightarrow B\overline{C}(1) + A\overline{B}\overline{C}$

**Circuit Diagram:**

$\Rightarrow B\overline{C} + A\overline{B}\overline{C} \Rightarrow (B + (\overline{B} \cdot A) \cdot \overline{C} \Rightarrow (B + A) \cdot \overline{C}$

$\Rightarrow (B + A) \cdot \overline{C} \Rightarrow (A + B) \cdot \overline{C}$

$(A + B) \cdot \overline{C}$

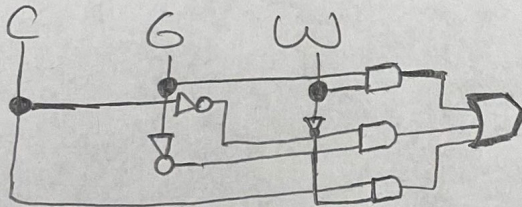**TA Initials:** _____

**Q2.** Read section 4.0 and fill in the truth table below for *lab2step2*. Then use it to construct the SOP expression and draw the resulting circuit using logic gates.

| Cabbage | Goat | Wolf | Alarm |
|---------|------|------|-------|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

SOP Logic Expression: $\overline{C}\,\overline{G}\,\overline{W} + \overline{C}\,\overline{G}\,W + \overline{C}\,G\,W + C\,\overline{G}\,\overline{W} + C\,G\,\overline{W} + C\,G\,W$

$\Rightarrow \overline{C}\,\overline{G}\,(\overline{W}+W) + G\,W\,(\overline{C}+C) + C\,\overline{W}\,(\overline{G}+G)$

Circuit Diagram: $\Rightarrow \overline{C}\,\overline{G} + G\,W + C\,\overline{W}$



TA Initials: _____

**LAB:**

**3.0** Hardware results demonstrate a correct circuit. TA Initials: _____

**4.0** Hardware results demonstrate a correct circuit. TA Initials: _____