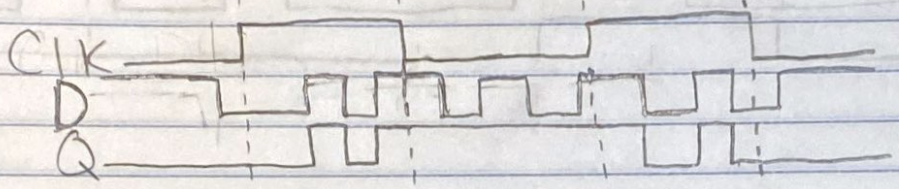
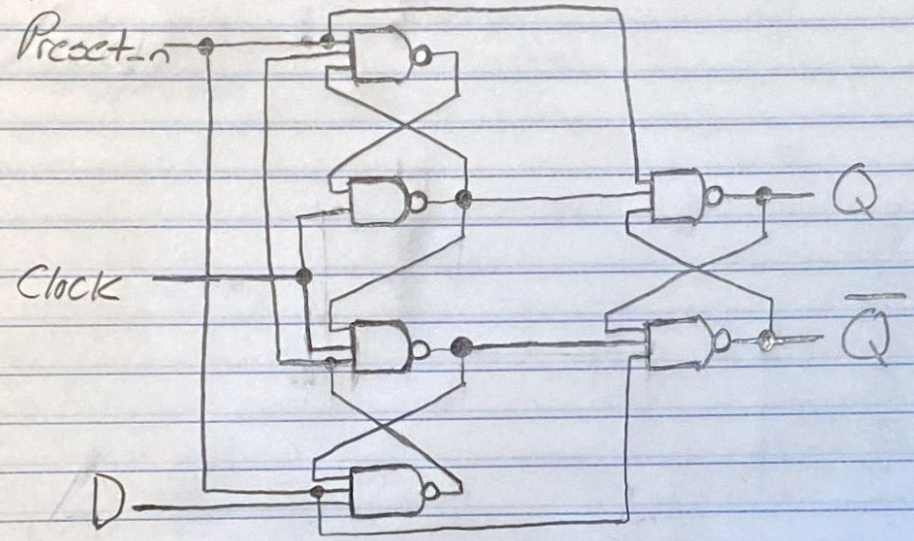
03/26/22 Quiz 7: DrEmdee

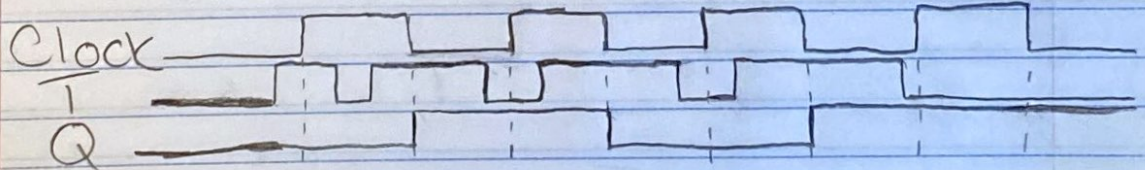
1) Gated D Latch
   - Clk = 1, Q = D
   - Clk = 0, Q remains unchanged



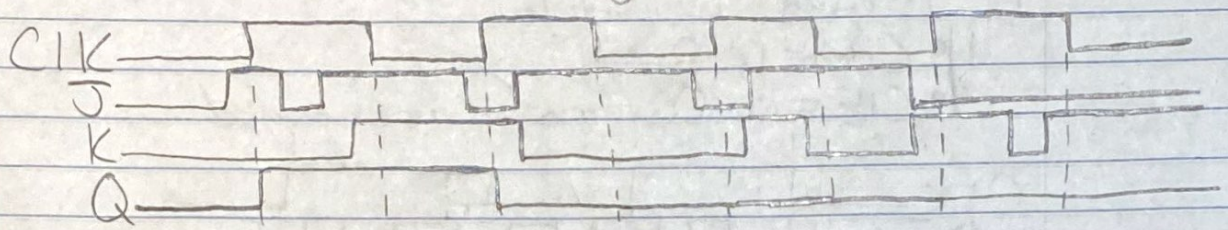
2) This circuit scares me.



3) Negative Edge Triggered T Flip-Flop



4) Positive Edge Triggered JK Flip Flop



- Kind of confused, in lecture the clock oscillated more often than in this example. However, I will follow the timing diagram from the quiz.