Cpr E 281 LAB5
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Lab 5 Answer Sheet

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PRELAB:

Q1. Use Figure 1 and the table below to fill in the truth table on the next page.

X_3	X_2	X_1	X_0	Display
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7

X_3	X_2	X_1	X_0	Display
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	b
1	1	0	0	C
1	1	0	1	d
1	1	1	0	E
1	1	1	1	F

Lab 5 Answer Sheet

X_3	X_2	X_1	X_0	A	B	C	D	E	F	G
0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0	1	0	0
0	1	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0
1	0	1	0	0	0	0	1	0	0	0
1	0	1	1	1	1	0	0	0	0	0
1	1	0	0	0	1	1	0	0	0	1
1	1	0	1	1	0	0	0	0	1	0
1	1	1	0	6	1	1	0	0	0	0
1	1	1	1	0	1	1	1	0	0	0

Q2. Write the verilog code for the 7-Segment Display Decoder based on the truth table from Q1. You only need to write the skeleton code (i.e., a code which shows only a rough outline and no unnecessary or repetitive details) below.

```
module seven_seg_decoder(X0,X1,X2,X3,A,B,C,D,E,F,G);
    input X0,X1,X2,X3;
    output A,B,C,D,E,F,G;
    reg A,B,C,D,E,F,G;

    always @(X0 or X1 or X2 or X3)
    begin
        case({X0,X1,X2,X3})
            4'b0000: A='b0,B='b0,C='b0,D='b0,E='b0,F='b0,G='b1;
            4'b0001: A='b1,B='b0,C='b0,D='b1,E='b1,F='b1,G='b1;
            4'b0010: A='b0,B='b0,C='b1,D='b0,E='b0,F='b1,G='b0;
            4'b0011: A='b0,B='b0,C='b0,D='b0,E='b1,F='b1,G='b0;
            4'b0100: A='b1,B='b0,C='b0,D='b1,E='b1,F='b0,G='b0;
            4'b0101: A='b0,B='b1,C='b0,D='b0,E='b1,F='b0,G='b0;
            4'b0110: A='b0,B='b1,C='b0,D='b0,E='b0,F='b0,G='b0;
            4'b0111: A='b0,B='b0,C='b0,D='b1,E='b1,F='b1,G='b1;
            4'b1000: A='b0,B='b0,C='b0,D='b0,E='b0,F='b0,G='b0;
            4'b1001: A='b0,B='b0,C='b0,D='b0,E='b1,F='b0,G='b0;
            4'b1010: A='b0,B='b0,C='b0,D='b1,E='b0,F='b0,G='b0;
            4'b1011: A='b1,B='b1,C='b0,D='b0,E='b0,F='b0,G='b0;
            4'b1100: A='b0,B='b1,C='b1,D='b0,E='b0,F='b0,G='b1;
            4'b1101: A='b1,B='b0,C='b0,D='b0,E='b0,F='b1,G='b0;
            4'b1110: A='b0,B='b1,C='b1,D='b0,E='b0,F='b0,G='b0;
            4'b1111: A='b0,B='b1,C='b1,D='b1,E='b0,F='b0,G='b0;
        endcase
    end
endmodule
```

TA Initials: _____

LAB:

3.0 Lab5step0 (seven_seg_decoder)
Hardware demonstrates a good circuit. TA Initials: _____

4.0 Lab5step1
Hardware demonstrates a good circuit. TA Initials: _____