Cpr E 281 LAB 09
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Lab 9 Answer Sheet

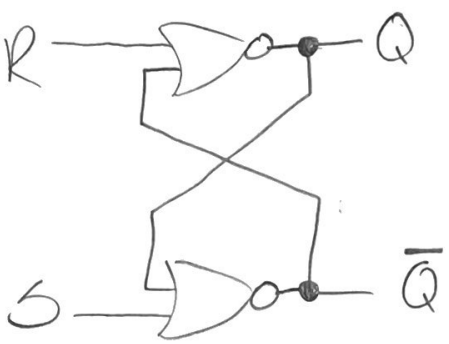
Name and Std No.: [redacted] 053855830 Lab Section: I

Date: 04/04/22

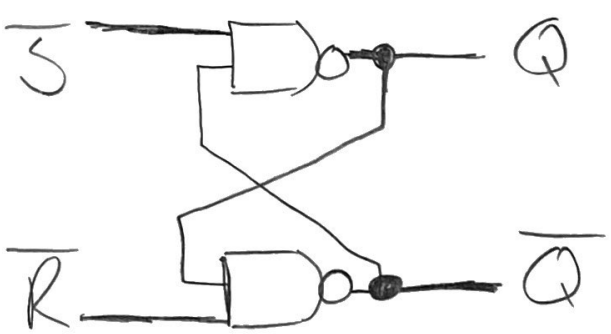
PRELAB:

Refer to Chapter 5 in your textbook and the lab instructions to complete your pre-lab. Please read all the material and complete the circuit diagrams before you come to the lab.

Q1. Draw the circuit diagram for the SR Latch using NOR Gates for **Section 2.0** in the space below.



Q2. Draw the circuit diagram for the $\overline{SR}$ Latch using NAND Gates for **Section 2.0** in the space below.



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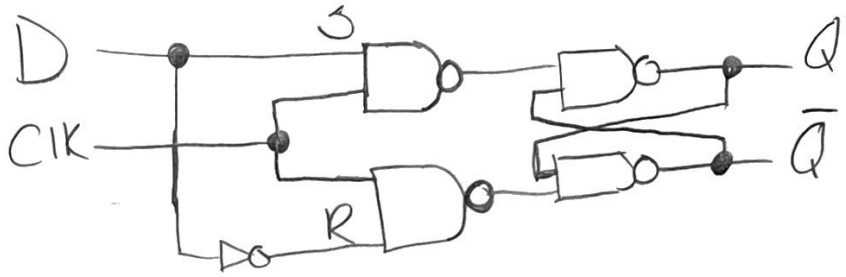
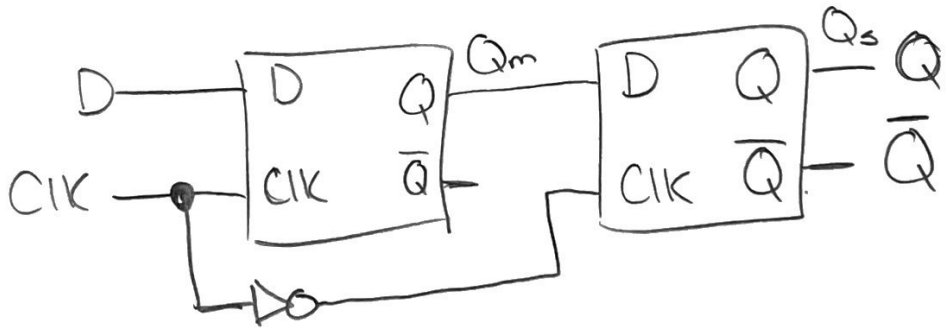
Q3. Draw the circuit diagram for the D Latch using NAND Gates and a NOT gate for **Section 3.0** in the space below.



Q4. Draw the circuit diagram for the D Flip-Flop for **Section 4.0** using the D latches you built in the previous step in the space below. The flip-flop should be triggered by the negative edge of the clock.



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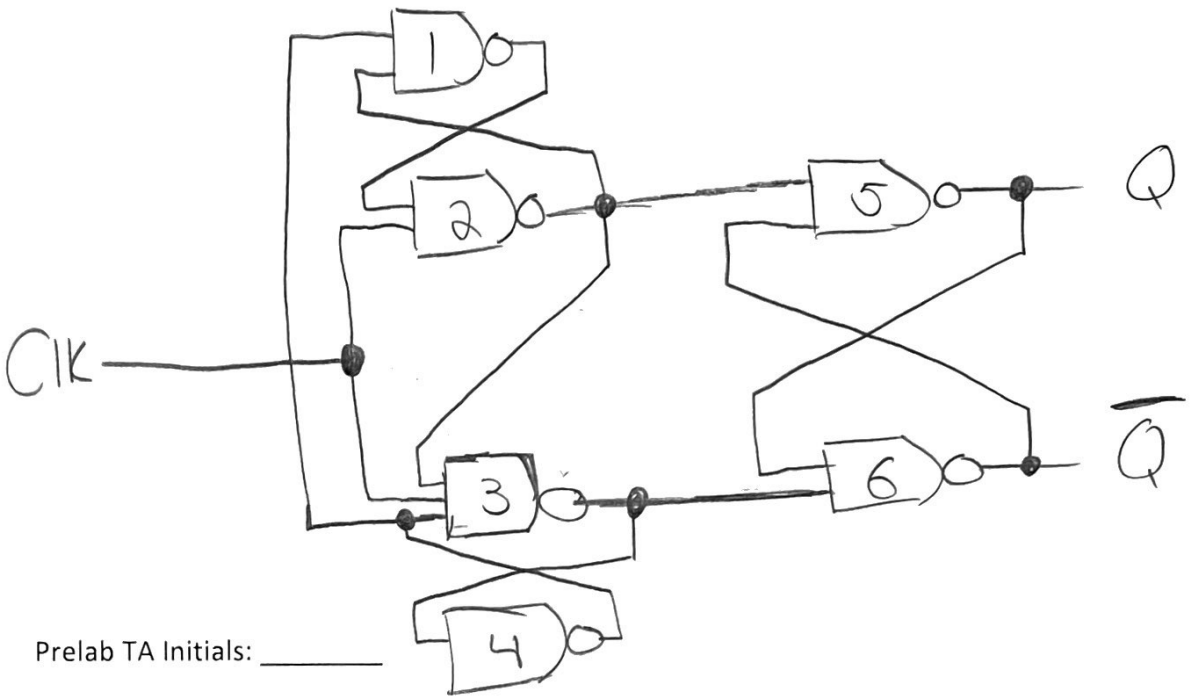
Q5. Draw the circuit diagram for the Positive-Edge-Triggered D Flip-Flop using NAND gates for **Section 4.0** in the space below.



Prelab TA Initials: _____

LAB:

2.0 Complete the characteristic table for both versions of the SR latch. Do both versions function properly as a latch? YES

SR NOR Latch		
S	**R**	**Action**
0	0	*Keep State*
0	1	$Q = 0$
1	0	$Q = 1$
1	1	*Restricted Combination*

$\overline{SR}$ NAND Latch		
S	**R**	**Action**
0	0	Restricted
0	1	$Q = 1$
1	0	$Q = 0$
1	1	Keep State

ModelSim results demonstrate a good circuit. TA Initials: **NOR** M.K.S **NAND** M.K.S

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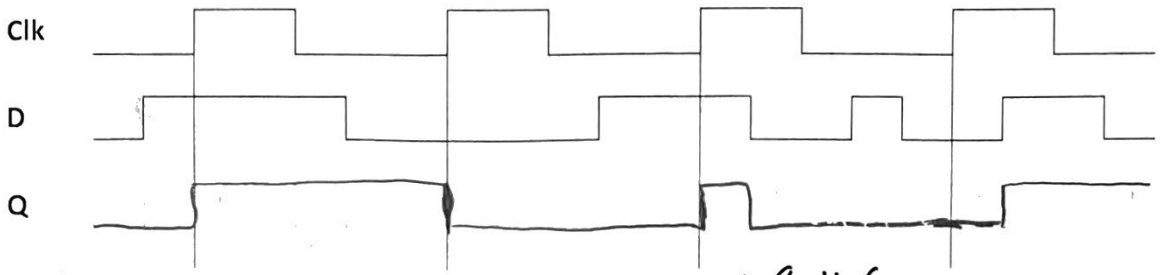
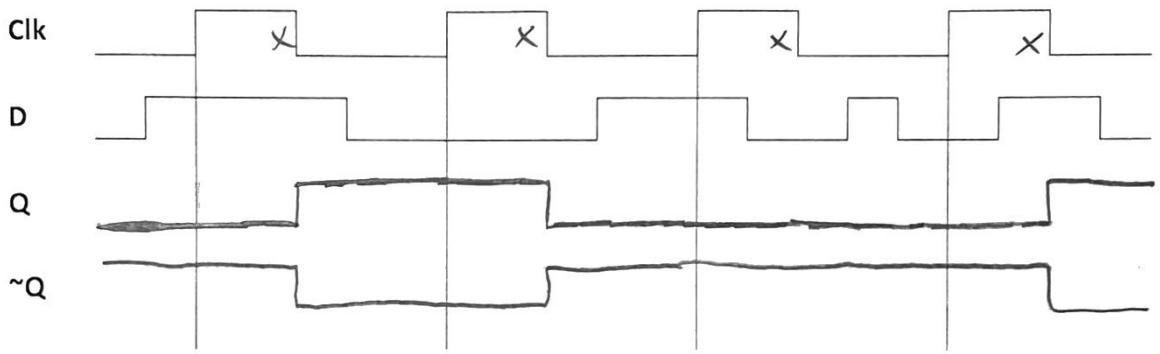
3.0 Complete the timing diagram below for your Gated D Latch.
What is the difference between this gated latch and the previous basic latches?

When CLK=1 Q follows D, otherwise keeps value



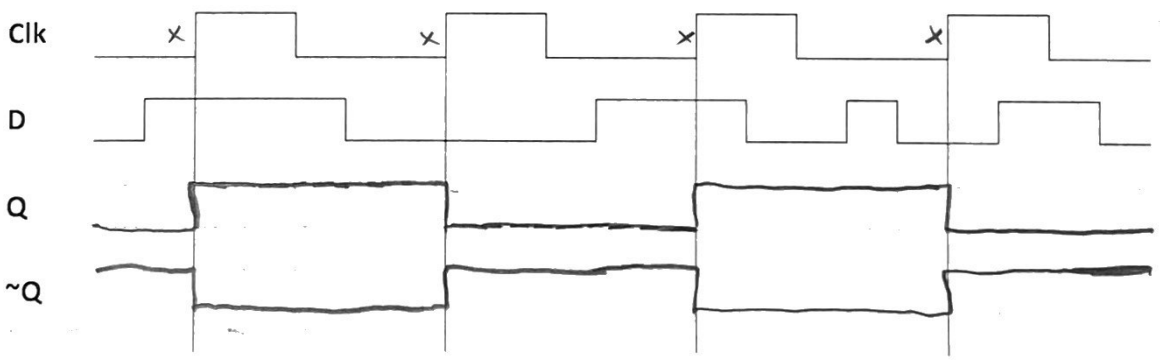
Hardware results demonstrate a good circuit. TA Initials: M.LS

4.0 Complete the timing diagram below for your Negative-Edge-Triggered D Flip-Flop.



Hardware results demonstrate a good circuit. TA Initials: M.LS

Complete the timing diagram below for your Positive-Edge-Triggered D Flip-Flop.



Hardware results demonstrate a good circuit. TA Initials: M.LS