Cpr E 281 LAB10
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Lab 10 Answer Sheet

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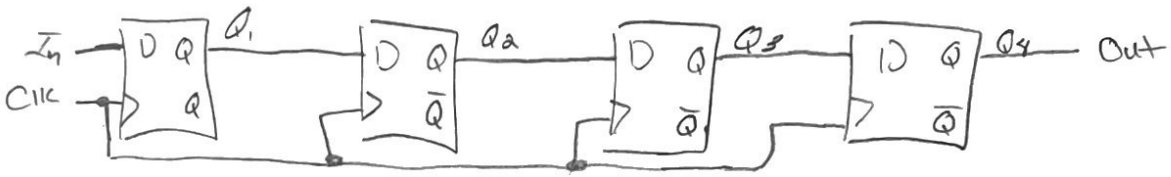
Date: 04/11/22

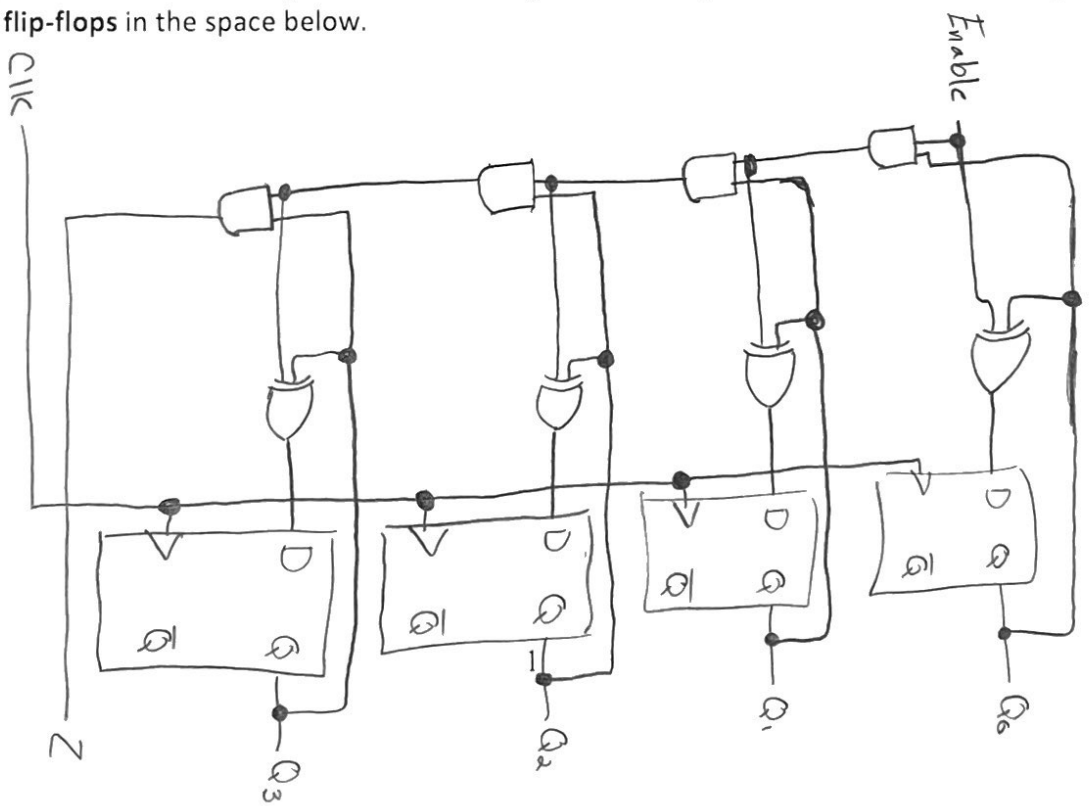
PRELAB:

Refer to Chapter 5 in your textbook and the lab instructions to complete your pre-lab. Please read all the material and complete the circuit diagrams before you come to the lab.

Q1. Draw the circuit diagram for the 4-bit **Shift Register** using D flip-flops in the space below.



Q2. Draw the circuit diagram for the 4-bit **Synchronous Up-Counter with Enable** using **D flip-flops** in the space below.



Cpr E 281 LAB10
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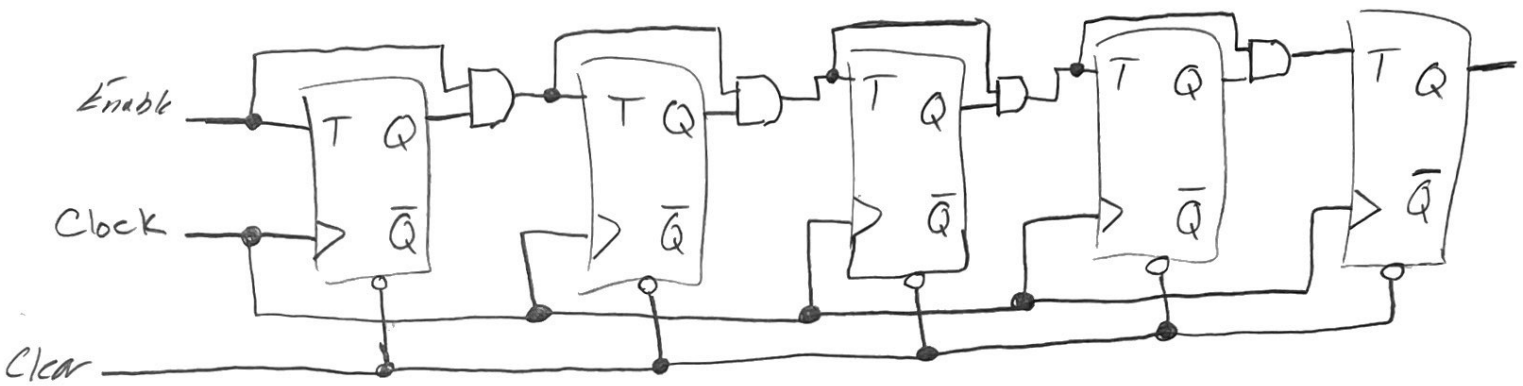
IOWA STATE UNIVERSITY

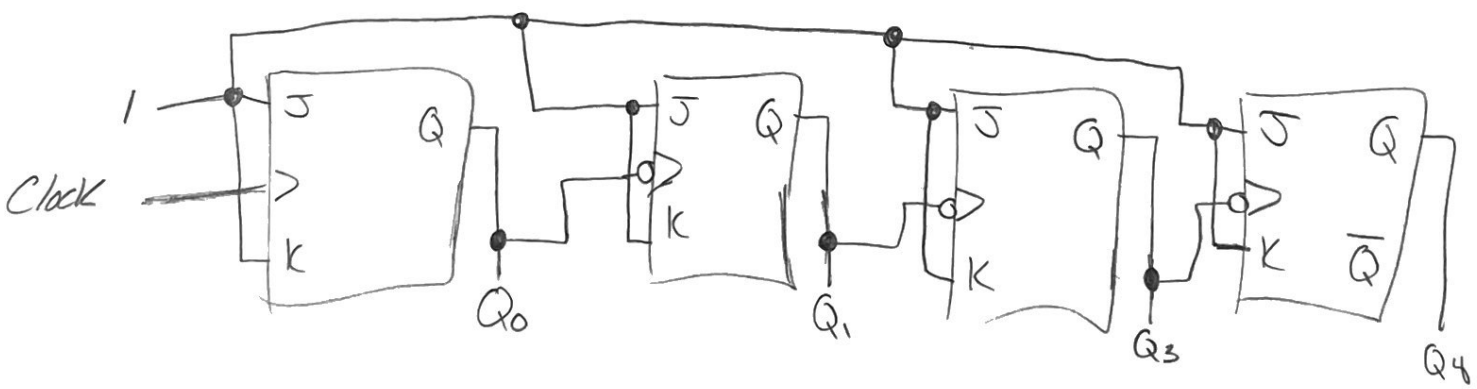
Lab 10 Answer Sheet

* Shall we include clear as well?

Q3. Draw the circuit diagram for a **5-bit** Synchronous Up-Counter with Enable using **T flip-flops** in the space below.



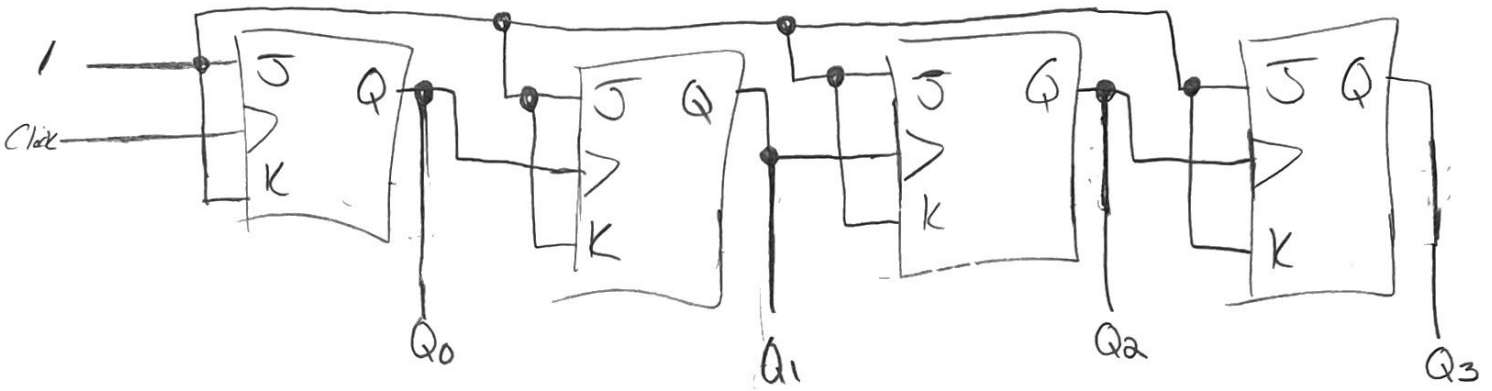
Q4. Draw the circuit diagram for the 4-bit **Asynchronous Up-Counter** using JK flip-flops in the space below.



Cpr E 281 LAB10
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Lab 10 Answer Sheet

Q5. Draw the circuit diagram for the 4-bit **Asynchronous Down-Counter** using JK flip-flops in the space below.



LAB:

2.0 Fill in the sequence table below.

Time	Q1	Q2	Q3	Q4	Set IN
T = 0	n/a	n/a	n/a	n/a	1
T = 1	1	n/a	n/a	n/a	0
T = 2	0	1	n/a	n/a	1
T = 3	1	0	1	n/a	1
T = 4	1	1	0	1	0
T = 5	0	1	1	0	1
T = 6	1	0	1	1	1
T = 7	1	1	0	1	n/a

* tOK about last row

Lab 10 Answer Sheet

ModelSim results demonstrate a good circuit. TA Initials: SB

3.1 ModelSim results demonstrate a good circuit using **DFFs**. TA Initials: MJLC-S

ModelSim results demonstrate a good circuit using **TFFs**. TA Initials: SB

3.2 Seven segment shows 0 to F while counting up. TA Initials: MJLC-S

Seven-segment display shows F to 0 while counting down. TA Initials: SB