CprE 281: Digital Logic
Midterm 2: Friday, Oct 23, 2020

Student Name: _____ Student ID: _____

1. True/False Questions (10 x 1p each = 10p)

(a) In a JK flip-flop, when J=K=0, the output Q(n+1) = Q(n). TRUE / FALSE

(b) In 2's complement notation, $1101_2 < 1110_2$ TRUE / FALSE

(c) A 1-to-64 MUX requires 6 select lines. TRUE / FALSE

(d) A 4-to-16 Decoder has one hot encoded output. TRUE / FALSE

(e) In 2's complement notation: $0011_2 + 1011_2 = 0000_2$ TRUE / FALSE

(f) Any logic function can be implemented with a Decoder and an OR gate. TRUE / FALSE

(g) A gated D-Latch changes its output only when the clock level is 1. TRUE / FALSE

(h) In 2's complement notation, a three-bit number can represent any number from $\mathbf{-8_{10}}$ to $\mathbf{+8_{10}}$. TRUE / FALSE

(i) Any Boolean function can be implemented using only D flip-flops. TRUE / FALSE

(j) A 1-to-4 Demultiplexer can be built with a 2-to-4 Decoder. TRUE / FALSE

2. Logic circuits (20p)

In all sub-problems, draw the complete wiring diagram using logic gates (no-high-level graphical symbols are allowed in this problem). Clearly label all the inputs and outputs.

(a) (5 points) Gated SR Latch (with NOR gates for the latch)

(b) (15 points) Implement a four-bit shift register that provides the parallel access. The control signal Shift/Load is used to select the mode of operation. If Shift/Load = 0, then the circuit operates as a shift register. If Shift/Load = 1, then the parallel input data are loaded into the register. In both cases the action takes place on the positive edge of the clock. Label all the inputs and outputs.

3. Addition/Subtraction (3x5 = 15p)

Assume the following binary numbers are represented in 6-bit 2's complement form. Perform the following operations. In each case, write the carries generated clearly and indicate whether or not overflow occurs. [Note: For subtraction, first convert it into addition.]

(a) 110101 + 001111

(b) 10111 - 100101

(c) 101110 - 110001

4. Number Conversions (4 x 5p each = 20p)

(a) What is the decimal value of the binary number 10011_2 if it is in the following form:

I. Unsigned binary
II. Sign-and-magnitude
III. 1's complement
IV. 2's complement

(b) Convert the following number to IEEE 754 Single Precision Floating Point format: **-24.0**

(c) Convert the following number to IEEE 754 Single Precision Floating Point format: **0.625**

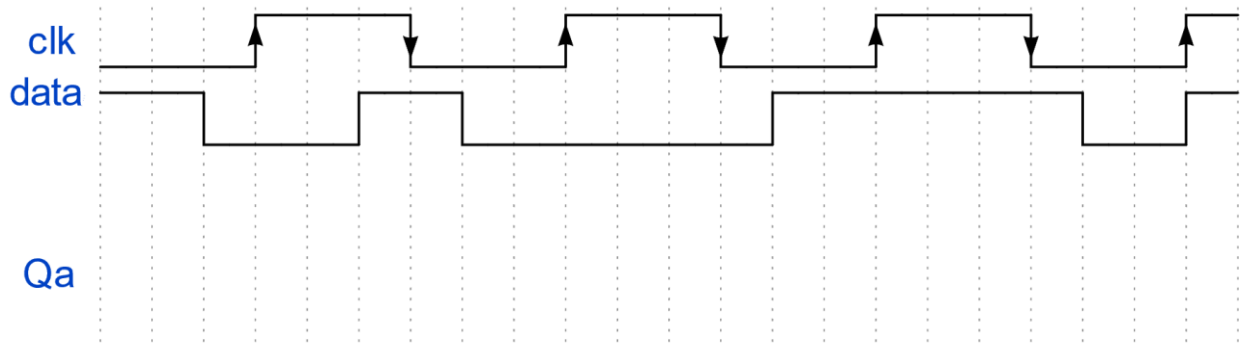
(d) Convert the following number from IEEE 754 Single Precision Floating Point format to 4-bit 2's complement format:

0 0 1 1 1 1 1 1 1 0 1 1 0 0 0 0 0 0 0 00 0 0 0 0 0 0 0 0 0 0 0

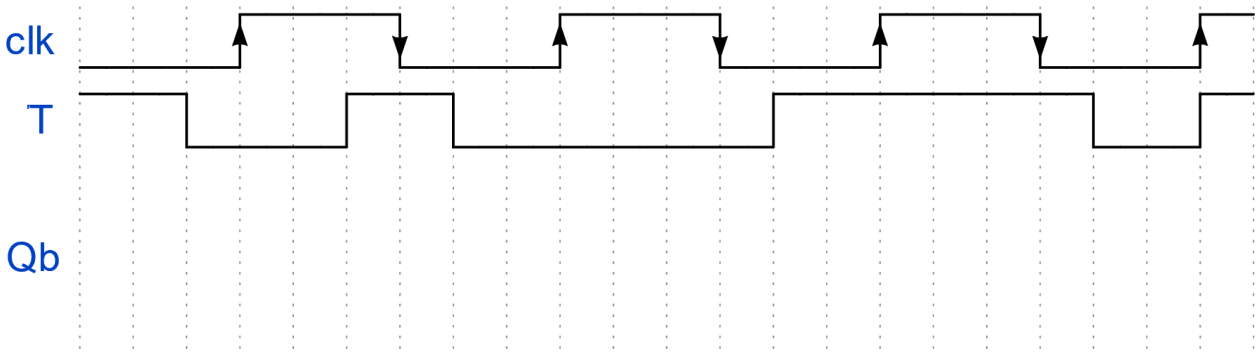
5. Timing Diagrams (3 x 5p each = 15p)

Complete the timing diagram for the specified flip-flops where Qa, Qb, and Qd are the outputs of the D flip-flops, T flip-flops, and JK flip-flops respectively. Assume that the input signal can change only on vertical lines. Ignore the setup time t_{su} and the hold time t_h requirements.

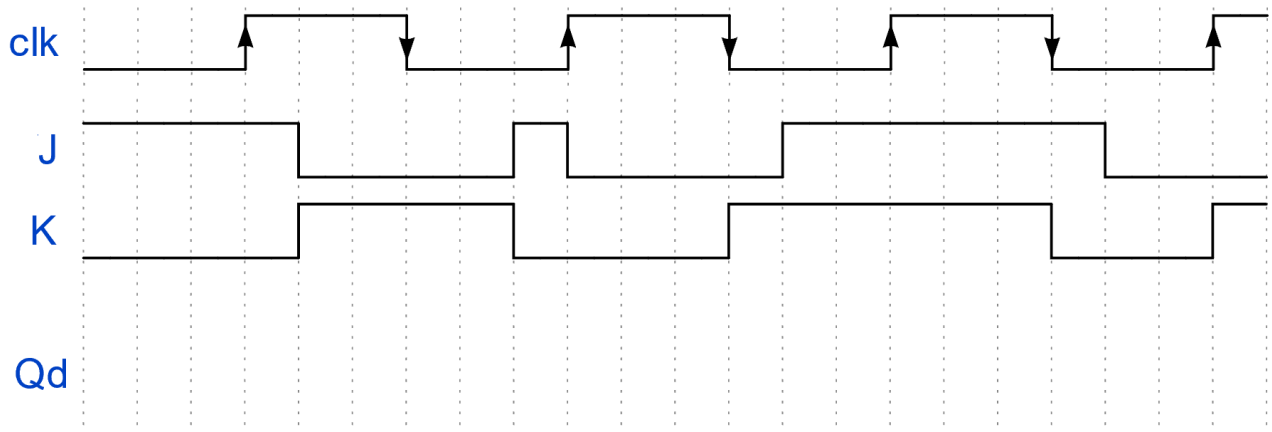
(a) Complete the following timing diagrams for the D input to a Negative edge triggered D flip-flops. Assume the initial value of Q_a is zero



(b) Complete the following timing diagrams for the T input to a positive edge triggered T flip-flops. Assume the initial value of Q_b is zero



(c) Complete the following timing diagrams for the J and K input to a positive edge triggered JK flip-flops. Assume the initial value of Q_d is zero



6. Multiplexers (15p)

For the following logic function, use Shannon's expansion to derive an implementation using **only** 2-to-1 multiplexers, and **no other logic gates**. Assume that the signals A, B, C, and D are available only in their non-inverted form as well as the constants 0 and 1. Clearly label all the inputs, outputs, and pins.

$$\boldsymbol{Z(A,B,C,D) = \overline{B}\overline{C} + \overline{B}\overline{D} + \overline{C}\overline{D} + A\overline{B} + \overline{A}BCD}$$

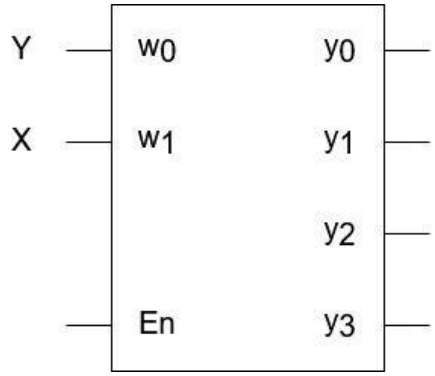
7. Full adder with decoder (4p + 6p = 10p)

(a) Fill out the truth tables for a full-adder and a 2-4 decoder (using X and Y as the decoder inputs).

X	Y	C_{in}	C_{out}	S
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

w_1 (X)	w_0 (Y)	y_3	y_2	y_1	y_0
0	0				
0	1				
1	0				
1	1				

(b) Implement the full-adder using a 2-4 decoder and additional NOT, OR, and AND gates. (Hint: It may help to derive expressions for Cout and S in terms of y_3, y_2, y_1, and y_0). Two inputs are already assigned.



8. More Multiplexers (4p + 6p = 10p)

Consider the following logic function: $\boldsymbol{F = ABC + ABD + A\bar{B}C + A\bar{B}\bar{C}D + BCD}$

(a) Draw the complete truth table

(b) Implement the function **F** using **only** 4-to-1 MUXs and **no other logic gates.**

9. Comparator (7p + 8p = 15p)

Design a logic circuit that accept 4-bit unsigned binary number as an input, and produces output F=1 when the input number is divisible either by 3 only or 7 only, but not both. The logic circuit must produce output F=0 for all other cases. Assume that the input signals are available in non-inverted/inverted forms as well as the constants 0 and 1. Clearly label all inputs, outputs and pins.

(a) Draw and complete the truth table for the logic circuit.

(b) Implement the function using a Decoder and a minimal number of AND, OR, and NOT gates.

Question	Max	Score
1. True/False	10	
2. Logic circuits	20	
3. Addition/Subtraction	15	
4. Number Conversions	20	
5. Timing Diagrams	15	
6. Multiplexers	15	
7. Full-Adder with Decoder	10	
8. More Multiplexer	10	
9. Comparator	15	
TOTAL	**130**	