

# Cpr E 281 MINI PROJECT

ELECTRICAL AND COMPUTER  
ENGINEERING  
IOWA STATE UNIVERSITY

## Mini Project Answer Sheet

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Lab Section: 1

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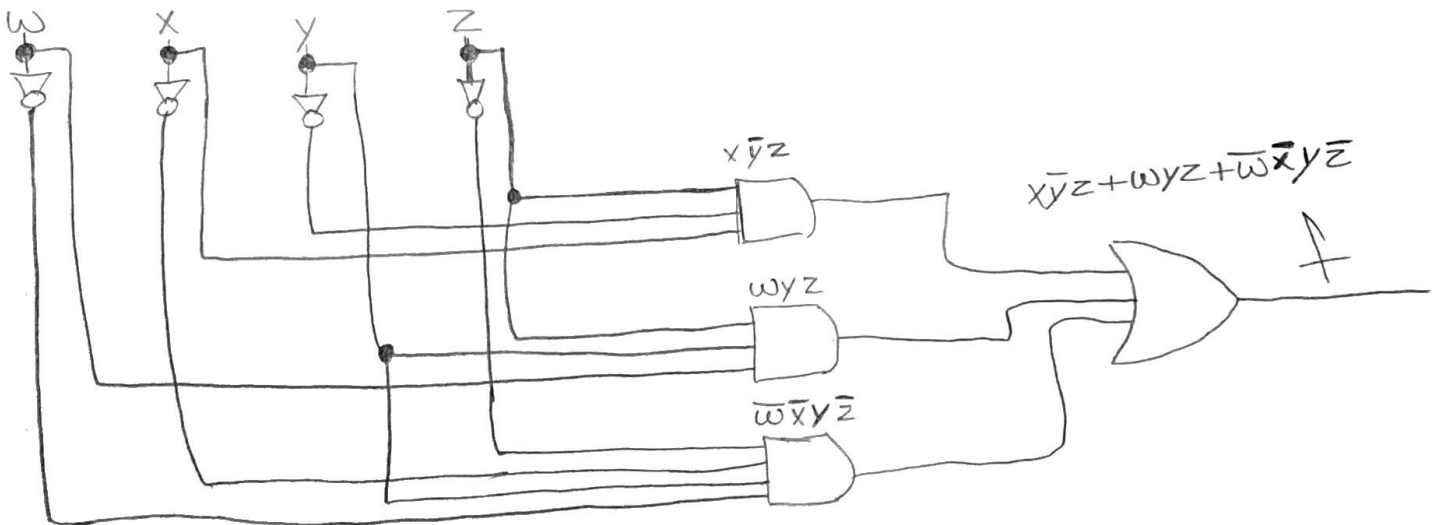
### PRELAB:

Read the Mini-Project lab document and complete as much of this answer sheet as you can before lab.

TA Initials: \_\_\_\_\_

### LAB:

4.0 Draw Uncle Bob's circuit below, using only AND, OR, and NOT gates.  $\text{NAND} \rightarrow \text{SOP}$



● Bob's Circuit =  $\bar{X} Y Z + W Y Z + \bar{W} \bar{X} \bar{Y} Z$

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5.0 Give the shorthand canonical SOP expression for Uncle Bob's circuit and then the Verilog code which implements this behavior:

$$B(W, X, Y, Z) = \underline{X\bar{Y}Z + WYZ + \bar{W}\bar{X}Y\bar{Z}}$$

Verilog: 

```
module mProjStep1(F,W,X,Y,Z);
    input W,X,Y,Z;
    output F;
    assign F = (X & ~Y & Z) | (W & Y & Z) | (~W & ~X & Y & ~Z);
endmodule
```

Demonstration of Quartus Results: \_\_\_\_\_

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6.0 Truth table for Uncle Bob's function B and the 4-bit prime detector function P.

	W	X	Y	Z	B	P
	0	0	0	0	0	0
	0	0	0	1	0	0
! *	0	0	1	0	1	1
*	0	0	1	1	0	1
	0	1	0	0	0	0
! *	0	1	0	1	1	1
	0	1	1	0	0	0
*	0	1	1	1	0	1
	1	0	0	0	0	0
	1	0	0	1	0	0
	1	0	1	0	0	0
! *	1	0	1	1	1	1
	1	1	0	0	0	0
! *	1	1	0	1	1	1
	1	1	1	0	0	0
!	1	1	1	1	1	0

P

wx

yz

	00	01	11	10
00	0	0	0	0
01	0	1	1	0
11	1	1	0	1
10	1	0	0	0

Simplified SOP Expression:

$$P(W, X, Y, Z) = \overline{W} \overline{X} Y + \overline{X} Y Z + \overline{W} X Z + X \overline{Y} Z$$

## Mini Project Answer Sheet

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7.0 Give your implementation of the correct 4-bit prime detector circuit (P) below as either Verilog or a schematic (your choice). Then demonstrate the results:

```
module mProjStep2(F,W,X,Y,Z);  
    input W,X,Y,Z;  
    output F;  
    assign F = (~W & ~X & Y) | (~X & Y & Z) | (~W & X & Z) | (X & ~Y & Z);  
endmodule
```

Demonstration of ModelSim Results: \_\_\_\_\_

**8.0** Design and implement a circuit that uses Uncle Bob's circuit but fixes his mistakes. Draw it below and demonstrate the results:

Demonstration of ModelSim Results: \_\_\_\_\_