Iowa State University **Lab 1 Answer Sheet**

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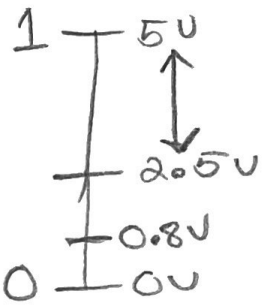


## PRELAB:

**Q1.** Fill in the Truth Table below for an AND gate:

| A | B | C |
|---|---|---|
| 0 | 0 | **0** |
| 0 | 1 | **0** |
| 1 | 0 | **0** |
| 1 | 1 | **1** |

**Q2.** What does the .bdf file extension stand for?

**The .bdf file extensions stands for "Block Design File".**

**Q3.** What is the name of the FPGA on the DE2-115 board?

**The name of the Field Programmable Gate Array, or FPGA, on the DE2-115 board is "Cyclone IV E".**

TA Initials: M.K.S

* what is difference between .qpf & .bdf?

## LAB:

**2.0 Fill in the Truth Table for *lab1step1*:**

| A | B | C |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Iowa State University **Lab 1 Answer Sheet**

Logic Expression: $C = A \cdot B$

Quartus Simulation TA Initials: M.K.S Questa ModelSim TA Initials: M.K.S

**4.0 Fill in the Truth Table for *lab1step2*:**

| W | X | Y | Z |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Logic Expression: $(\bar{w} \cdot x \cdot \bar{y}) + (w \cdot \bar{x} \cdot \bar{y}) + (w \cdot x \cdot y) = z$

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**4.0 Fill in the Truth Table for *lab1step3*:**

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Iowa State University **Lab 1 Answer Sheet**

Logic Expression: $\bar{A} \cdot \bar{B} \cdot C + \bar{A} \cdot B \cdot C + A \cdot \bar{B} \cdot C + A \cdot B \cdot \bar{C} = F$

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