

**Name and Student ID: Devin Amdahl, 053855830    Lab Section: 1**

**Date: 1/19/22**

**PRELAB:**

**Q1.** Fill in the Truth Table below for an AND gate:

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

**Q2.** What does the .bdf file extension stand for?

**The .bdf file extensions stands for “Block Design File”.**

**Q3.** What is the name of the FPGA on the DE2-115 board?

**The name of the Field Programmable Gate Array, or FPGA, on the DE2-115 board is “Cyclone IV E”.**

TA Initials: \_\_\_\_\_

**LAB:**

**2.0 Fill in the Truth Table for *lab1step1*:**

A	B	C
0	0	
0	1	
1	0	
1	1	

Logic Expression: \_\_\_\_\_

Quartus Simulation TA Initials: \_\_\_\_\_ Questa ModelSim TA Initials: \_\_\_\_\_

**4.0 Fill in the Truth Table for *lab1step2*:**

W	X	Y	Z
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Logic Expression: \_\_\_\_\_

TA Initials: \_\_\_\_\_

**4.0 Fill in the Truth Table for *lab1step3*:**

A	B	C	F

**Cpr E 281 LAB1**  
ELECTRICAL AND COMPUTER ENGINEERING

Iowa State University

**Lab 1 Answer Sheet**

Logic Expression: \_\_\_\_\_

TA Initials: \_\_\_\_\_