$Y_0 = w\bar{y}_2\bar{y}_1\bar{y}_0 + w y_2 y_1 \bar{y}_0 + \bar{w} y_2 \bar{y}_1 \bar{y}_0 + \bar{w} y_2 y_1 y_0$

$Y_1 = \bar{w} y_2 \bar{y}_1 y_0 + w \bar{y}_2 y_1 \bar{y}_0 + \bar{w} \bar{y}_2 y_1 y_0 + \bar{w} \bar{y}_2 y_1 \bar{y}_0$

$Y_2 = \bar{w} \bar{y}_2 y_1 y_0 + w y_2 \bar{y}_1 \bar{y}_0 + \bar{w} y_2 \bar{y}_1 \bar{y}_0 + \bar{w} y_2 y_1 y_0$

Cpr E 281 LAB11
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Lab 11 Answer Sheet

Name & Std. No.: Emily 0328583O Lab Section: 1

Date: 04/18/22

PRELAB:

Complete the prelab and make sure you have your designs and circuit diagrams ready before the lab session. You may refer to your text book, Chapter 6.

Q1. Design a simple counting device (Section 2.0).

Number of States: 6
Number of State Variables: 6

State Table:

Present State	Next State		Output
	w=0	w=1	
A	A	B	0
B	B	C	1
C	C	D	2
D	D	E	3
E	E	F	4
F	F	A	5

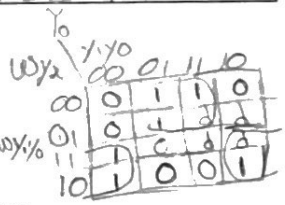
State-Assigned Table:

Present State	Next State		Output
	w=0	w=1	$Z_2 Z_1 Z_0$
000	000	001	000
001	001	010	001
010	010	011	010
011	011	100	011
100	100	101	100
101	101	000	101

NO SPACE FOR CANONICAL SOP EXPRESSIONS

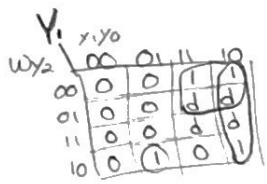
Canonical SOP Expressions for Next State Logic:

$Y_0 = w\bar{y}_0 + \bar{w}y_0 \quad | \quad Y_1 = \bar{w}y_1 + y_1\bar{y}_0 + w\bar{y}_2\bar{y}_1 y_0 \quad | \quad Y_2 = \bar{w}y_2 + y_2\bar{y}_0 + w y_1 y_0$

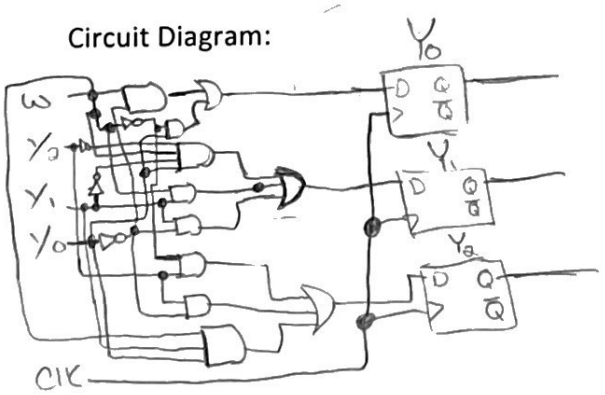


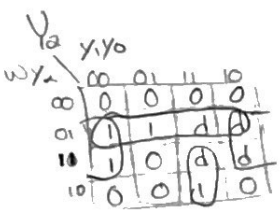
Simplified Next State Logic Expressions and Output Logic Expressions:

$Z_0 = \bar{w}y_0 \quad | \quad Z_1 = \bar{w}y_1 + y_1\bar{y}_0 \quad | \quad Z_2 = \bar{w}y_2 + y_2\bar{y}_0$



Circuit Diagram:





Lab 11 Answer Sheet

Q2. Design a simple counter (Section 3.0).

Number of States: 4
Number of State Variables: 4

State Table:

Present State	Next State		Output
	w=0	w=1	
A	A	B	1
B	B	C	2
C	C	D	5
D	D	A	7

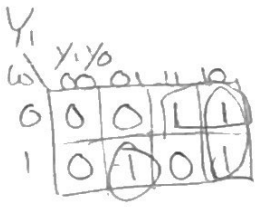
State-Assigned Table:

Present State Y_1Y_0	Next State		Output
	w=0 Y_1Y_0	w=1 Y_1Y_0	
00	00	01	1
01	01	10	2
10	10	11	5
11	11	00	7

Canonical SOP Expressions for Next State Logic:

$Y_1 = w\bar{Y}_1Y_0 + wY_1\bar{Y}_0 + \bar{w}Y_1Y_0 + \bar{w}Y_1\bar{Y}_0$

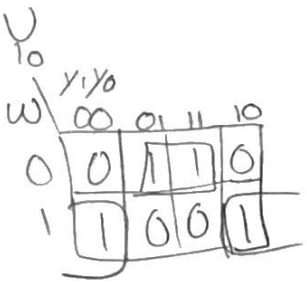
$Y_0 = w\bar{Y}_1\bar{Y}_0 + wY_1\bar{Y}_0 + \bar{w}\bar{Y}_1Y_0 + \bar{w}Y_1Y_0$



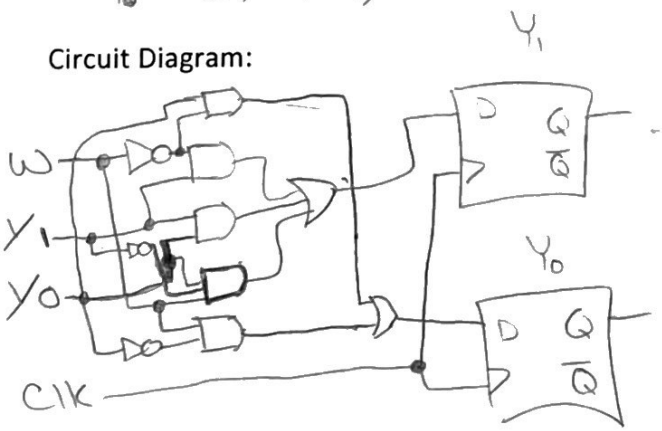
Simplified Logic Expressions:

$Y_1 = \bar{w}Y_1 + Y_1\bar{Y}_0 + w\bar{Y}_1Y_0$

$Y_0 = \bar{w}Y_0 + w\bar{Y}_0$



Circuit Diagram:



Lab 11 Answer Sheet

LAB:

2.0 A Simple Counting Device

How does the **clock_generator** module produce a signal with a period of about 670 milliseconds?

Hardware results demonstrate a functional design: _____

3.0 A Simple Counter

Hardware results demonstrate a functional design: _____

4.0 Switch Debouncing

Hardware results demonstrate a functional design: _____