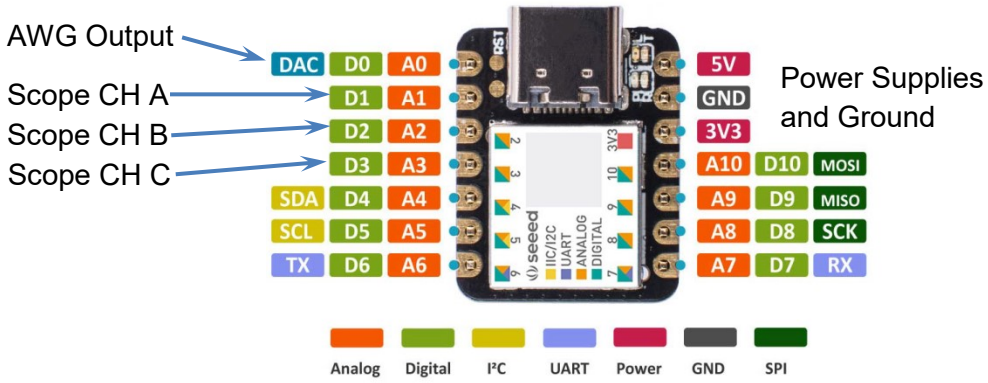
Four Transistor Op-Amp Test Circuit

Objective:

This is a simple transistor Op-Amp test circuit to demonstrate lab testing using the XIAO SAMD21 based measurement module with ALICE Universal in hands on circuits and electronics labs.

The XIAO Based measurement module:



The circuit:

A simple three stage op-amp can be constructed using just four bipolar transistors, 12 resistors and 1 capacitor. The LTspice simulation schematic is shown in figure 1. The differential input stage consists of NPN transistors Q1 and Q2, emitter tail resistor R1 and collector load resistors R2, R3. A resistor degenerated common emitter PNP second stage consists of Q4, R4 and R5. Miller compensation capacitor C1 insures stability and sets the amplifier slew rate. A final emitter follower output stage consists of NPN Q3 and resistor R6.

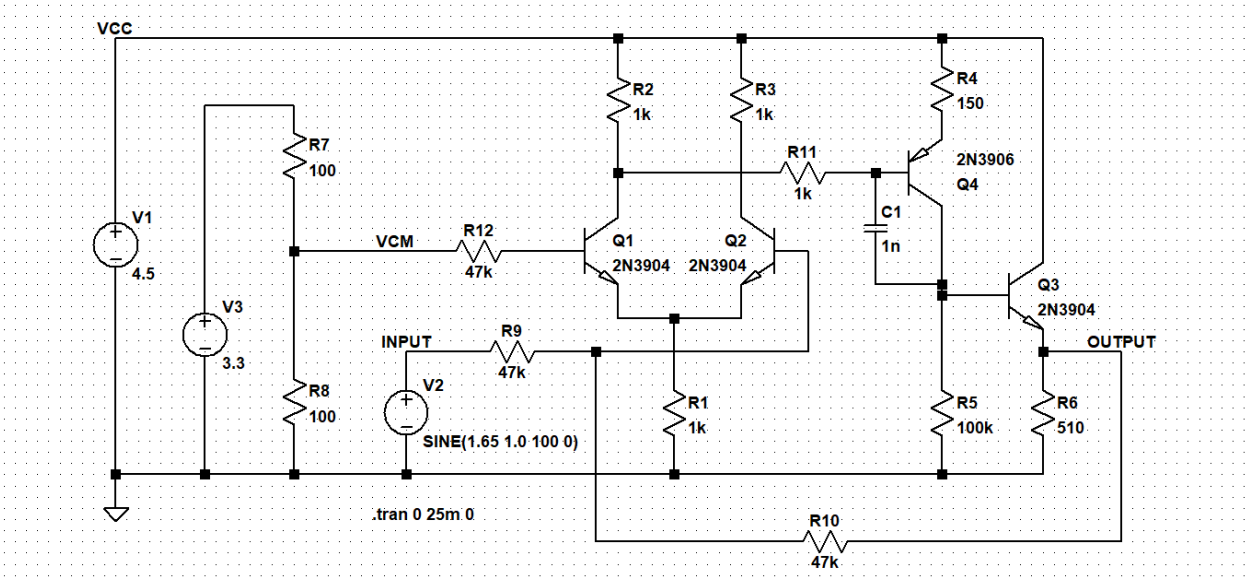


Figure 1, LTspice schematic

A resistor divider across the 3.3V power supply, R7 and R8, generates a 1.65 V common mode voltage VCM at the + input (base of Q1). The amplifier is configured as an inverter with a gain of -1 with feedback resistors R9 and R10 connected to the – input (base of Q2).

LTspice simulation results are shown in figure 2.

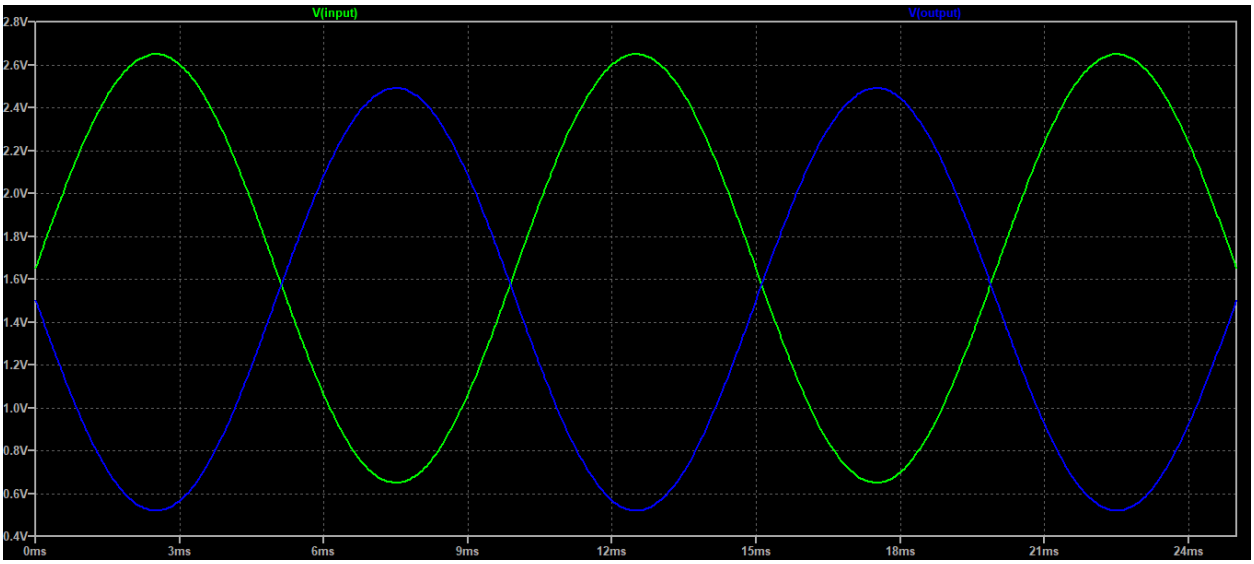


Figure 2, LTspice simulation results

Construction:

The circuit can be constructed on a solderless breadboard alongside the XIAO SAMD21 measurement module as shown in figure 3. The two bottom rails are connected to GND and 3.3V from the module and the top (red) rail is connected to the approximately 4.5 V supplied from the USB port minus 1 diode drop.

The AWG output and the Channel A scope input are tied together and is the input to the amplifier. The Channel B scope input measures the amplifier output.

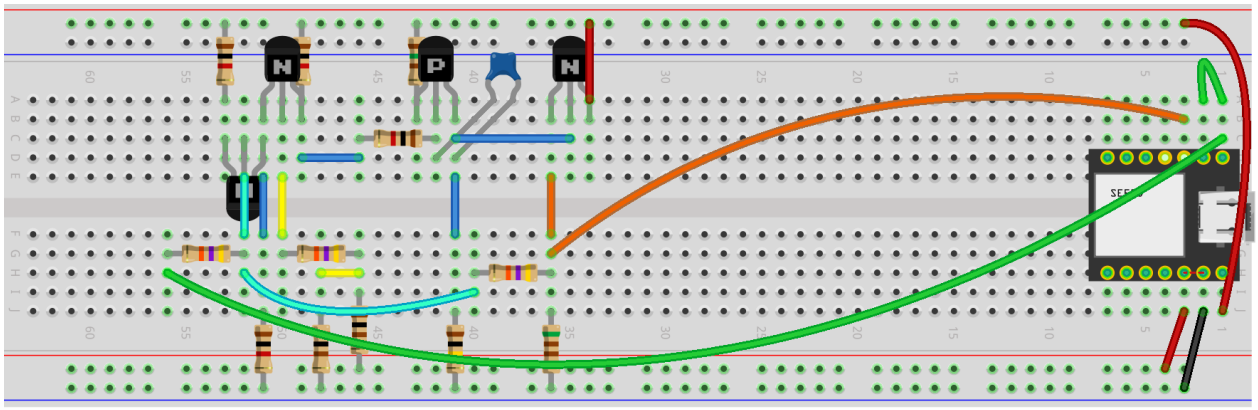


Figure 3, Solderless Breadboard Layout

Care should be taken to insure that the Scope inputs are never connected to voltages greater than 3.3 V such as the 4.5 V rail used here to power the circuit. The Scope inputs can be made

“5V Tolerant” by inserting a resistor of at least 5kΩ (4.7kΩ or 5.1kΩ) between the XIAO module pin and the circuit node being measured. The added series resistance will have a negligible effect owing to the very high impedance of the ADC inputs but limit the current to a safe level.

The amplifier output should never exceed the 3.3 V maximum output of the AWG when configured as in this example. Increasing the gain by changing the feedback resistors could cause the output to exceed 3.3 V.

Measurement Results:

The ALICE user interface is used in conjunction with the module to drive and measure the test circuit. The screen shot in figure 4 shows similar results to the LTspice simulation.

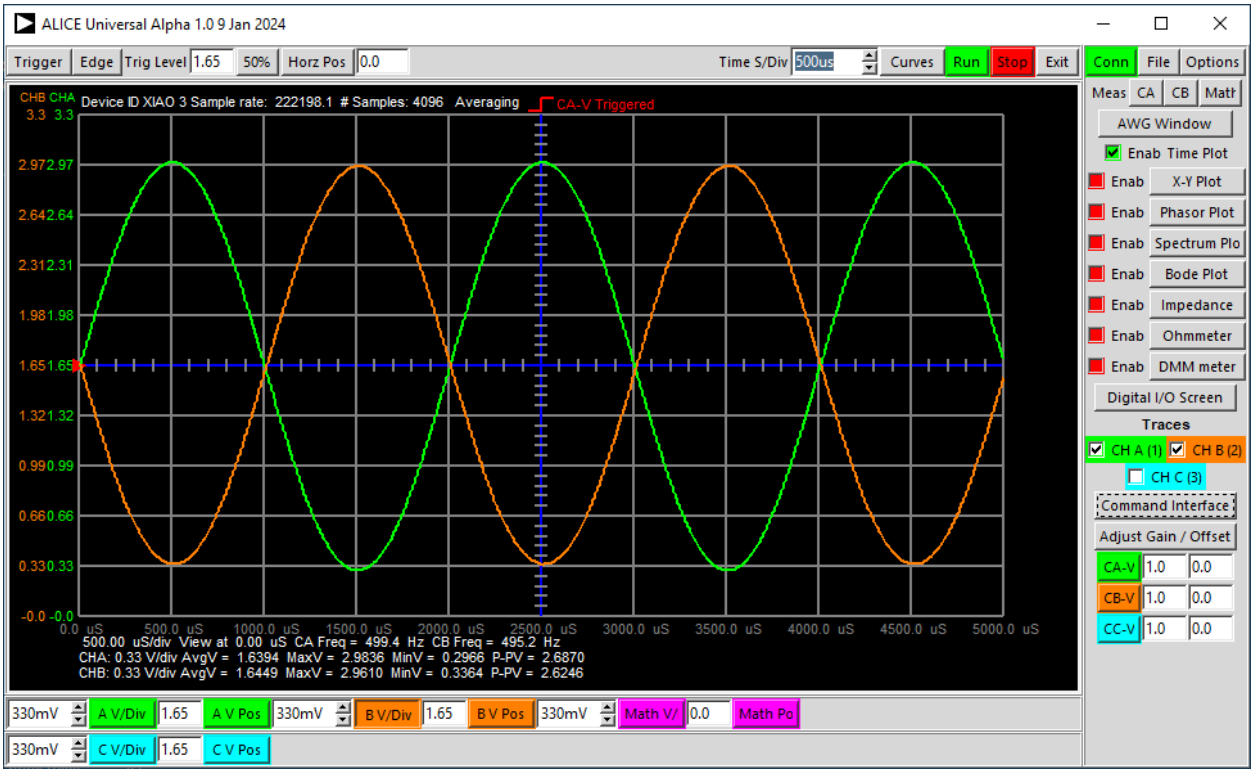


Figure 4, ALICE Scope screen.

If we increase the value of the compensation capacitor C1 to 10 nF and switch the AWG waveform shape to a square wave we can measure the resulting slew rate. We can also turn on and connect scope Channel C to the summing junction at the – input of the amplifier to view the input voltage difference seen when the amplifier is slewing as shown in figure 5.

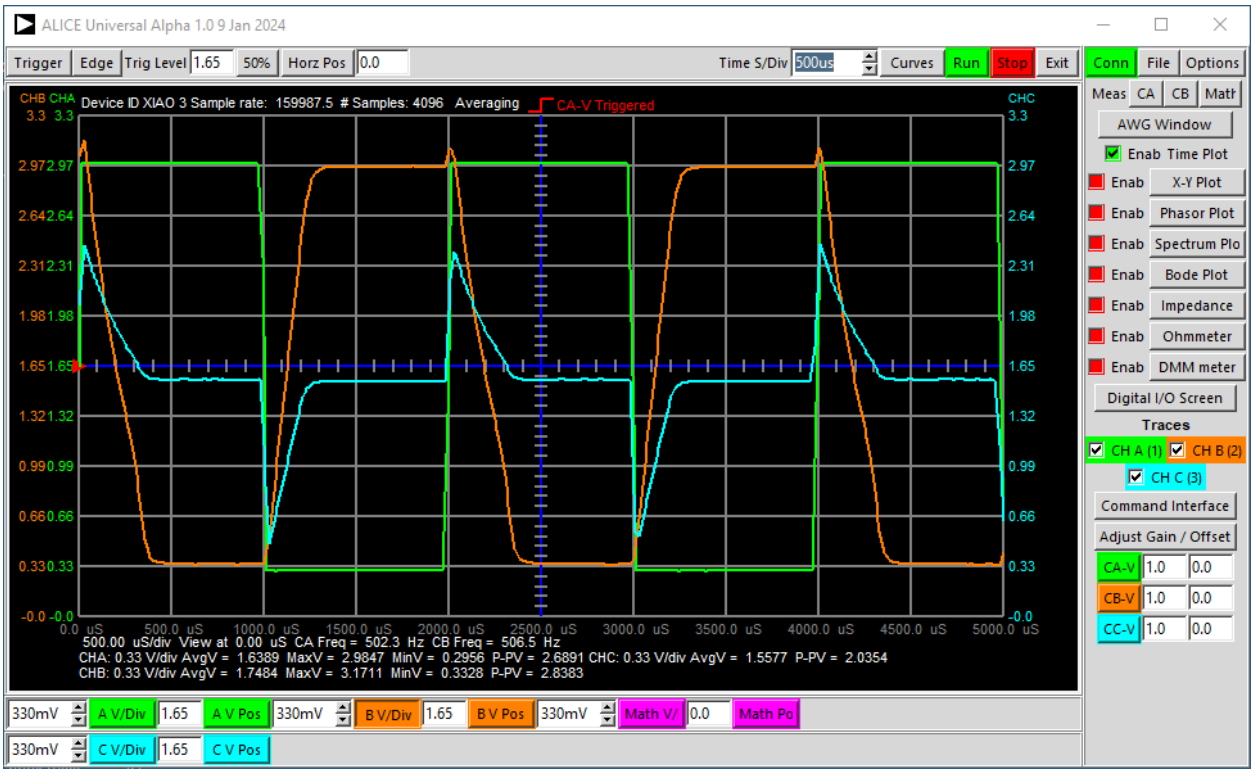


Figure 5, Slew rate test.