# Seeed Studio XIAO SAMD21 as an introductory personal instrument.

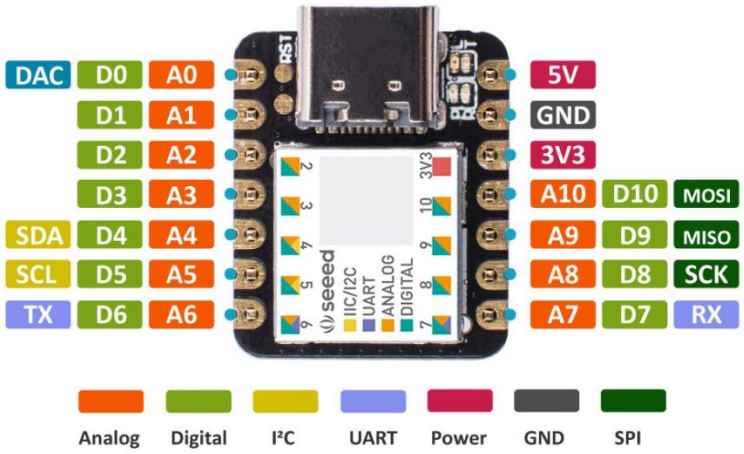
## Objective:

To demonstrate the use of the Seeed Studio XIAO SAMD21 micro-controller board as a personal lab data measurement system in introductory level circuits (and electronics) courses.

## Hardware:

Seeed Studio XIAO SAMD21 micro-controller board. Cost $5.40 (Digi-Key Part Number 1597-102010328-ND)

The XIAO board is a small 14 pin DIP like module. By installing male pin headers it can be easily inserted into a solderless breadboard and effectively becomes just another “part” in the experimental setup.




XIAO pinout

The XIAO contains one 12 bit ADC which can be multiplexed to multiple pins. It also contains one 10 bit DAC available on pin A0. The overall maximum ADC sample rate (50 KSPS) will be shared by the scope input channels and the per channel sample rate will depend on the number of analog input pins being measured. The XIAO can also generate a PWM digital output on pin D10. This PWM output can also be modulated and low pass filtered to provide a pseudo second AWG output channel (B). Using the PWM output as a second AWG output will cut the analog DAC sample rate essentially in half.

The remaining 6 digital input pins (D4 – D9) can optionally be sampled along with the analog inputs to provide a kind of “mixed signal” scope display.

None of the XIAO pins are 5 V tolerant and will likely be damaged if voltages beyond 0 and 3.3V are applied. The XIAO SAMD21 is a 3.3 volts device and applying 5 volts to an input will overload and damage the XIAO. There may be a 5-volt power connection on the board, but DO NOT use it to power experiments unless you are certain of the voltages of any nodes you might be measuring with one of the input pins. Absolute Maximum Pin voltage with respect to GND - GND-0.6V and VDD - VDD+0.6V.

USB C to USB A cable.
Solderless breadboard.
Various components, resistors, capacitors, diodes …

## Board Firmware:

Developed using the Arduino IDE.

Download the Arduino IDE from here: https://www.arduino.cc/en/software

Seeed Studio Getting Started web page (contains info on configuring Arduino IDE for XIAO): https://wiki.seeedstudio.com/Seeeduino-XIAO/

How to Add Seeed boards to Arduino IDE: (from https://wiki.seeedstudio.com/Seeed_Arduino_Boards/)

Open the Arduino IDE, click on File > Preferences, and copy the below url to the Additional Boards Manager URLs list:

https://files.seeedstudio.com/arduino/package_seeeduino_boards_index.json

Click on Tools > Board > Board Manager. Now search the board by name, “Seeeduino XIAO”

Click on Tools > Ports and select the correct COM port for the board.

Open the Source file: XIAO_Scope_pwm_awg.ino

Click on the Upload arrow button.

## PC Host Software:

ALICE Universal, PC Host User Interface developed using Python 3.10 and XIAO hardware specific interface code also developed using Python 3.10 (PySerial library required). Source code and configuration files:

Alice-universal-alpha.pyw
alice_init.ini
XIAO_3a_1w_6d_Interface_Level.py

## Demonstration Lab Examples:

The test circuit schematic shown in figure 1 and breadboard layout shown in figure 2 is used to illustrate how the micro-controller hardware is connected to a simple R-C low pass circuit. The R-C test circuit consists of R1 and C1. The “grounded” end of C1 is connected to a resistor divider (R2 and R3) between GND (black wire) and the 3.3V power supply (red wire).

The voltage at the divider will be 3.3V / 2 or about 1.65 V. The equivalent resistance seen at the divider node will be 100Ω / 2 or about 50Ω.

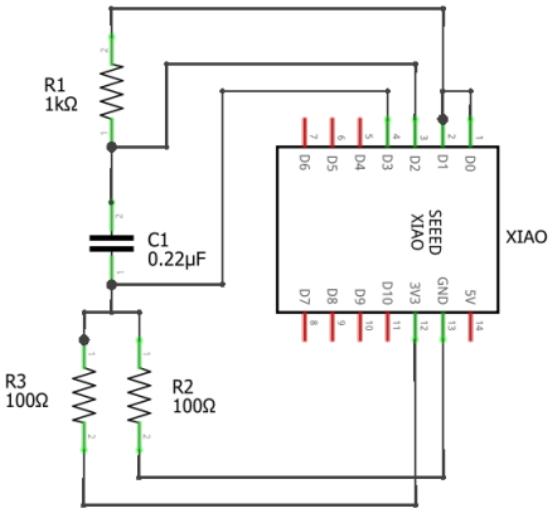



Figure 1, Simple R-C test circuit.

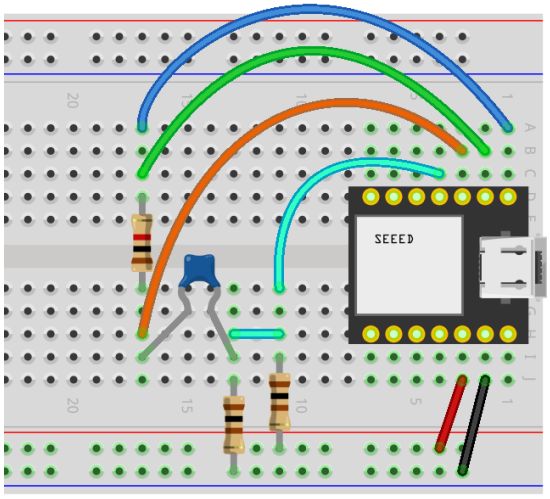



Figure 2, R-C Solderless Breadboard layout.

The A0 pin on the XIAO is the DAC output which provides the AWG (A) function generator output. The A1, A2 and A3 pins on the XIAO are used for the three Scope input channels (CH A, CH B and CH C respectively).

Figure 3 shows the waveform traces as displayed in ALICE. The AWG output is set to generate a 2.8 V p-p sine wave at 300 Hz. The green trace is the green wire in figure 2, the orange trace is the orange wire and the cyan trace is the cyan wire. The p-p voltage seen at the resistor divider junction divided by the 50Ω equivalent resistance is the current in capacitor C1 (about 1.1mA p-p in this example).

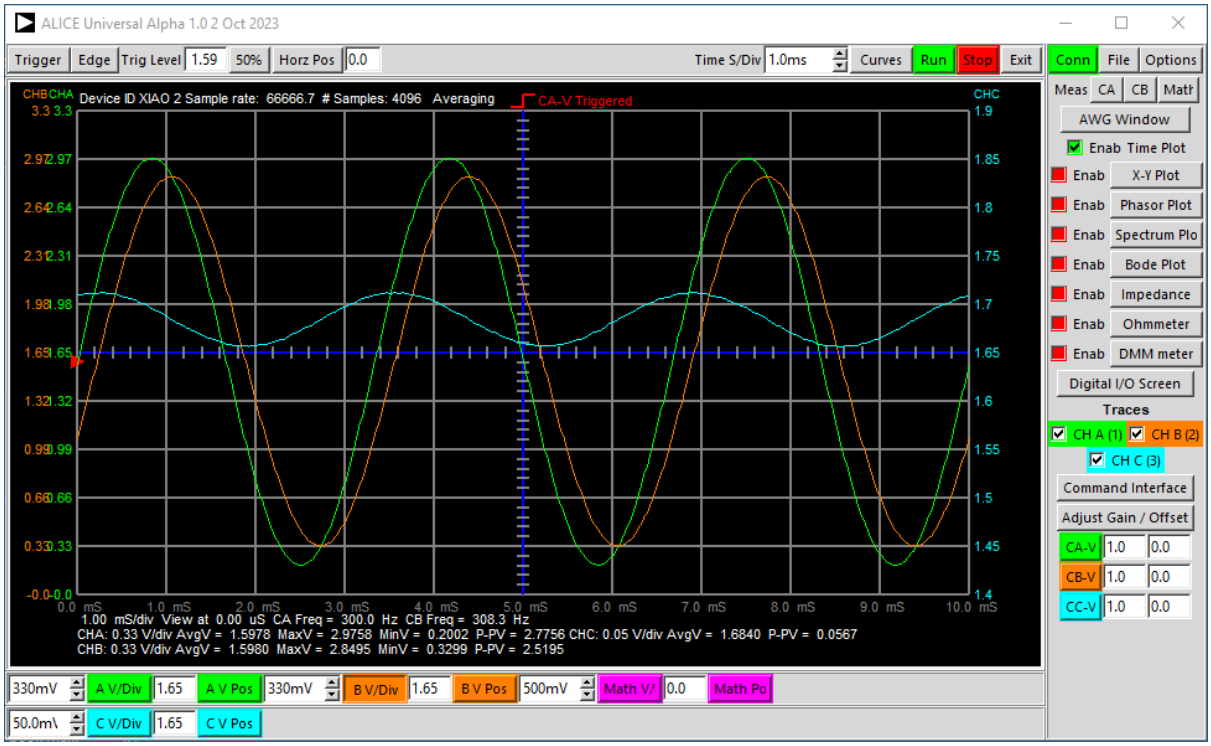



Figure 3, R-C test User interface screen shot.

Using essentially the same breadboard circuit as in Figure 2 we can plot the I/V curve of a diode. We replace C1 with diode D1 (1N914 or similar) and change the value of R1 to 150Ω, as in figures 4 and 5. The DAC output is set to generate a 122 Hz triangle waveform that swings the maximum voltage from nearly 0 to 3.2 V. Again we reference the "negative" end of the diode to the ½ supply divider to apply positive and negative voltages across the diode.

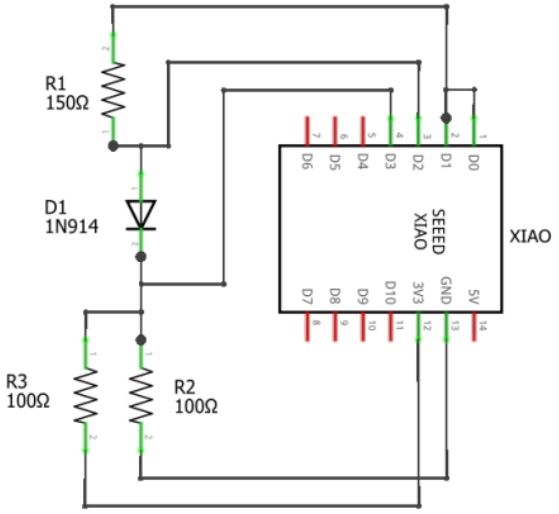



Figure 4, Diode I/V test circuit.

We can use the X,Y plotting tool in ALICE to calculate the current in the diode and plot it vs the voltage across the diode as shown in the figure 6 X,Y window screen shot. The vertical Y axis is scaled in mA. The horizontal axis has been shifted to be centered on 0 V across the diode.

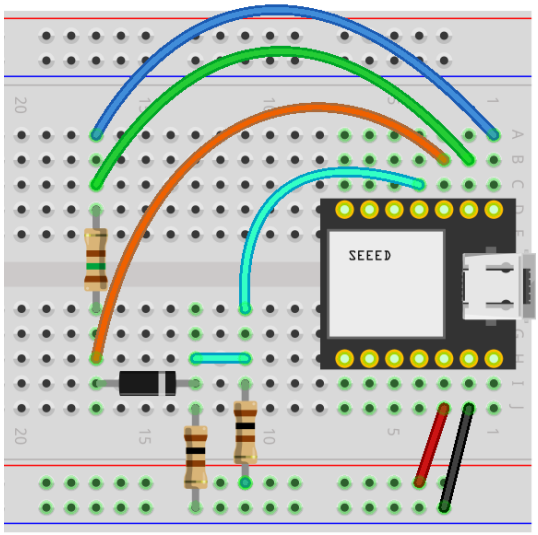



Figure 5, Diode I/V breadboard layout.

We use the Math controls in ALICE to calculate the diode current with the following formula for the Math-X trace:

(VBuffA-VBuffB)*6.6667

Where VBuffA is the voltage on the top of R1 and VBuffB is the voltage on the bottom of R1. We get the voltage across R1 by subtracting the two voltages. The current in mA is scaled by multiplying the difference voltage by 1000/150Ω or 6.6667.

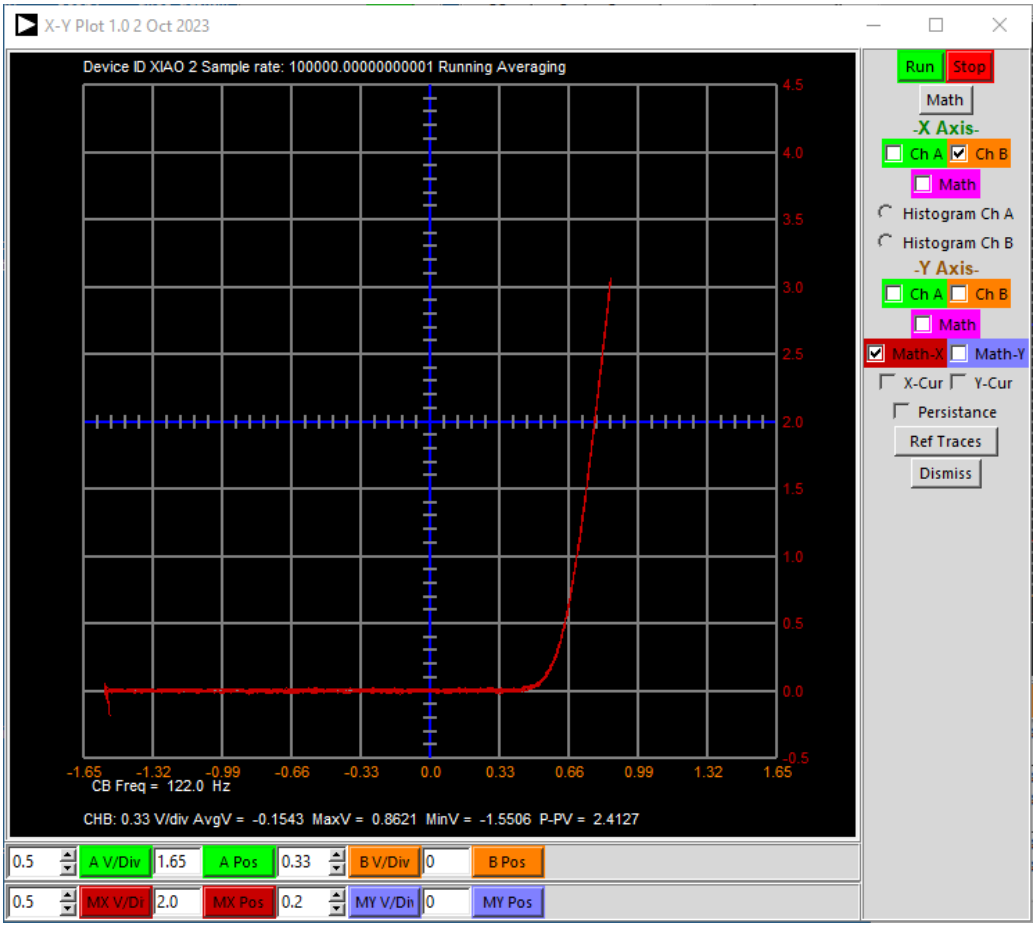



Figure 6, Diode I/V plot.

As a third example test circuit we have an inverting and non-inverting gain of 1 NPN amplifier (the so called “phase splitter”) shown in figure 7. The circuit consists of one NPN transistor (2N3904 or similar) and two 1kΩ resistors. R1 is the collector load resistor and R2 is the emitter resistor. The amplifier input signal from the AWG generator is connected to the base of the transistor. The gain from base to emitter (non-inverting) is +1 as the transistor is acting as an emitter follower. Since R1 and R2 are equal the (inverting) gain from base to collector is -1.

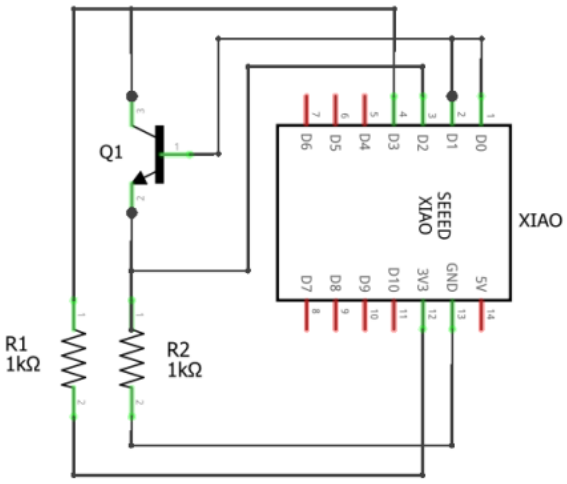



Figure 7, NPN Amplifier schematic

In the breadboard layout shown in figure 8, the AWG output is connected to the base of the transistor (blue wire) and the waveform Shape is a sine wave at 400 Hz. The Min and Max voltage values are adjusted such that neither of the output signals, at the collector or at the emitter, are clipped. We can use the three scope input channels to monitor the input signal at the base (CH A green wire) and the two output signals at the emitter (orange wire) and at the collector (cyan wire) as shown.

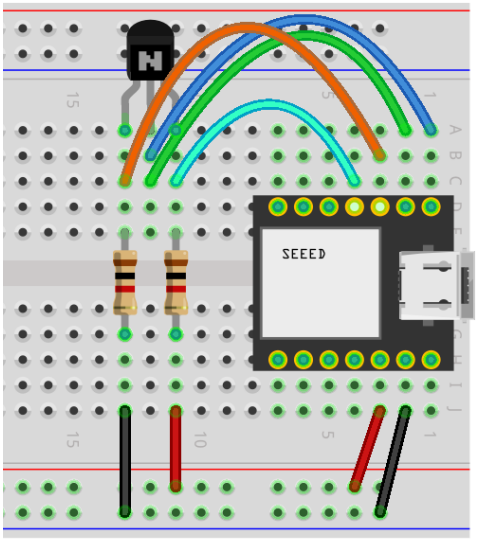



Figure 8, NPN Amplifier breadboard layout.

In figure 9 we see the three scope traces. There is a DC level shift from the input to the respective outputs but the p-p amplitude is nearly the same at gains of +1 to the emitter (orange trace) and -1 to the collector (cyan trace).

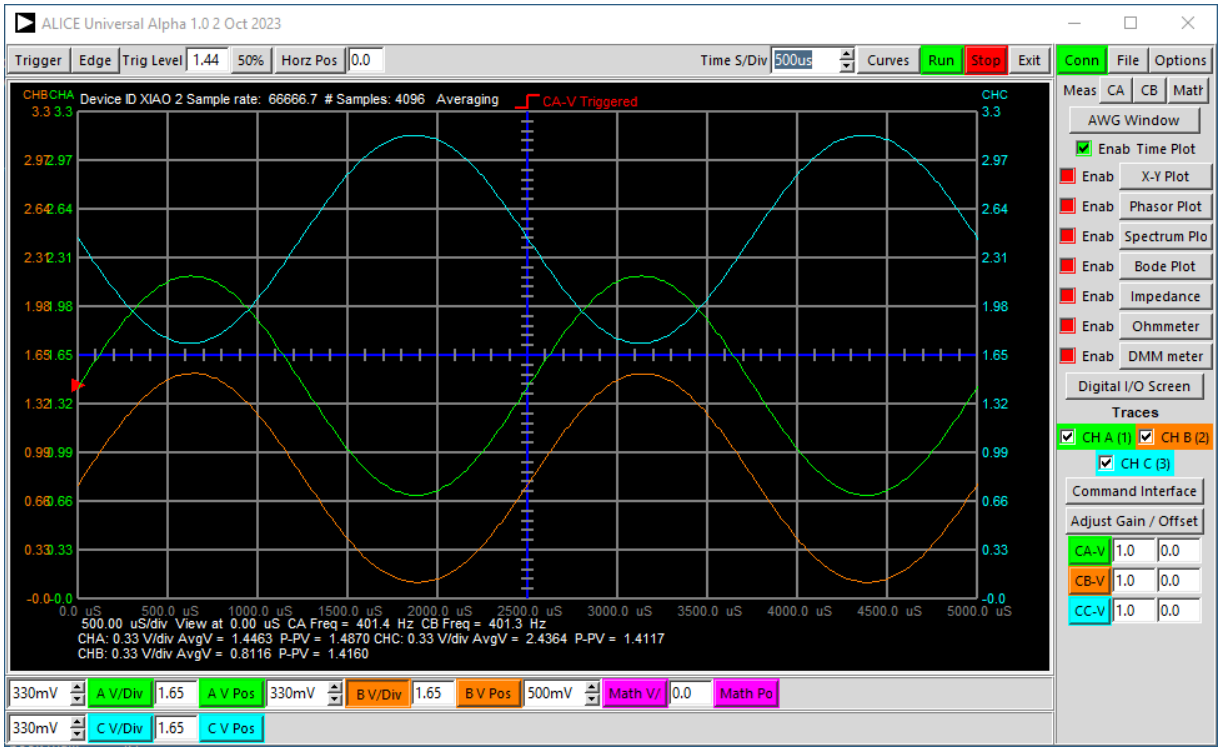



Figure 9, NPN Amplifier Scope traces.

**PWM Output as Second AWG Channel:**

The PWM digital output on pin D10 can be modulated with analog waveform samples to generate a second AWG output channel. The PWM switching frequency is set at 64 KHz which is well above the scope sampling frequency and beyond the input bandwidth and cannot be directly viewed using the scope input.

The PWM signal of course needs to be low pass filtered to reconstruct the analog waveform. A simple R-C filter as shown in figure 10 is sufficient for low frequency waveforms. In the example schematic the analog DAC output AWG (on pin A0) is measured using Scope CH A (on pin A1) for reference purposes. The D10 output is filtered by R1, 1.5kΩ, and C1, 0.22µF. The filtered output is measured by Scope CH B (on pin A2).

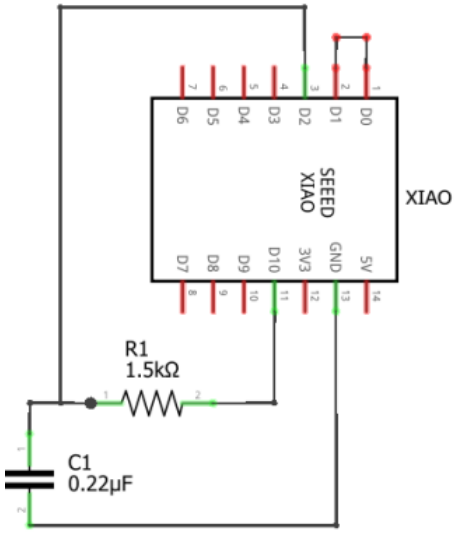



Figure 10, R-C low pass filtered PWM output AWG channel.

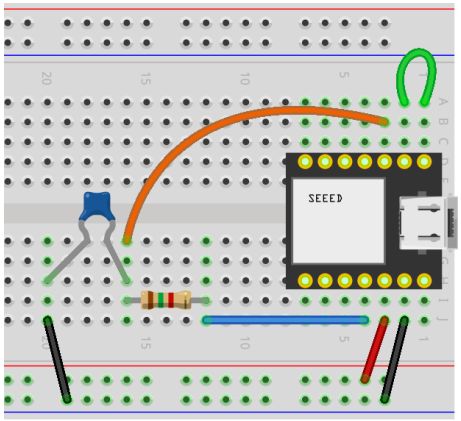


Figure 11, PWM output AWG channel breadboard layout.

For comparison purposes the analog DAC output AWG is displayed on Scope CH A (green trace) and the filtered PWM AWG output is displayed on CH B (orange trace), figure 12. Both are generating a 150 Hz sine wave. The Min and Max values of the PWM channel were adjusted to approximately match the AWG A output amplitude and offset. The digital output is

not going to produce an exact 0 to 3.3 V swing. The R-C filter time constant introduces a phase delay in channel B but that could be corrected for by introducing an appropriate phase shift in the AWG waveform data samples.

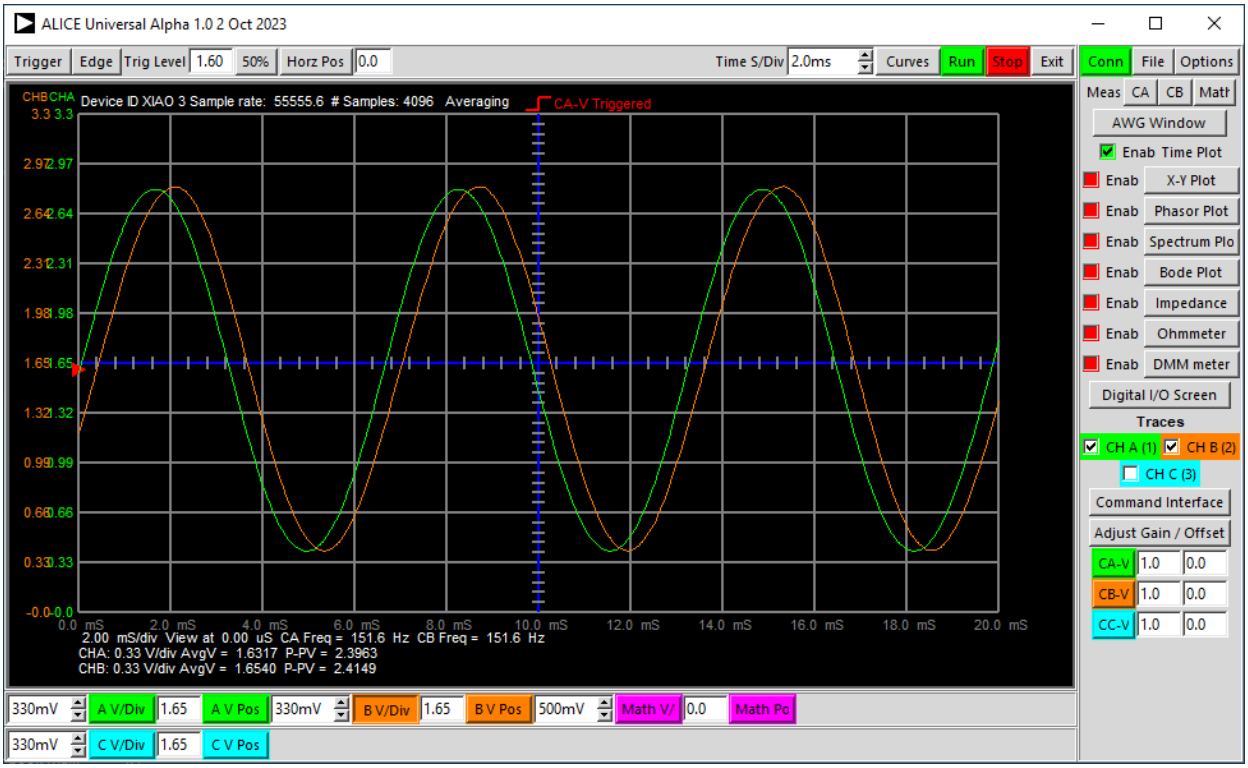



Figure 12, R-C low pass filtered PWM output AWG waveform.

Note that modulating the PWM output takes considerable extra CPU cycles and thus the ADC (Scope) sample rate, even for just two scope channels, is significantly reduced.

### Input Dividers for voltages greater than 0 to 3.3V:

The relatively high input impedance (measured as ~2MegΩ) of the XIAO allows the use of relatively simple resistive input dividers. Example dividers are shown in figure 13. The 220kΩ and 2 100kΩ parallel resistors combine to make an input scale factor of ~5.5:1 with an offset that centers the allowed peak to peak input swing of 5.5 X 3.3 V ~ 18 V on 1.65 V (-16.35 to 19.65). The input resistance will be 220kΩ + 50kΩ or 270kΩ. The relatively high 220kΩ value of the input resistor inherently limits the current that might flow into the XIAO input pin during over voltage conditions.

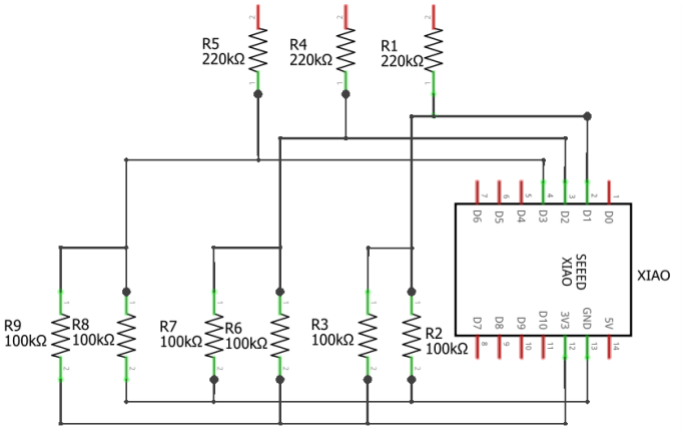



Figure 13, Input resistor voltage divider example

Other resistor values and combinations are of course possible but it is best to keep the effective resistance seen at the XIAO input pins no greater than 50k to 100k.

ALICE provides an input resistor divider calculator tool as shown in figure 14. The resistor value to enter for R1 in the above example is of course the 220k. The resistor value to enter for R2 is the parallel combination of the two 100kΩ resistors or 50kΩ. The offset voltage value to enter will be 3.3 V / 2 or 1.65 because the 100kΩ resistors are connected to both GND and 3.3V.

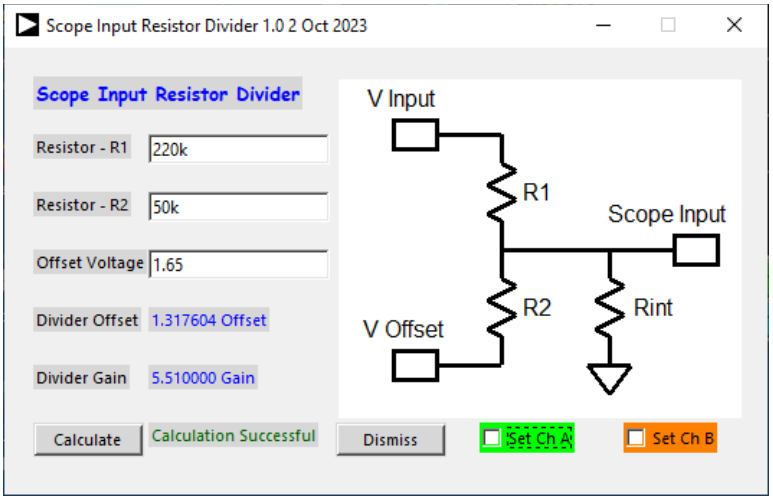



Figure 14, ALICE resistor input divider gain calculator

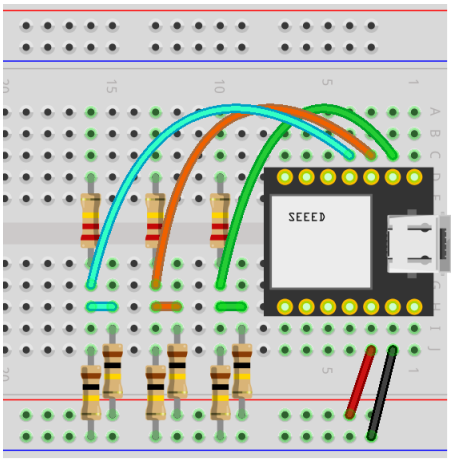
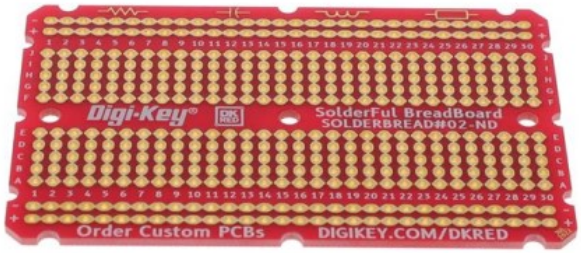



Figure 15, Dividers included on a solderless breadboard

The XIAO module along with any input resistor dividers could additionally be permanently mounted on a solder breadboard such as this one from Digi-Key: Cost $1.48.




Digi-Key part number: DKS-SOLDERBREAD-02, 30 ROW SOLDERFUL BREADBOARD

Breadboard, General Purpose Plated Through Hole (PTH) 5 Hole Pad (Both Sides) 0.100" (2.54mm)