Seeed Studio XIAO SAMD21 as an introductory personal instrument.

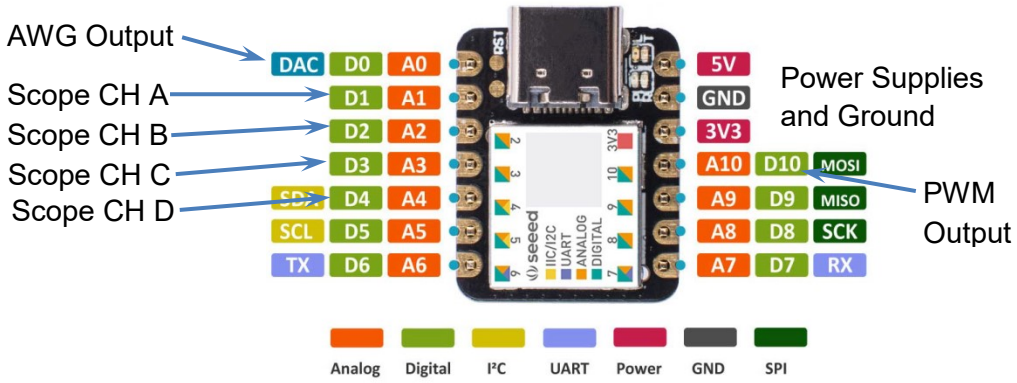
Objective:

To demonstrate the use of the Seeed Studio XIAO SAMD21 micro-controller board as a personal lab data measurement system in introductory level circuits (and electronics) courses. The main intended audience of this document is instructors wishing to learn the capabilities of the hardware and software. Parts of the document could be adapted for use by students as a starting introduction to the hardware and software.

Hardware:

Seeed Studio XIAO SAMD21 micro-controller board. Cost $5.40 (Digi-Key Part Number 1597-102010328-ND)

The XIAO board is a small 14 pin DIP like module. By installing male pin headers it can be easily inserted into a solderless breadboard and effectively becomes just another “part” in the experimental setup.



XIAO pinout

The XIAO contains one 12 bit ADC which can be multiplexed to multiple pins. It also contains one 10 bit DAC available on pin A0. The overall maximum ADC sample rate (~100 KSPS) will be shared by the scope input channels and the per channel sample rate will depend on the number of analog input pins being measured. The sample rate of the internal 10 Bit DAC is roughly 70 KSPS or 14 microseconds. The XIAO can also generate a PWM digital output on pin D10. This PWM output (at 93.750 kHz) can also be modulated with 9 bit resolution samples at the same rate as the DAC. The PWM output is then low pass filtered to provide a pseudo second AWG output channel (B).

None of the XIAO pins are 5 V tolerant and will likely be damaged if voltages beyond 0 and 3.3V are applied. The XIAO SAMD21 is a 3.3 volts device and applying 5 volts to an input will overload and damage the XIAO. There may be a connection on the board to the 5 volt USB power, but DO NOT use it to power experiments unless you are certain of the voltages of any nodes you might be measuring with one of the input pins. Absolute Maximum Pin voltage with respect to GND - GND-0.6V and VDD - VDD+0.6V.

Extra required materials, USB A to USB C cable, Solderless breadboard, various components, resistors, capacitors, diodes, transistors …

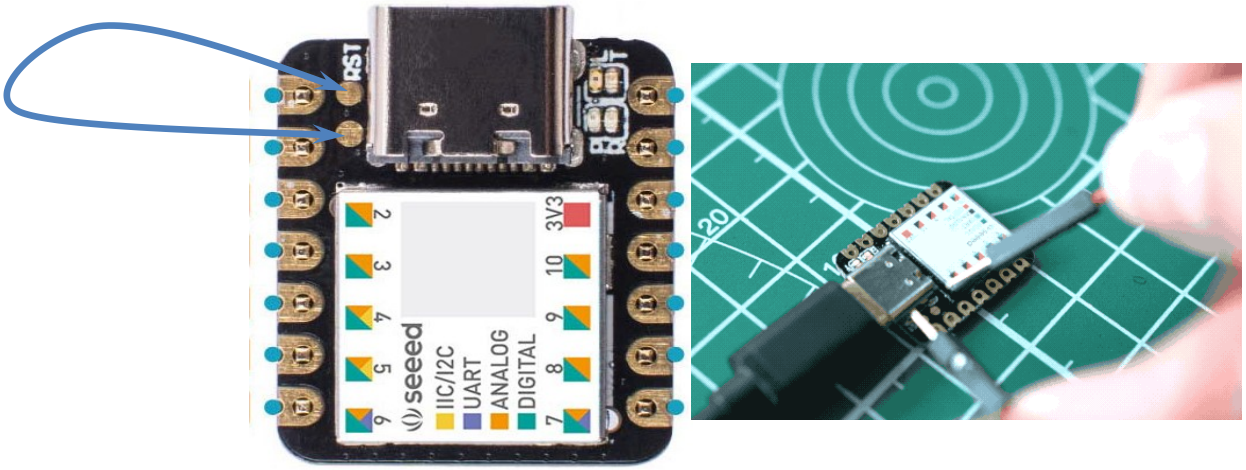
Board Firmware:

Developed using the Arduino IDE.

The firmware file XIAO_Scope_pwm_awg.uf2 from Zip archive.

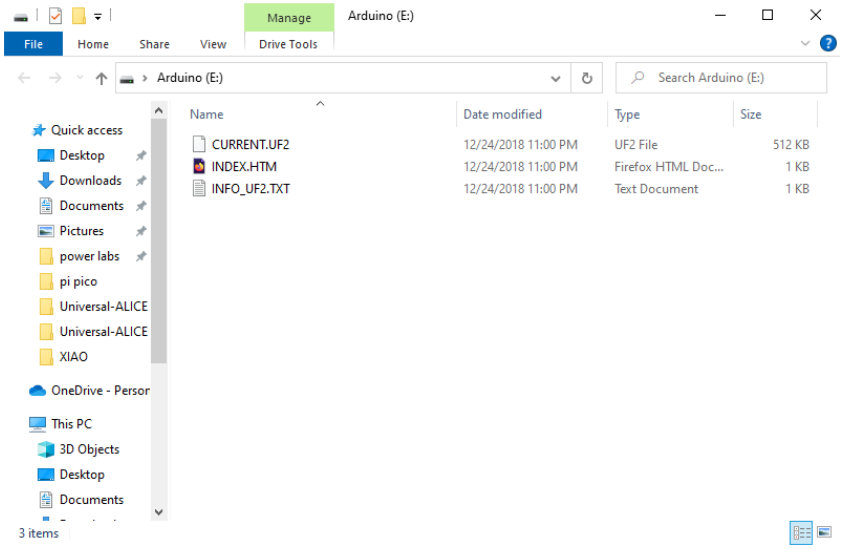
To load the .uf2 firmware file, the board needs to be put into the UF2 Bootloader. There are a couple of ways to accomplish this. Some are more difficult than others. Choose the one that seems the easiest to do for you.

Method 1: With the board plugged into a USB port and powered up, use a wire jumper to short the two small round pads, labeled RST, to the left of the USB C connector as shown below. Short the pads **twice quickly**, i.e. tap, to put the board into the bootloader. The amber (yellow) LED will flash and then go into a slow “breathing” mode.



Placing board into bootloader Method 1

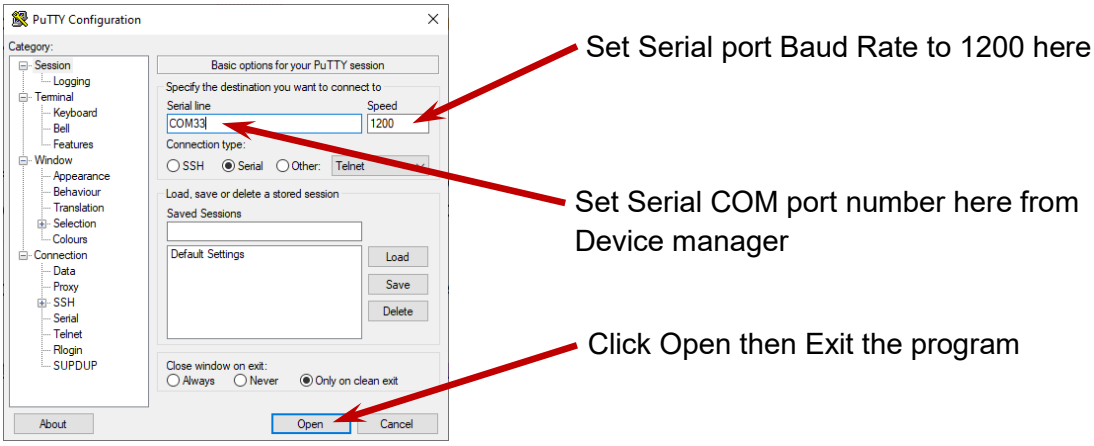
An external USB drive folder should pop up like this:



External drive folder Arduino (E:)

Method 2: Using a serial terminal program, such as PuTTY on Windows, connect to the board’s serial port at 1200 Baud and then close the connection by exiting the serial terminal program. (On Windows

the COM port number can be found using the Device Manager). The external USB drive folder should pop up as in Method 1.



Placing board into bootloader Method 2

Copy and paste the firmware file XIAO_Scope_pwm_awg.uf2 on to this new USB drive (Drag and Drop works). The drive window will close (disappear) and the yellow LED will go out and just the green power LED will be on. The board is now programed with the firmware and ready to use.

Method 3: Use ALICE PC Host software, See Below.

Alternatively the Arduino source code can be compiled and up loaded to the board using the Arduino IDE. Source code sketch from here:

https://github.com/damercer/Arduino-Scopes/tree/main/XIAO_Scope_pwm_awg

PC Host Software:

ALICE Universal, PC Host User Interface (numpy library required) developed using Python 3.10 and XIAO SAMD21 hardware specific interface code also developed using Python 3.10 (installing the pyserial library is required). Source code and configuration files (ALICE Users Guide is in same repository) contained in this .zip file:

Alice-universal-alpha.pyw
XIAO_4a_1w_pwm_Interface_Level.py
alice_init.ini
alice-last-config.cfg

At the moment for Windows based computers the ALICE program can up load the firmware file XIAO_Scope_pwm_awg.uf2 to XIAO SAMD21 boards that are not already programed. The .uf2 file must be in the same folder with the Python program(s). External disk drive letter E: must be available, that is, it is not being used by another storage device like a CD/DVD drive or USB drive.

On other Operating systems, at the moment, the program will only place the board in the Bootloader. An external USB drive folder should pop up and the User must manually copy the .uf2 file to the external USB drive as above.

Demonstration Lab Examples:

The test circuit schematic shown in figure 1 and breadboard layout shown in figure 2 is used to illustrate how the micro-controller hardware is connected to a simple R-C low pass circuit. The R-C test circuit consists of R1 and C1. The “grounded” end of C1 is connected to a resistor divider (R2 and R3) between GND (black wire) and the 3.3V power supply (red wire).

The voltage at the divider will be 3.3V / 2 or about 1.65 V. The equivalent resistance seen at the divider node will be 100Ω / 2 or about 50Ω.

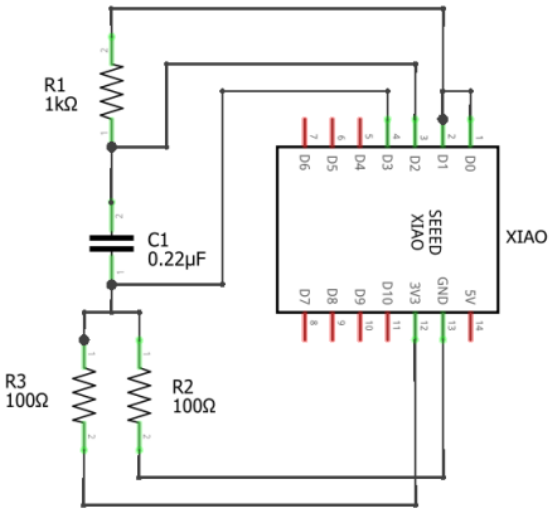


Figure 1, Simple R-C test circuit.

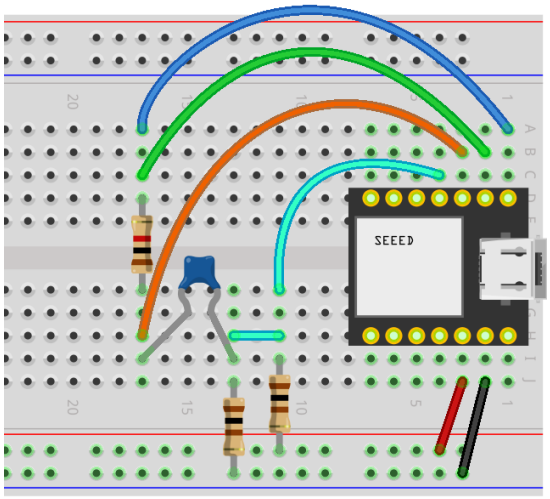


Figure 2, R-C Solderless Breadboard layout.

The A0 pin on the XIAO is the DAC output which provides the AWG (A) function generator output. The A1, A2 and A3 pins on the XIAO are used for the three Scope input channels (CH A, CH B and CH C respectively).

Figure 3 shows the waveform traces as displayed in ALICE. The AWG output is set to generate a 2.8 V p-p sine wave at 300 Hz. The green trace is the green wire in figure 2, the orange trace is the orange wire and the cyan trace is the cyan wire. The p-p voltage seen at the resistor divider junction divided by the 50Ω equivalent resistance is the current in capacitor C1 (about 1.1mA p-p in this example).

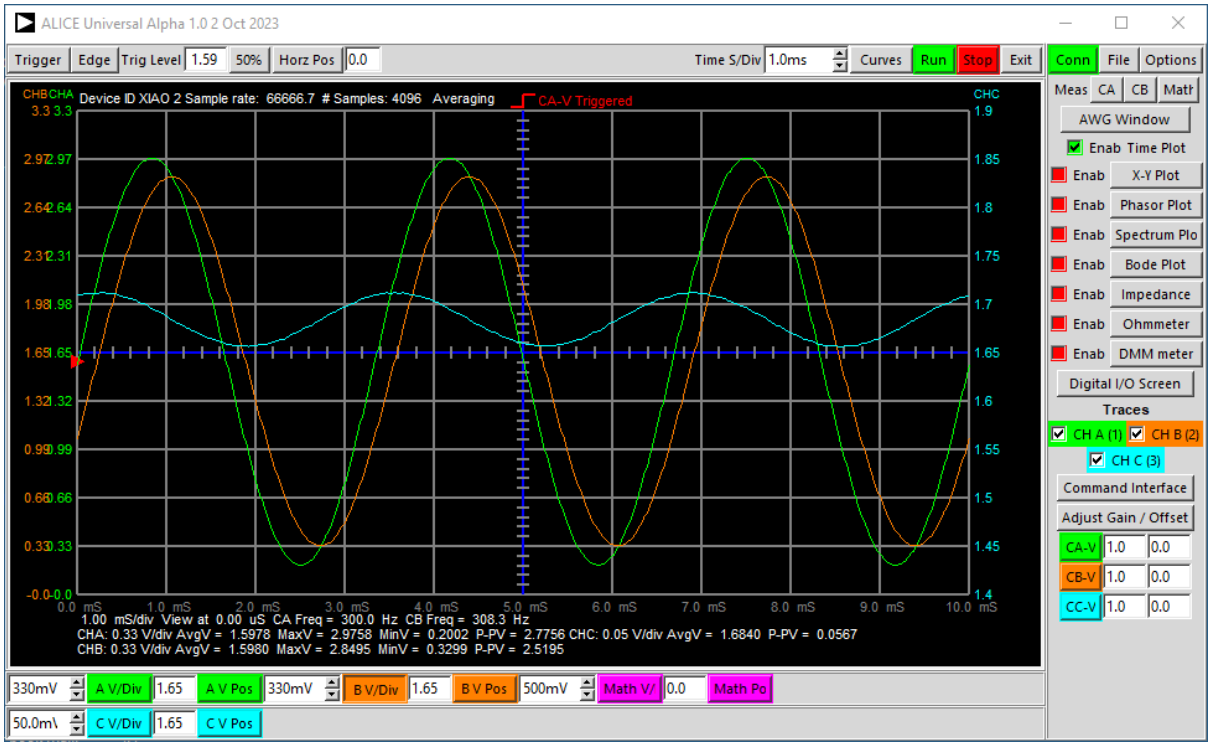


Figure 3, R-C test User interface screen shot.

Using essentially the same breadboard circuit as in Figure 2 we can plot the I/V curve of a diode. We replace C1 with diode D1 (1N914 or similar) and change the value of R1 to 150Ω, as in figures 4 and 5. The DAC output is set to generate a 122 Hz triangle waveform that swings the maximum voltage from nearly 0 to 3.2 V. Again we reference the "negative" end of the diode to the ½ supply divider to apply positive and negative voltages across the diode.

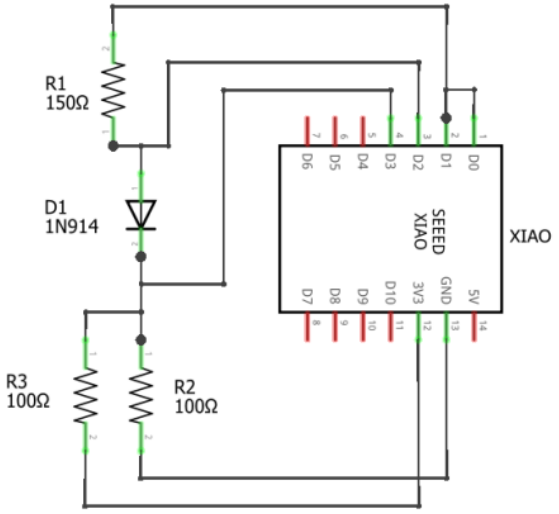


Figure 4, Diode I/V test circuit.

We can use the X-Y plotting tool in ALICE to calculate the current in the diode and plot it vs the voltage across the diode as shown in the figure 6 X-Y window screen shot. The vertical Y axis is scaled in mA. The horizontal axis has been shifted to be centered on 0 V across the diode.

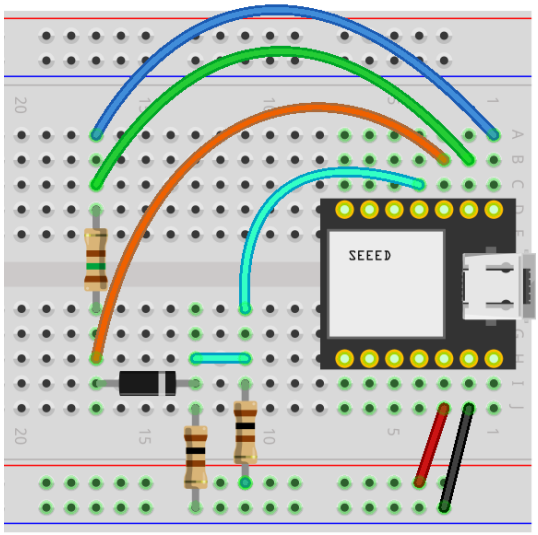


Figure 5, Diode I/V breadboard layout.

We use the Math controls in ALICE to calculate the diode current with the following formula for the Math-X trace:

(VBuffA-VBuffB)*6.6667

Where VBuffA is the voltage on the top of R1 and VBuffB is the voltage on the bottom of R1. We get the voltage across R1 by subtracting the two voltages. The current in mA is scaled by multiplying the difference voltage by 1000/150Ω or 6.6667.

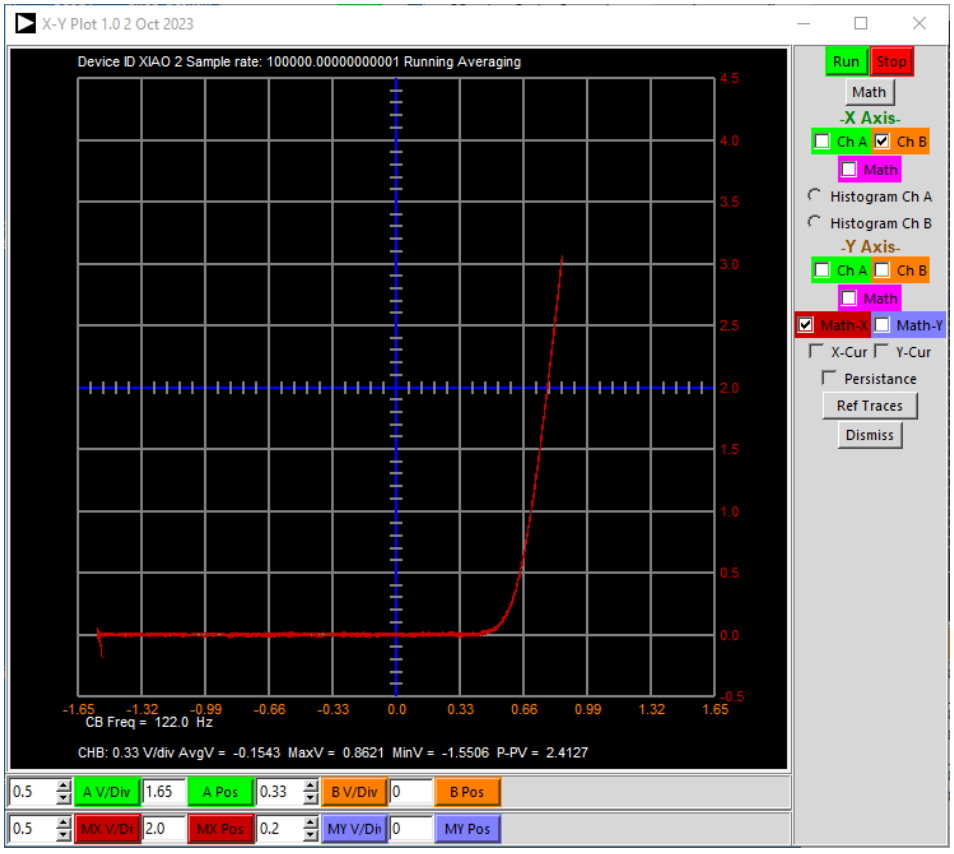


Figure 6, Diode I/V plot.

As a third example test circuit we have an inverting and non-inverting gain of 1 NPN amplifier (the so called “phase splitter”) shown in figure 7. The circuit consists of one NPN transistor (2N3904 or similar) and two 1kΩ resistors. R1 is the collector load resistor and R2 is the emitter resistor. The amplifier input signal from the AWG generator is connected to the base of the transistor. The gain from base to emitter (non-inverting) is +1 as the transistor is acting as an emitter follower. Since R1 and R2 are equal the (inverting) gain from base to collector is -1.

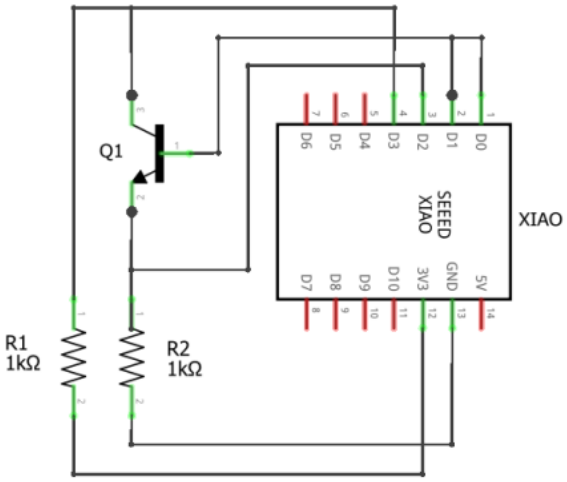


Figure 7, NPN Amplifier schematic

In the breadboard layout shown in figure 8, the AWG output is connected to the base of the transistor (blue wire) and the waveform Shape is a sine wave at 400 Hz. The Min and Max voltage values are adjusted such that neither of the output signals, at the collector or at the emitter, are clipped. We can use the three scope input channels to monitor the input signal at the base (CH A green wire) and the two output signals at the emitter (orange wire) and at the collector (cyan wire) as shown.

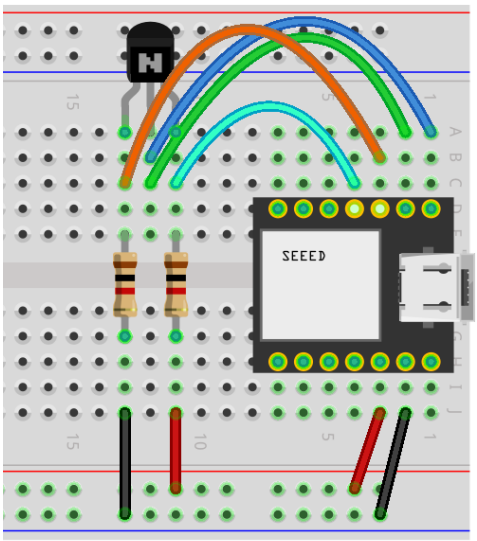


Figure 8, NPN Amplifier breadboard layout.

In figure 9 we see the three scope traces. There is a DC level shift from the input to the respective outputs but the p-p amplitude is nearly the same at gains of +1 to the emitter (orange trace) and -1 to the collector (cyan trace).

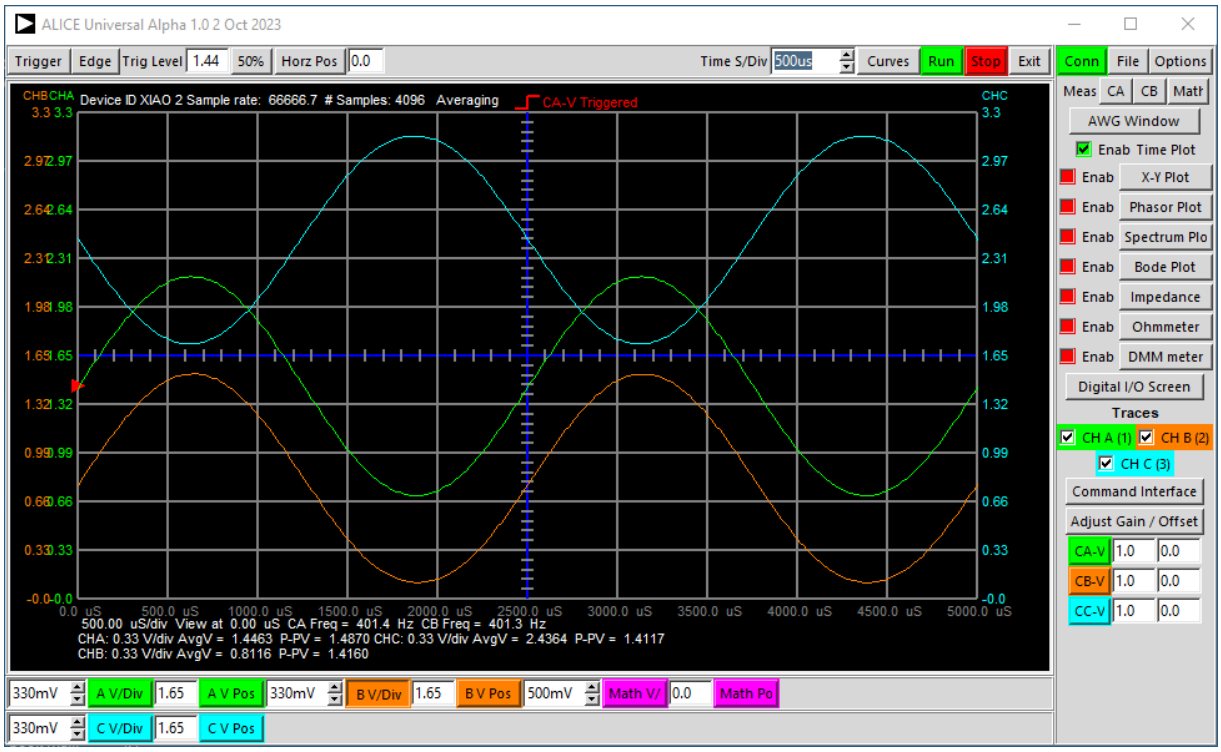


Figure 9, NPN Amplifier Scope traces.

PWM Output as Second AWG Channel:

The PWM digital output on pin D10 can be modulated with analog waveform samples to generate a second AWG output channel. The PWM switching frequency is set at 93.750 kHz which is above the scope sampling frequency (50 KSPS each for two channels in this example) and beyond the input bandwidth and cannot be directly viewed using the scope input.

The PWM signal of course needs to be low pass filtered to reconstruct the analog waveform. A simple R-C filter as shown in figure 10 is sufficient for low frequency waveforms. In the example schematic the analog DAC output AWG (on pin A0) is measured using Scope CH A (on pin A1) for reference purposes. The D10 output is filtered by R1, 1.5kΩ, and C1, 0.22µF. The filtered output is measured by Scope CH B (on pin A2).

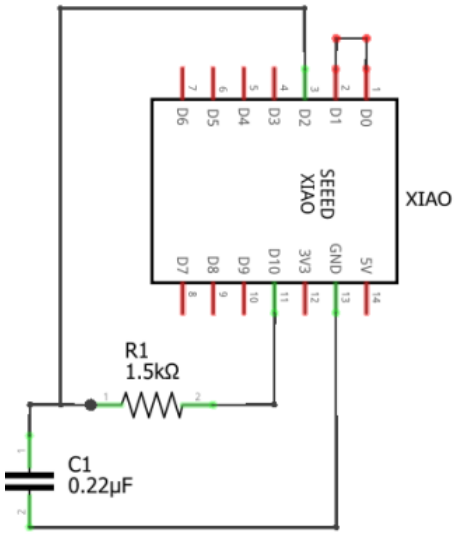


Figure 10, R-C low pass filtered PWM output AWG channel.

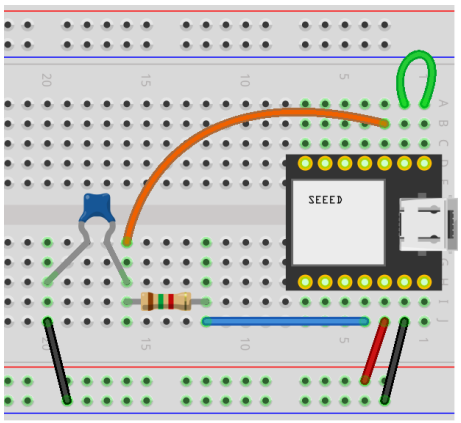


Figure 11, PWM output AWG channel breadboard layout.

For comparison purposes the analog DAC output AWG is displayed on Scope CH A (green trace) and the filtered PWM AWG output is displayed on CH B (orange trace), figure 12. Both are generating a 150 Hz sine wave. The Min and Max values of the DAC channel is set to 0.2 and 3.0 V and the PWM channel was adjusted to approximately match the AWG A output amplitude and offset at 0.12 and 3.11 V. The digital output is not going to produce an exact 0 to 3.3 V swing. The R-C filter time constant introduces a phase delay in channel B but that could be corrected for by introducing an appropriate phase shift in the PWM waveform data samples with respect to the DAC waveform.

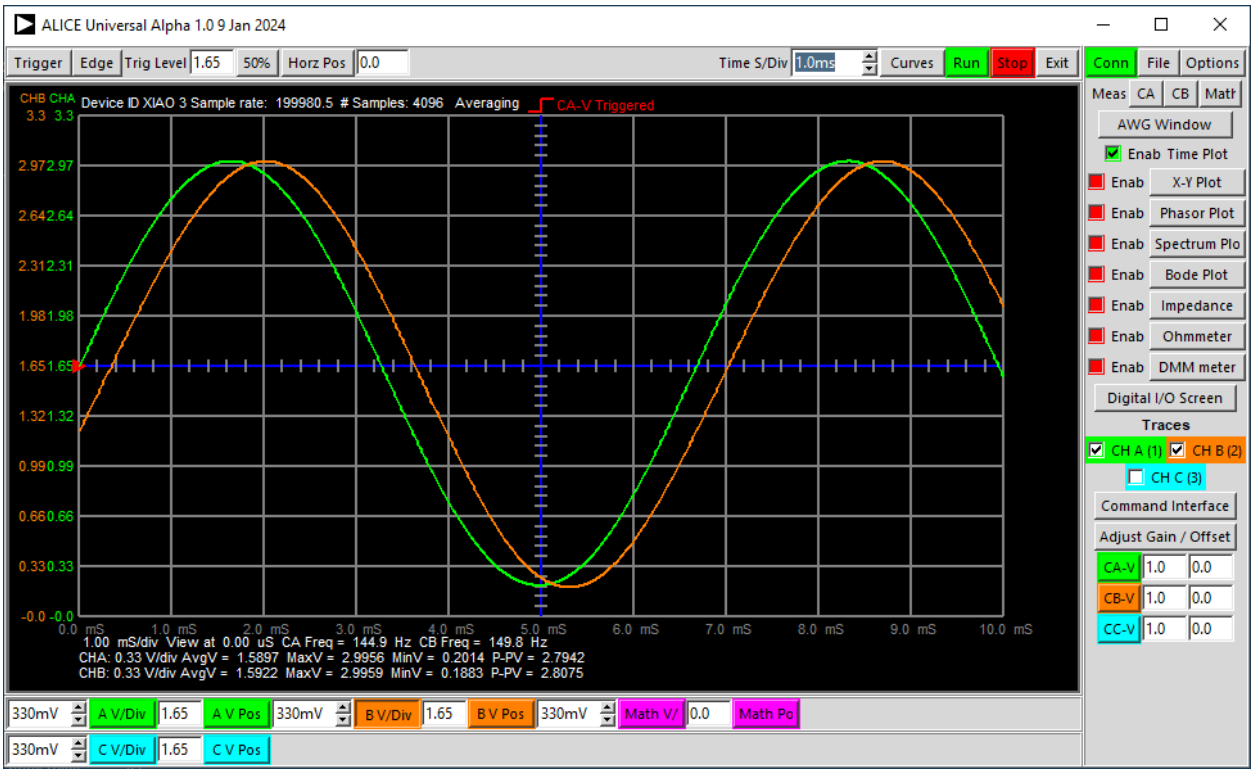


Figure 12, R-C low pass filtered PWM output waveform vs DAC waveform.

Note:

Care should be taken to insure that the Scope inputs are never connected to voltages greater than 3.3 V such as the nearly 5 V supply rail that is also available on the XIAO module. The Scope inputs can be made “5V Tolerant” by inserting a resistor of at least 5kΩ (4.7kΩ or 5.1kΩ) between the XIAO module pin and the circuit node being measured. The added series resistance will have a negligible effect owing to the relatively high impedance of the ADC inputs but limit the current to a safe level.

Input Dividers for voltages beyond 0 to 3.3V:

The relatively high input impedance of the XIAO module allows the use of relatively simple resistive input dividers. Example dividers are shown in figure 13. The 220kΩ and 2 100kΩ parallel resistors combine to make an input scale factor of ~5.5:1 with an offset that centers the allowed peak to peak input swing of 5.5 X 3.3 V ~ 18 V on 1.65 V (-16.35 to 19.65). The input resistance will be 220kΩ + 50kΩ or 270kΩ. The relatively high 220kΩ value of the input resistor inherently limits the current that might flow into the XIAO input pin during over voltage conditions.

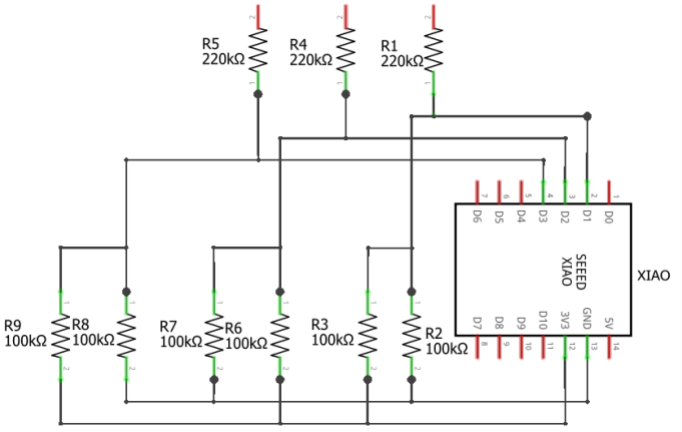


Figure 13, Input resistor voltage divider example

Other resistor values and combinations are of course possible but it is best to keep the effective resistance seen at the XIAO input pins no greater than 50k and actually the lower the better. If a higher resistance divider is requited then an op-amp buffer should be placed between the divider output and the XIAO ADC (Scope) inputs.

ALICE provides an input resistor divider calculator tool as shown in figure 14. The resistor value to enter for R1 in the above example is of course the 220k. The resistor value to enter for R2 is the parallel combination of the two 100kΩ resistors or 50kΩ. The offset voltage value to enter will be 3.3 V / 2 or 1.65 because the 100kΩ resistors are connected to both GND and 3.3V.

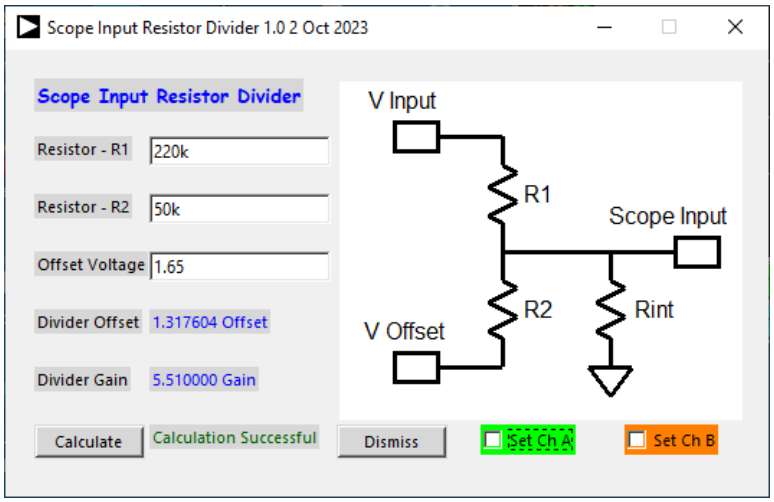


Figure 14, ALICE resistor input divider gain calculator

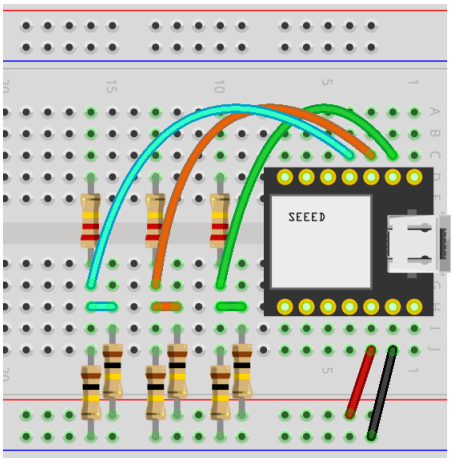
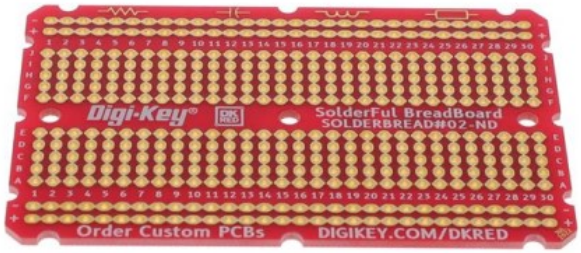


Figure 15, Dividers included on a solderless breadboard

The XIAO module along with any input resistor dividers could additionally be permanently mounted on a solder breadboard such as this one from Digi-Key: Cost $1.48.



Digi-Key part number: DKS-SOLDERBREAD-02, 30 ROW SOLDERFUL BREADBOARD

Breadboard, General Purpose Plated Through Hole (PTH) 5 Hole Pad (Both Sides) 0.100" (2.54mm)

Effects of Source Impedance Test:

Unlike more complete (more costly) solutions these MCU breakout boards do not include any of the analog signal processing chain often built into more advanced data acquisition hardware. The raw input of the internal ADC is not buffered and the charge redistribution nature of the ADC presents finite impedance to the circuit being measured. This input impedance will be in parallel with any impedance of the node being measured and will affect the results (such as using external resistor dividers as discussed above).

To demonstrate this effect the following experiment can be done. By inserting various resistors in series with the AWG output we can change the source impedance and see the effect. Connect the AWG output to 1kΩ, 10kΩ and 100kΩ resistors as shown in figure 16. Scope channel A is connected directly to the AWG output with no series resistance to be used for comparison. Scope channel B is connected to the AWG output through one of the three series resistors.

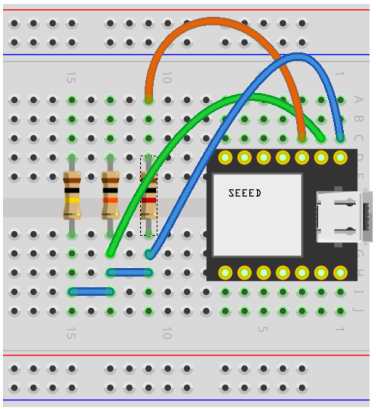


Figure 16, Source Impedance Test.

The following series of Scope plots show the Channel A and B traces (green and orange) and the Math trace of CHA – CHB to show the difference between the two for the three different series resistors, 1kΩ, 10kΩ and 100kΩ.

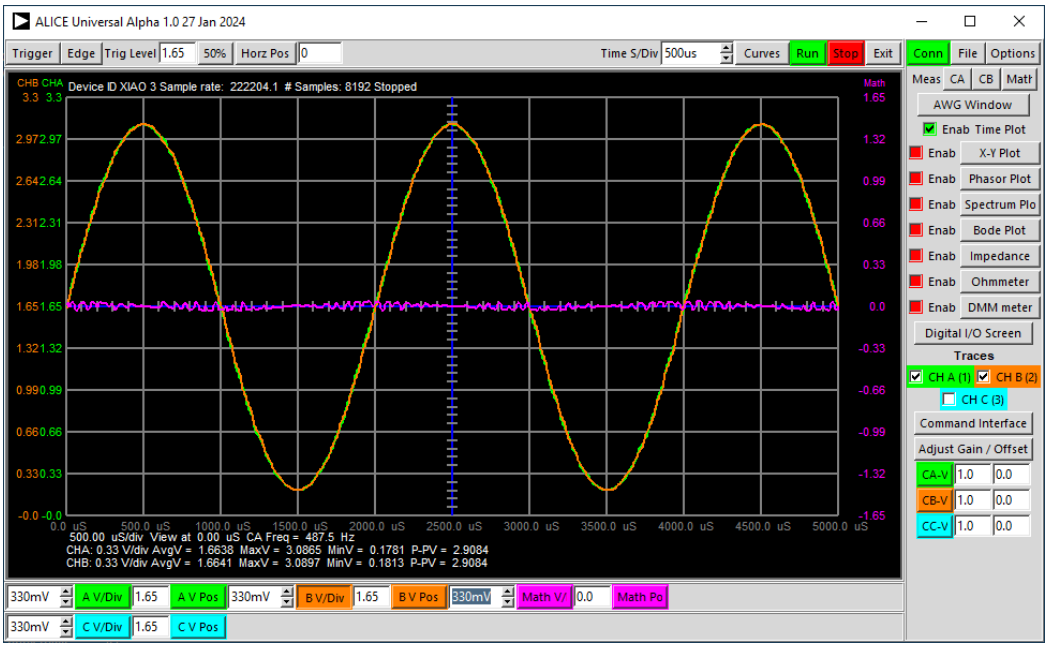


Figure 17, 1kΩ Source Impedance.

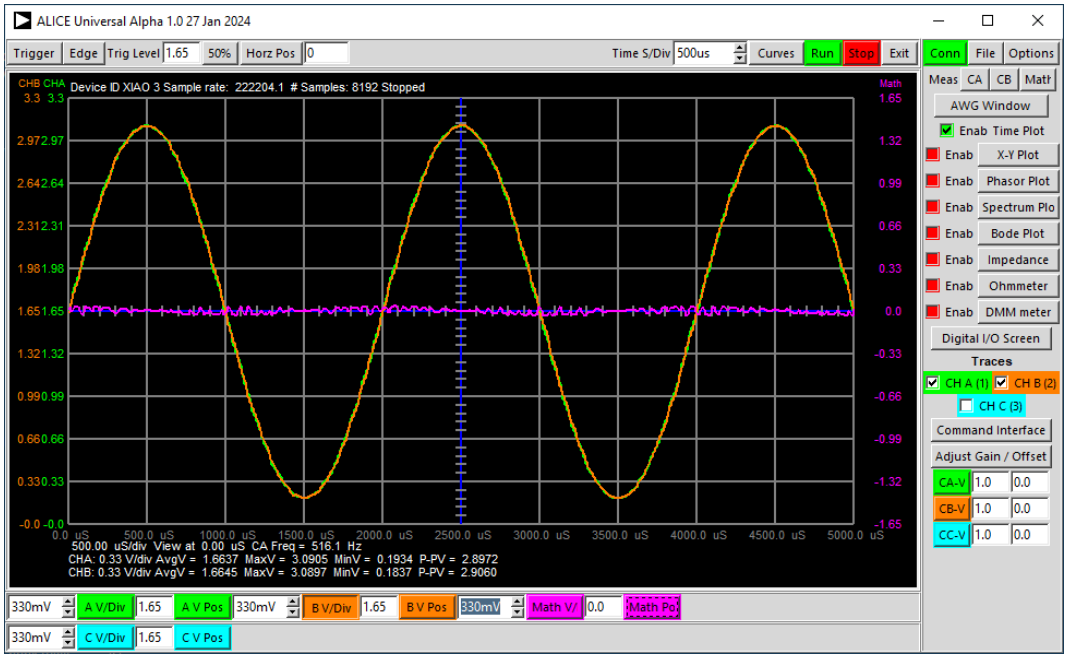


Figure 18, 10kΩ Source Impedance.

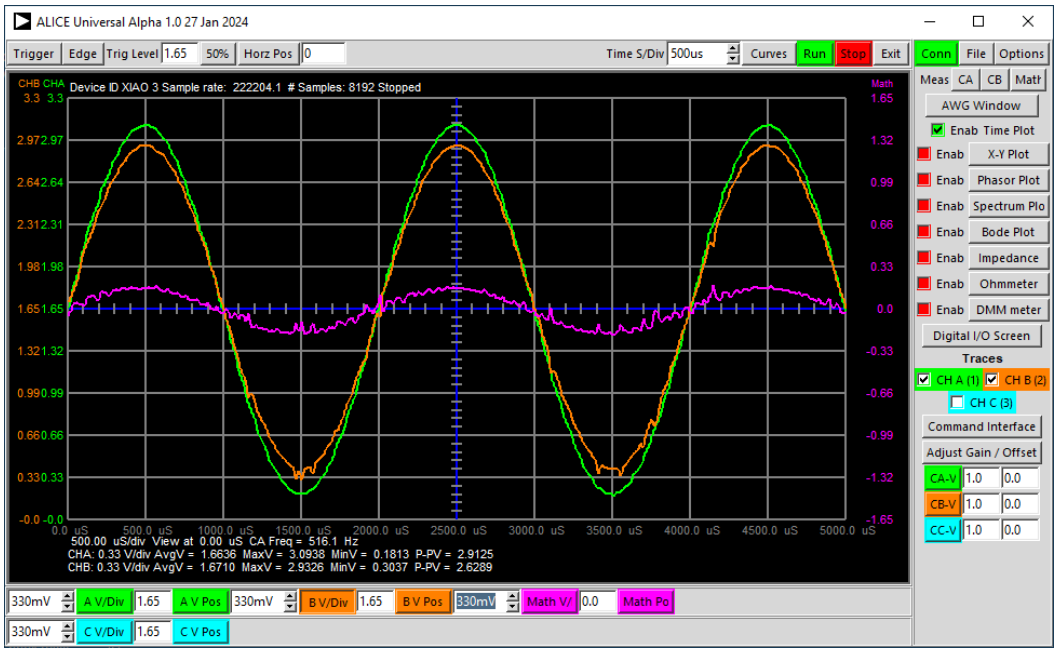


Figure 19, 100kΩ Source Impedance.

The 1kΩ and 10kΩ traces show very little difference between the waveform with no series resistance while the 100kΩ trace shows a significant reduction in the channel B amplitude and an increase in the level of the noise (large jumps seen at some sample points due to incomplete settling of the ADC input). The channel B amplitude is about 88.5% lower now and a 200 mV offset has been introduced. From these tests it looks like source impedance up to 10kΩ gives acceptable results. Beyond that measurement results will start to degrade noticeably. Another set of traces for a 1MegΩ series resistor is included below as well for completeness.

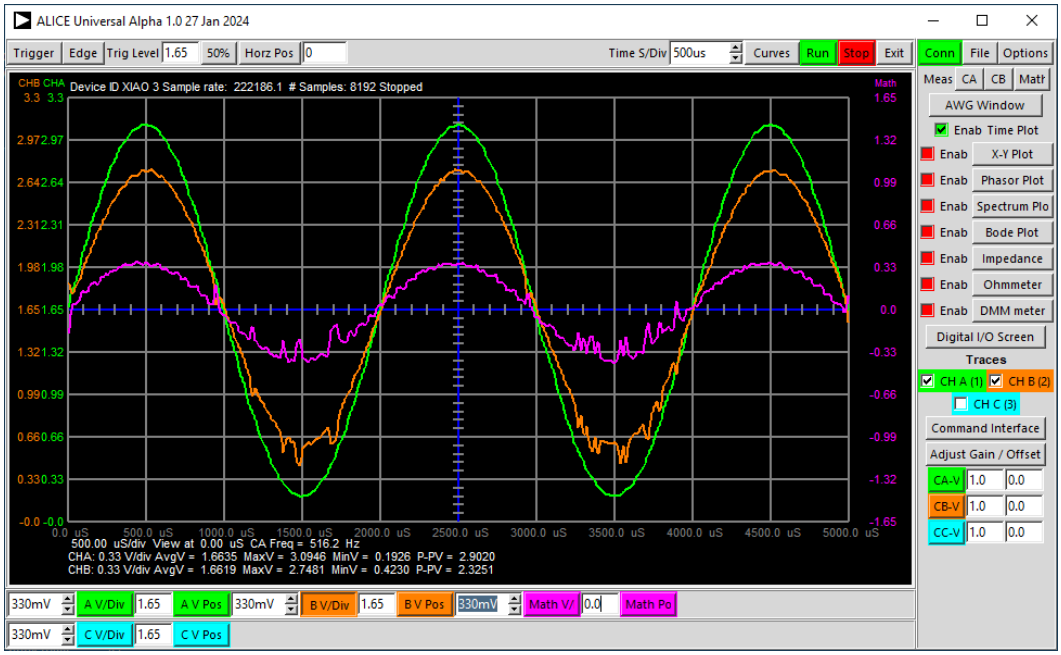


Figure 20, 1MegΩ Source Impedance.

The ALICE software provides the ability to mathematically correct for gain and offset in channel B by entering correction factors (lower right corner of Scope screen. The software also has the ability to average multiple sweeps (trace averaging) to smooth out the uncorrelated noise in periodic signals. The following screen (figure 21) shows the 100kΩ results when the gain (1.13) and offset (0.2) errors for channel B are corrected and trace averaging is applied.

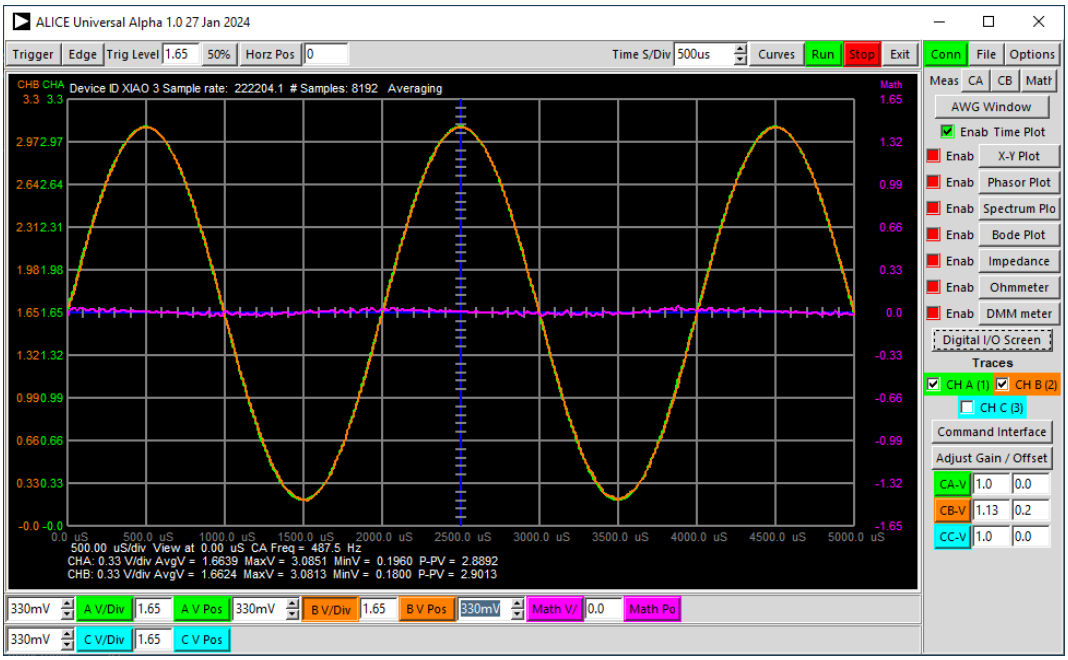


Figure 21, 100kΩ Source Impedance with gain / offset correction and averaging.

Negative Voltage Generator:

There are some use cases where a small negative voltage is necessary. One example is powering op-amp circuits. Many times op-amps with true rail-to-rail input and output voltage ranges such as the OP484 are not readily available. Powering a non-rail-to-rail amplifier such as the uA741 from a small negative voltage rather than ground will often be sufficient to produce a negative output swing to 0 V.

A simple switched capacitor voltage inverter, as shown in figure 22, driven by the 0 to 3.3V square wave from the PWM digital output on pin D10, can generate -2.0 volts at 1 mA of current. Diodes D_1 and D_2 are conventional Si diodes with 0.65 V forward drop so the peak output is reduced from 3.3 V by 2 diode drops (1.3V) to -2 V. If Schottky diodes are used the peak output voltage could be closer to -2.7 V.

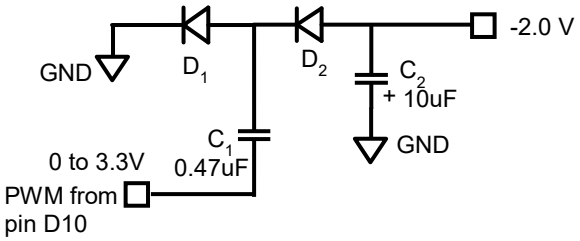


Figure 22, Negative voltage generator.

Setting the digital PWM signal frequency to around 20 kHz with a 50% duty cycle is optimal. The available output current can be increased by driving capacitor C_1 from higher current external CMOS drivers / gates.

As an example use case an inverting gain of 1 op-amp circuit using a uA741 is shown in figure 23. A resistor divider between GND and +3.3V generates a +1.65 V common mode voltage to bias the + input of the op-amp. A 1kΩ resistor is inserted in series with the CH B input pin to protect from possible overvoltage. This is not likely given the limited supply voltages of the uA741 but is always good practice when a test circuit is powered from supplies outside 0 to 3.3V.

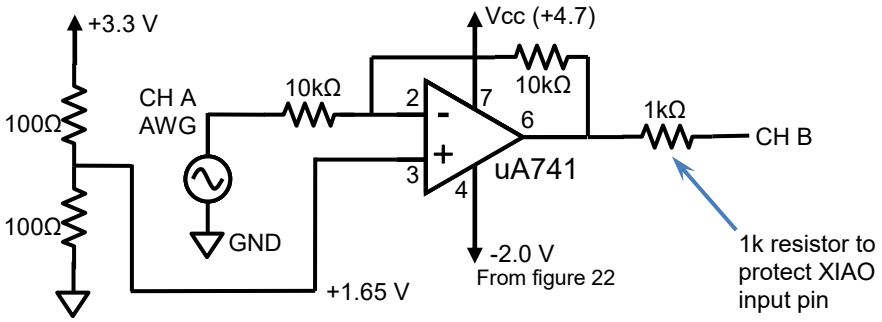


Figure 23, uA741 example powered from +4.7V and -2.0V.

Figure 24 shows the results. A resistor divider / attenuator is used along with Scope channel C to measure the -2.0V supply.

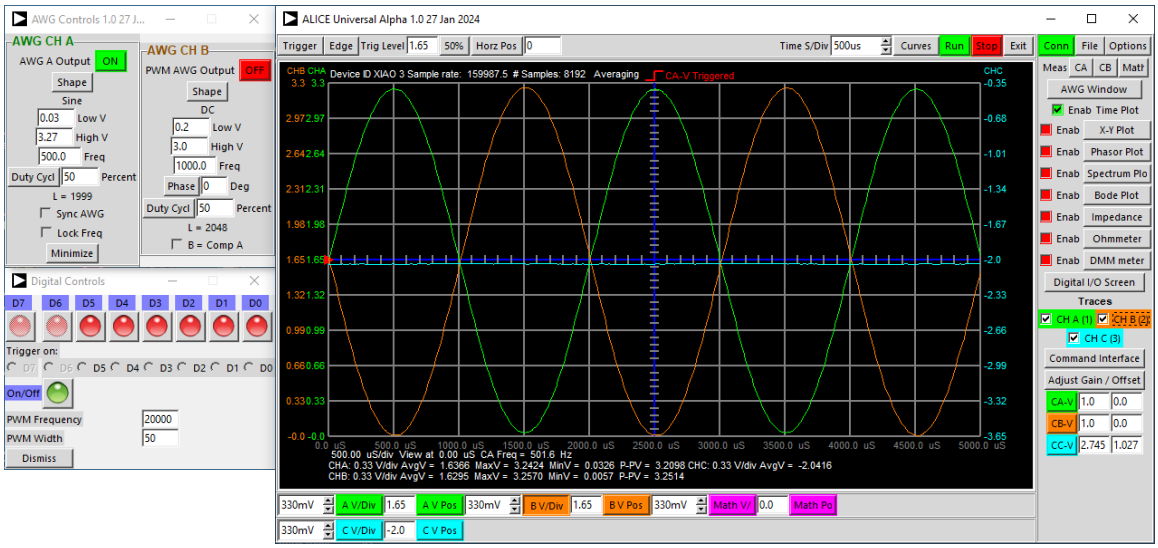


Figure 24, uA741 example powered from +4.7V and -2.0V.