# Hardware Research (revised 1/18/25):

Software-Configured Breadboard Hardware Targeting Circuit Wiring Error Reduction in ECE Labs.

**Abstract:**

The hardware project aims to examine the effectiveness of software-configured wiring compared to traditional manual wiring of breadboards. While both methods use actual hardware, the software-configured approach automates the connections between components, thereby minimizing wiring errors and setup time. The intent is to investigate the impact of each approach on student comprehension, engagement, and error rates. By comparing these two approaches, the project seeks to determine which method better supports student engagement, educational outcomes and reduces frustration associated with complex circuit construction.

**Introduction:**

Hands-on experiential learning is a cornerstone of ECE education, typically relying on manual wiring of circuits on solderless breadboards. Using a traditional solderless breadboard as the means for building electronic circuit lab experiments requires the student, in addition to placing components, to manually insert wires to connect together the component pins according to a schematic diagram. These manual translation steps from schematic to hardware can lead to wiring errors in the experimental setup that can obscure circuit principles. While this manual wiring method offers valuable experience in physical component handling and troubleshooting, the extra time needed for debugging and correcting these errors leads to frustration and loss of precious lab time to investigate the circuit concept in question.

Recently, commercially available software-configurable bread boarding platforms have emerged[1], allowing users to build real circuits with automated wiring based on computer software input, thus retaining the tactile experience while minimizing connection errors. The intent is not to compare such commercial devices since the development of the proposed lower cost system (See more details in Appendix below) is progressing well.

As additional background, one approach that has been used to reduce wiring mistakes is to build pre-wired printed circuit experiment boards[2]. However, this approach has limited configurability and component flexibility to explore multiple circuit configurations. In addition pre-wired printed circuit boards do not offer the same level of experience in physical component handling, troubleshooting and debugging.

The goal is to evaluate the educational benefits and potential drawbacks of these software-configured hardware systems compared to traditional manual wiring. By doing so, it addresses the need for balancing hands-on skills with error minimization and conceptual understanding in electrical engineering education.

**High Level Development Plan:**

The goal of this project is to develop and build a “smart” software defined or configurable breadboard system (SCB). The proposed project leverages the results of the prototype hardware outlined in the appendix below now under investigation.

- Construct software configurable breadboard hardware for pilot evaluation.

- Develop / Adapt pilot course materials based on existing solderless breadboard labs that motivate the design and demonstrate its capabilities. Initial focus will be on basic functionality.

- Explore and develop *build on demand / build to order* supply chain(s) for the hardware. Exploring ways to cost effectively obtain such hardware may actually be a more important broadly impactful aspect of this project.

**Potential Implications:**

The results of this study could have significant implications for the design of electronics lab curricula. If software-configurable hardware systems are found to be more effective in reducing errors without compromising learning, they could be integrated into introductory courses to provide a balanced learning experience. Conversely, if manual wiring proves essential for certain skill development, educators may consider using a hybrid approach in some courses, incorporating both methods based on learning objectives.

**Overall Plan for the Budget (to be determined by principal researchers):**

-The base budget for the project is:

- Materials cost, $2000 (approx. for 24 boards)

- Faculty Hours?

- Staff support Hours?

- Student Hours?

## Appendix:

## Analog switch matrix cross point experiment breadboard.

The idea is to computerize the wiring of the breadboard in an effort to reduce student frustration when building complex experiments. Using four analog 16X8 cross point switches wired together into two 32X8 cross points with a fifth switch matrix interconnecting the two smaller arrays into effectively a single 64X16 array. This breadboard makes real, hardware connections between the 64 component pins on the board to the16 “jumper” nodes on the board via software commands, instead of needing to manually install jumper wires. The prototype PCB is shown, figure 1, which incorporates two mini 170 pin solderless breadboards, one for each of the 32X8 cross point arrays. There are a combined 68 total component pin locations across both mini breadboards with power distribution strips top and bottom. The two mini breadboards connect to the PCB through pogo pins and so they can be easily removed. It would then be possible to bolt on custom daughter PCBs with whatever components are needed for a given course already installed. Such as CMOS transistor arrays (CD4007) with even some pre-wired sub-circuits like current sources and OTAs.

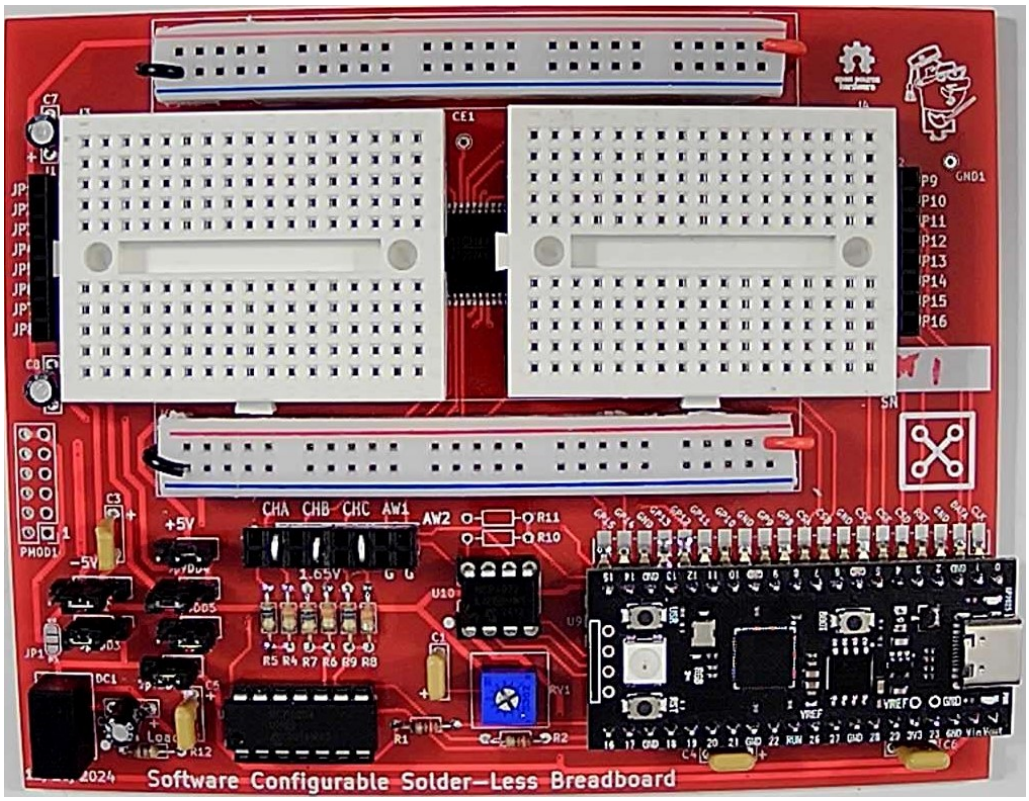



Figure 1, Prototype PCB.

The combined 64X16 cross point matrix board uses a total of 5 CH446DS [2] 16X8 analog cross point ICs (from China) programed via a RP-2040 micro controller breakout board (Pi Pico[3] or equivalent). Materials cost per board, in quantities of 10 or more, is less than $30 not including the assembly labor.

The board is powered from the Pi Pico USB connection. Male Pin Jumpers for powering the experiment can be set for 0 and +3.3V, 0 and +5V or -5V and +5V power (or 0 and +10V) using an on board isolated 5V DC-DC generator.

LTspice[4] is used to enter the schematic for the experiment. In addition to the standard library symbols a number of supporting schematic library files have been created, figure 2. Schematic symbols for TO-92 transistors and resistors of various lead spacing have been created. There are also example schematic symbols with the proper pin spacing for 8, 14 and 16 pin DIP packages. The standard library components can of course also be used.

The library schematics for the switch matrix connections contain 60 Ω resistors and 16 pF capacitors which model the analog switch. One end of a matrix switch will have the component pin net and the other end will have one of the 16 "jumper" nets (JP1-16).

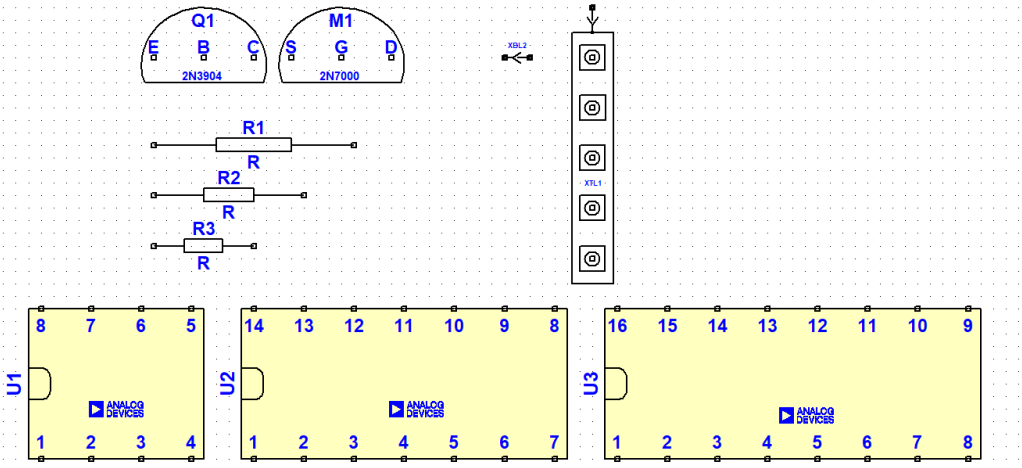



Figure 2, Schematic symbols.

A floor planning schematic template, figure 3, has been created to help the user figure out where to place the parts on the left and right side mini breadboards and then use the "jumpers" to wire them together. There is a schematic symbol for each breadboard column (the 5 pins shorted together). Each breadboard column has a specific name based on its location. Names are numbered from 1 to 17 starting with the top left section, TL1-17, then the bottom left section, BL1-17, then the top right section TR1-17, and finally the bottom right section, BR1-17.

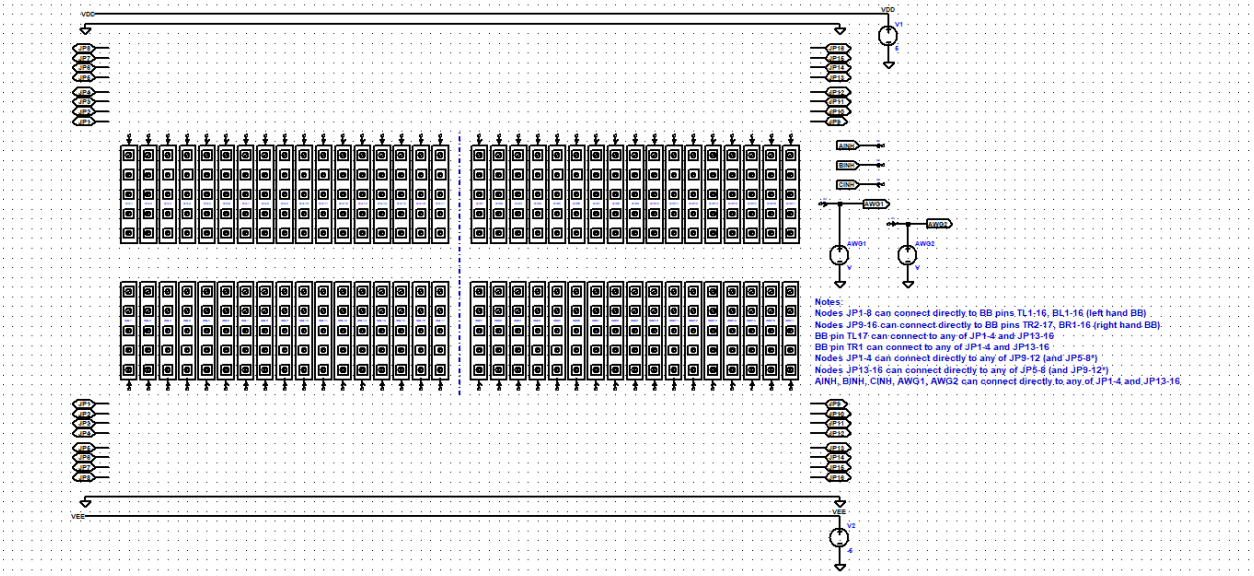



Figure 3, LTspice floor planner template schematic

In figure 4 we see an example circuit of a transistor level op-amp that has been floorplanned and interconnected with the JP jumper nets. Components can also be connected between a column pin and one of the top and bottom power and ground rails simply by a wire.

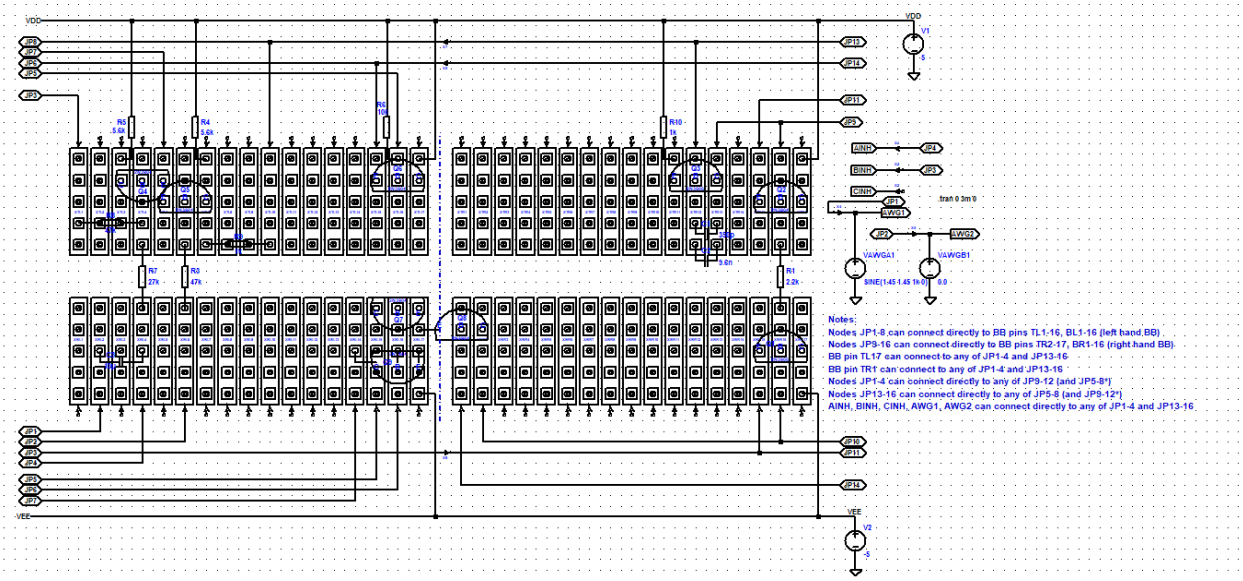



Figure 4, Example floor planned circuit

There is also a way to draw the circuit as a more conventional schematic, figure 5. The same op-amp circuit has been redrawn using standard symbols from the LTspice library with the addition of single switch interconnection symbols. The little pointy arrow symbols are placed in series with certain nets to indicate the component locations on the breadboard. These interconnection symbols are again named based on the BB holes (TL1-17, BL1-17, TR1-17, BR1-17) the parts are plugged into. This approach is easier to visualize the circuit as a schematic but perhaps harder to floor plan where to place the devices.

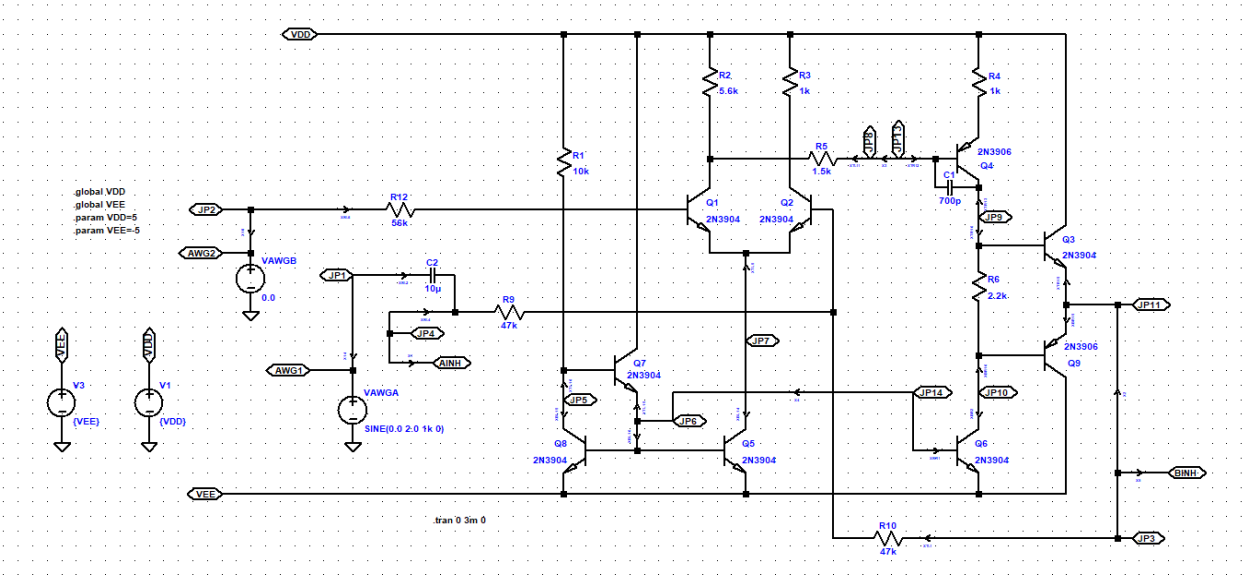
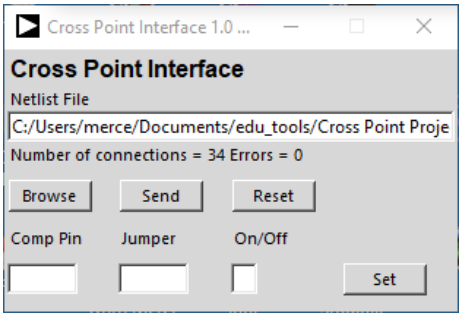



Figure 5, Conventional Schematic method

Correct simulation results insure that you have it all wired correctly before moving to the actual hardware.

A Python script looks through the saved LTspice .cir net list file looking for sub circuits starting with XX in their names. Then parses the connections based on the names (based on breadboard pin locations, TL1-17, BL1-17, TR1-17, BR1-17) and JP1-16 to send commands to the Pi Pico and on to the cross point switches. Everything else is ignored.

As long as you follow these rules when building the schematic the process is simple and mostly automatic. Programming the board is done through ALICE Universal[5] using a hardware specific interface configuration file for this cross point prototype including a way to turn on and off matrix switches manually as well.




Cross Point Matrix control user interface

The following are a few additional example circuits built using the breadboard.

The LTspice schematic in figure 6 was used to configure four CD4007 transistor arrays as a ring oscillator consisting of 11 CMOS inverter stages. It uses 56 of the 68 possible device pins and all 16 of the jumpers of the switch matrix. Manual jumper wires are used to connect each of the DIP (pins 7 and 14) ground and power pins to the power and ground rails on the board. All other connections are programed by the netlist.

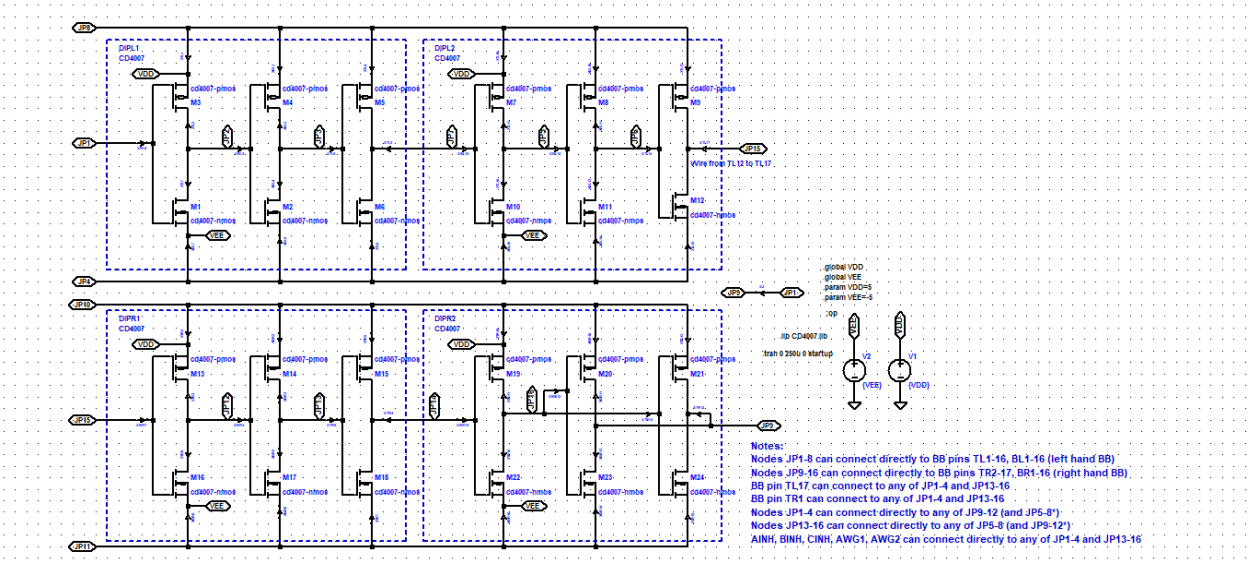



Figure 6, CD4007 LTspice example schematic.

The net list from the example schematic was processed by the python function in ALICE talking to the Pi Pico to configure the matrix. Powered from 0 and +5V, the ring oscillator outputs at JP1 and JP15 are shown on a bench oscilloscope in figure 7 (the waveform is too fast to measure with the Pi Pico scope).

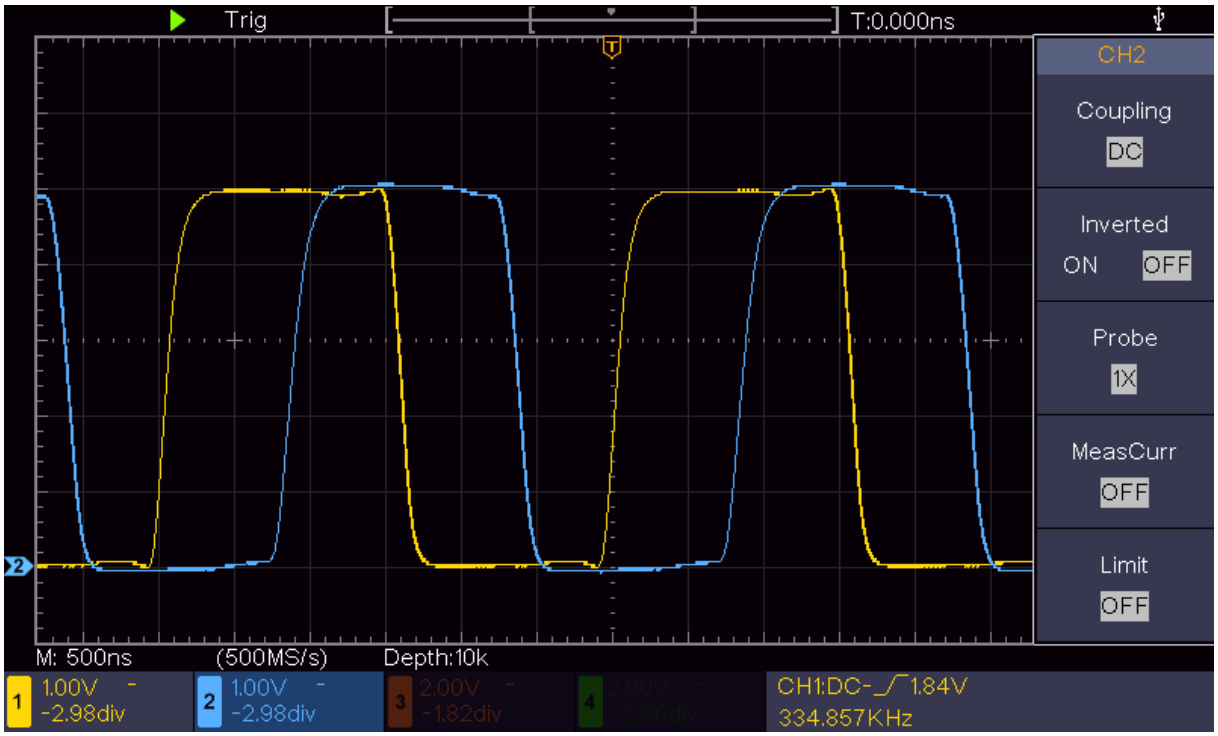



Figure 7, Scope screen shot of +5V ring oscillator output.

The frequency is about 335 KHz.

The CD4007 ring oscillator was measured again with the inverters powered from -5V and +5V and the speed more than doubles to 715 KHz, figure 8.


Figure 8, Scope screen shot of -5V/+5V ring oscillator output.

A Schmitt trigger relaxation oscillator can be constructed from the CD4007 CMOS transistor level inverters, figure 9. The Schmitt trigger is made by rearranging the connections and adding resistor R1 and Capacitor C1 to set the frequency. The M1,3 and M7,10 inverters are stronger than the other 4 inverters because their sources are connected directly to VDD and VEE rather than through the 60 Ω switch resistances. A “strong” inverter and a “weak” inverter are connected as a latch. This latch action determines the high and low threshold of the Schmitt trigger.

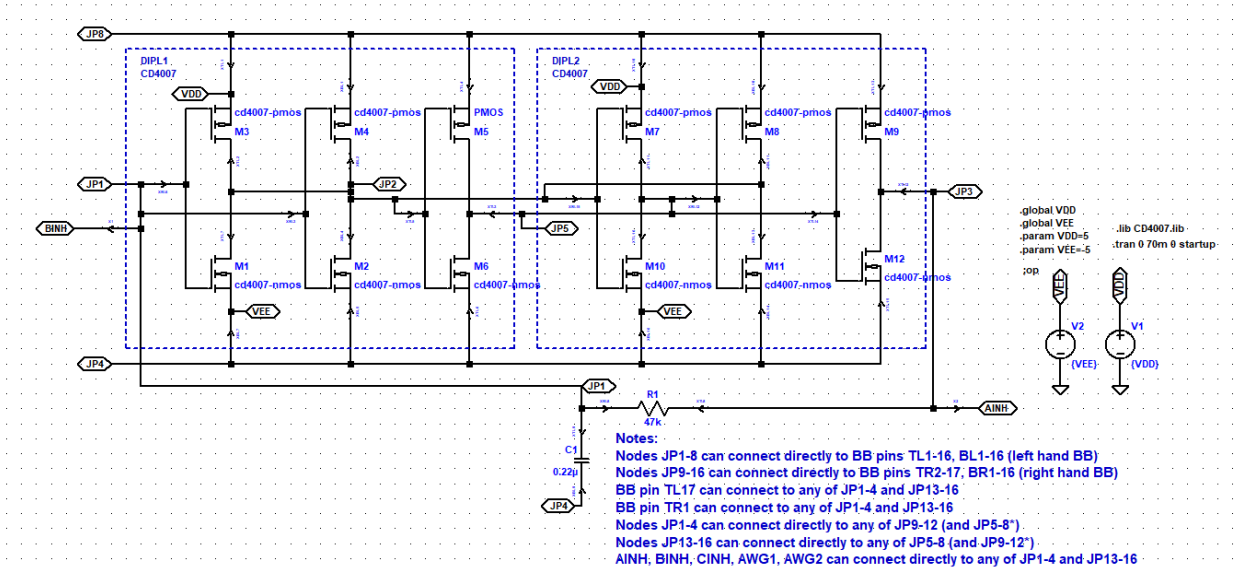



Figure 9, CMOS inverter relaxation oscillator.

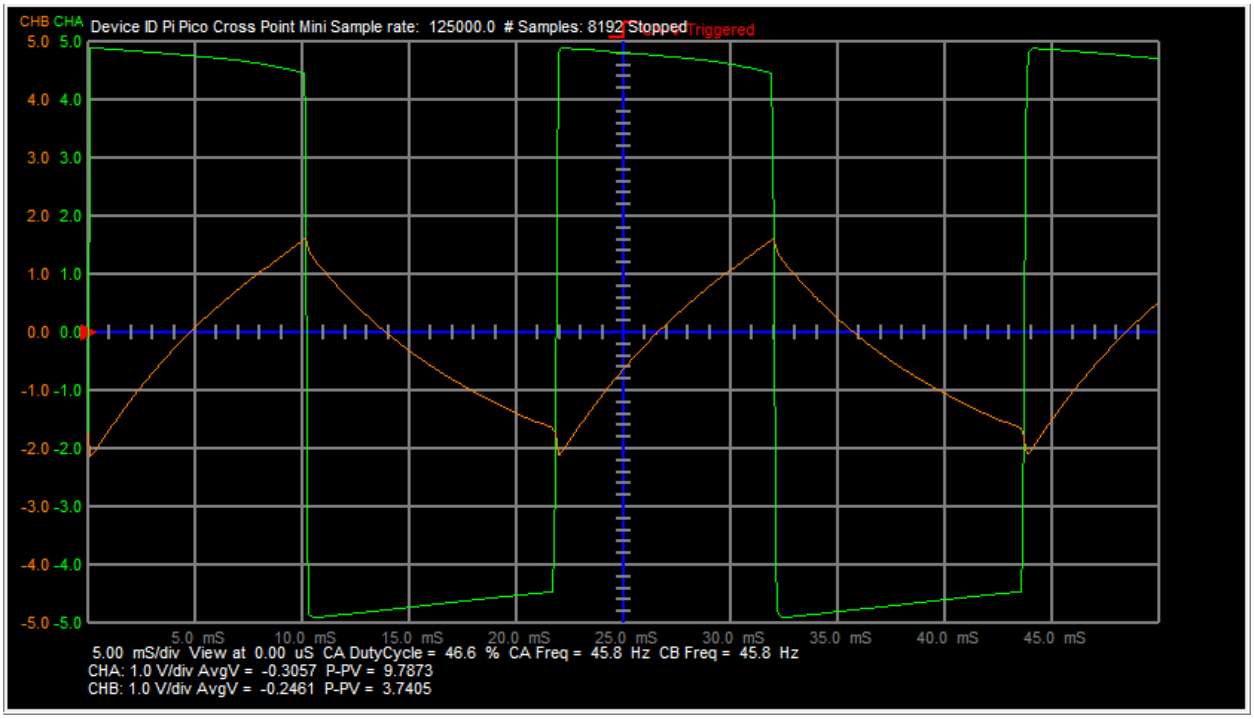



Figure 10, Pi Pico Scope traces for nodes JP3 and JP1.

The CD4007 CMOS transistor arrays can also be used to construct analog circuits such as this two stage OTA, Figure 11.

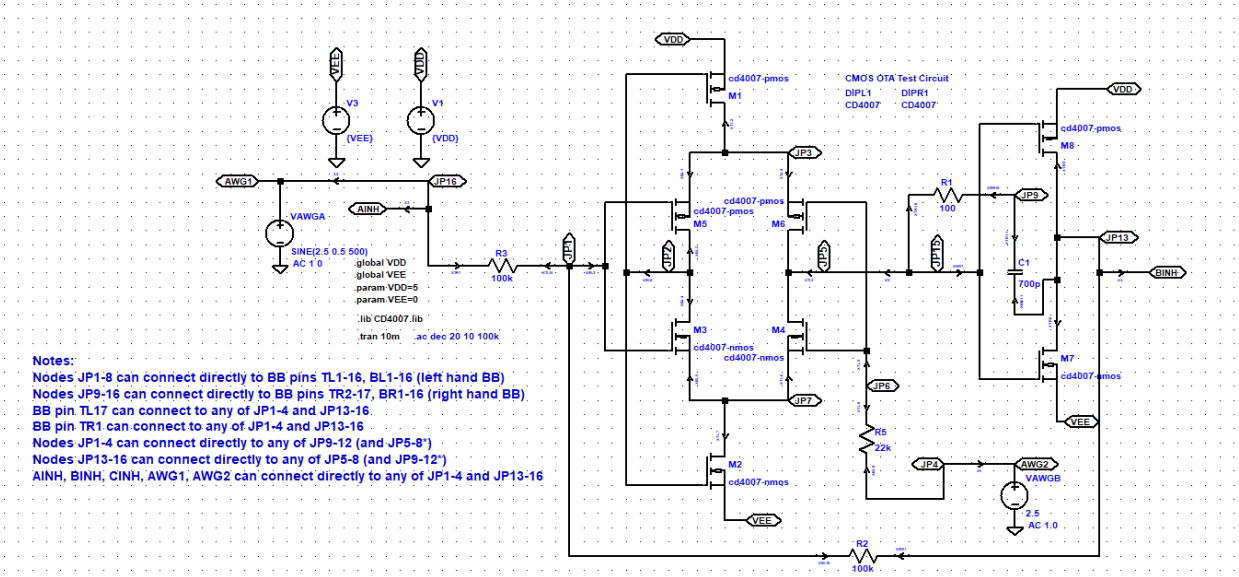


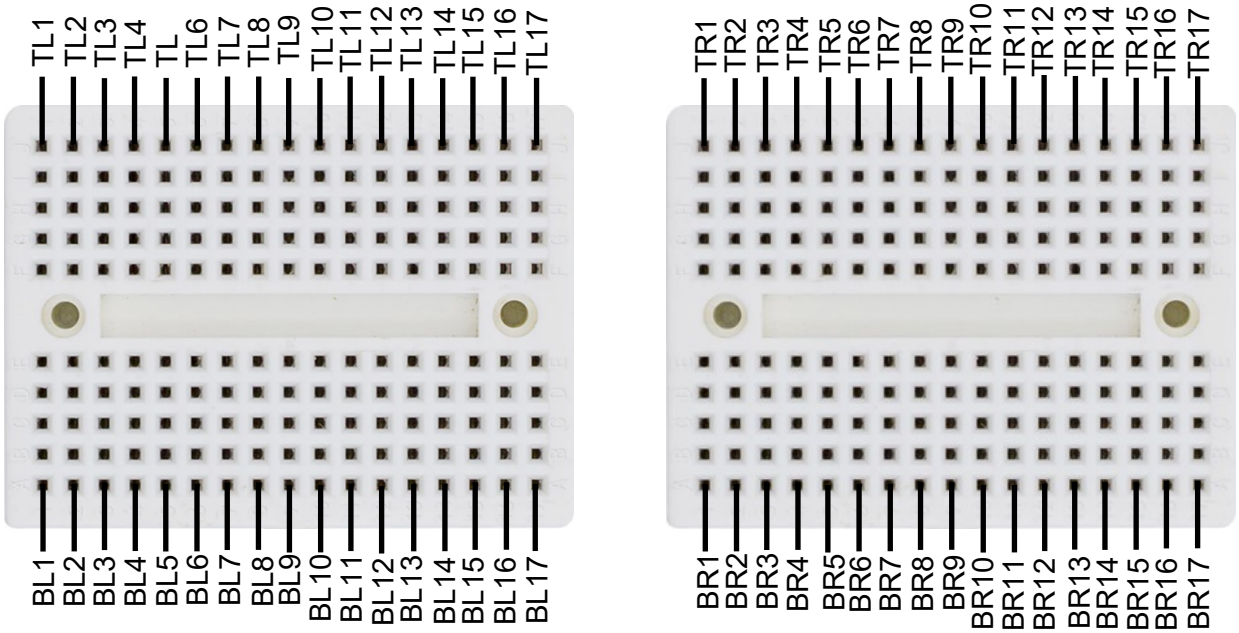

Figure 11, Two stage CMOS OTA.

**References:**


[1] Jumperless breadboard product, https://www.tindie.com/products/architeuthisflux/jumperless/ , https://github.com/Architeuthis-Flux/Jumperless
[2] CH446DS1 datasheet, https://www.wch-ic.com/downloads/CH446DS1_PDF.html
[3] Pi Pico, https://www.digikey.com/en/products/detail/raspberry-pi/SC0915/13684020?utm_adgroup=&gad_source=1
[4] LTspice, https://www.analog.com/en/resources/design-tools-and-calculators/ltspice-simulator.html
[5] ALICE Universal, https://github.com/damercer/Universal-ALICE

**Additional Notes:**

Software Configurable Solderless Breadboard Connections




**Mini Solderless Breadboard Pin Names (Red)**

Notes:

Switch Nodes JP1-8 can connect directly to BB pins TL1-16, BL1-16 (left hand BB)
Switch Nodes JP9-16 can connect directly to BB pins TR2-17, BR1-16 (right hand BB)
BB pin TL17 can connect to any of JP1-4 and JP13-16
BB pin TR1 can connect to any of JP1-4 and JP13-16
Switch Nodes JP1-4 can connect directly to any of JP9-12 (and JP5-8*)
Switch Nodes JP13-16 can connect directly to any of JP5-8 (and JP9-12*)
AINH, BINH, CINH, AWG1, AWG2 can connect directly to any of JP1-4 and JP13-16

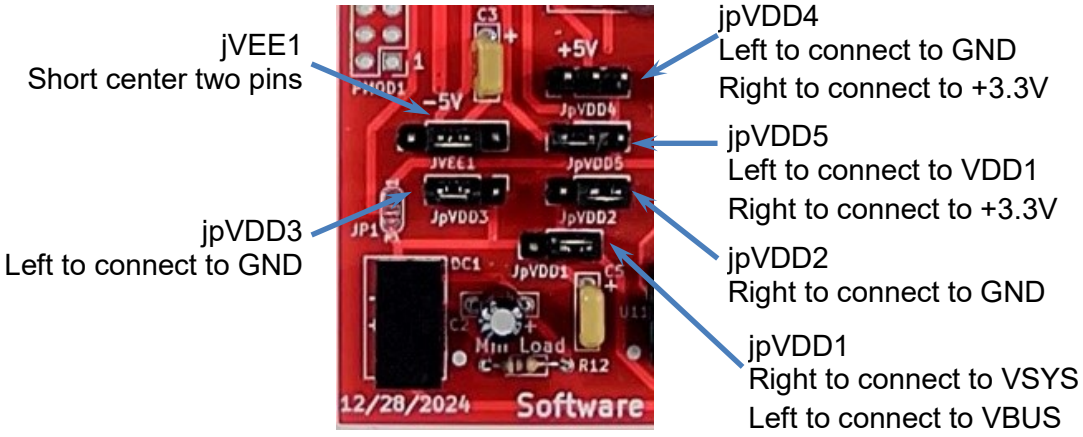
BL17 and BR17 normally default as open circuit but can be optionally connected to -5 V power rail using solder jumpers marked JP3 and JP4 on the underside of the board.

Power Rail Jumper Configuration:

The standard Pi Pico pinout has two possible positive voltages supplied from the USB port. The VBUS pin is directly connected to the USB connector +5V. The VSYS pin has a diode in series with USB connector +5V. The board has 6 jumper locations that are used to configure and distribute voltages on the board. The analog switches are powered from the VDD1 positive voltage trace (+5V) and VEE1 negative voltage trace (-5V). How VDD1 and VEE1 are configured is determined by how the jumpers are shorted.

Jumper jpVDD1 (see picture below) is a three pin jumper where the center pin can be shorted to either the left or right pin. Installing a short between center and left pin connects VDD1 to VBUS. Installing a short between center and right pin connects VDD1 to VSYS.

The on board isolated DC/DC converter is powered directly from the VBUS pin. The isolated 5V output can be connected two ways using Jumpers jpVDD2 and jpVDD3. The positive output terminal on the center pin of jpVDD2 can be connected to ground by shoring it to the right pin (GND) or the VDD1 trace by shorting it to the left pin. When the positive output terminal is connected to ground the output negative terminal becomes  -5V with respect to ground and is connected to the center pin of jumper jpVDD3.  This -5V can be connected to VEE1 by shorting the center pin to the left pin.




The board has four power distribution rails. Two on the top and two on the bottom. The lower of the two top power rails is always connected to GND. The pins of jumper jpVDD5 determine what voltage supplies the upper half of the top rail. The center pin of jpVDD5 is connected to the upper half of the top rail. Shorting the left pin to the center connects to VDD1 and shorting the right pin to the center connects to the +3.3V supplied by the Pi Pico on board LDO.

Four pin jumper jVEE1 determines the voltage supplied to the lower of the two bottom power rails. Shorting the two center pins connects it to the VEE1 (generally -5V). Three pin jumper jpVDD4 determines the voltage supplied to the upper of the two bottom power rails. Shorting the left pin to center pin connects to GND. Shorting the right pin to center pin connects to +3.3V.