1. Description

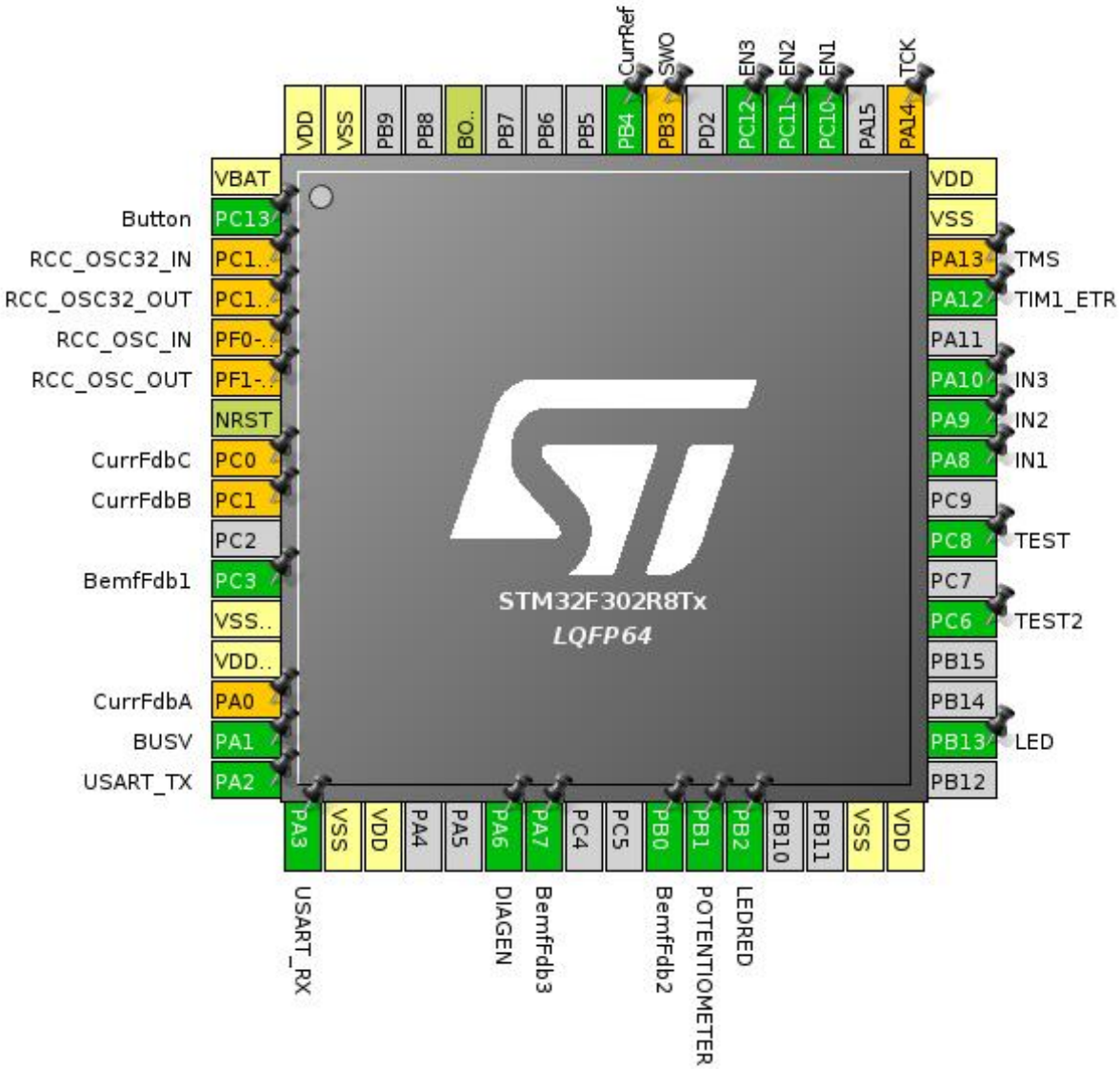
1.1. Project

Project Name	BLDC_DRIVE
Board Name	NUCLEO-F302R8
Generated with:	STM32CubeMX 4.17.0
Date	11/12/2016

1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F302
MCU name	STM32F302R8Tx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



3. Pins Configuration

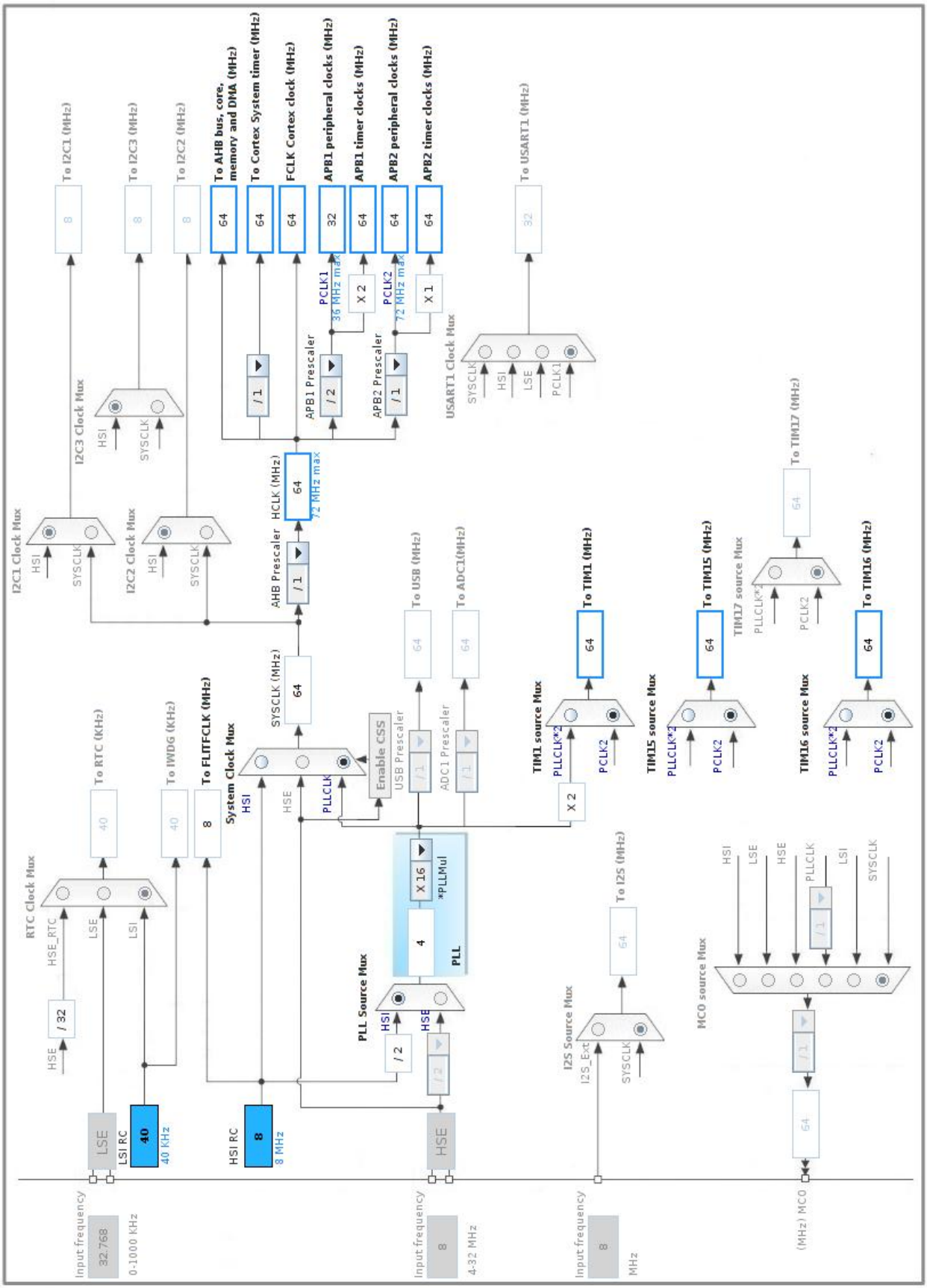
Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	Button
3	PC14 - OSC32_IN *	I/O	RCC_OSC32_IN	
4	PC15 - OSC32_OUT *	I/O	RCC_OSC32_OUT	
5	PF0-OSC_IN *	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT *	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0 *	I/O	ADC1_IN6	CurrFdbC
9	PC1 *	I/O	ADC1_IN7	CurrFdbB
11	PC3	I/O	ADC1_IN9	BemfFdb1
12	VSSA/VREF-	Power		
13	VDDA/VREF+	Power		
14	PA0 *	I/O	ADC1_IN1	CurrFdbA
15	PA1	I/O	ADC1_IN2	BUSV
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
22	PA6 **	I/O	GPIO_Input	DIAGEN
23	PA7	I/O	ADC1_IN15	BemfFdb3
26	PB0	I/O	ADC1_IN11	BemfFdb2
27	PB1	I/O	ADC1_IN12	POTENTIOMETER
28	PB2 **	I/O	GPIO_Output	LEDRED
31	VSS	Power		
32	VDD	Power		
34	PB13 **	I/O	GPIO_Output	LED
37	PC6 **	I/O	GPIO_Output	TEST2
39	PC8 **	I/O	GPIO_Output	TEST
41	PA8	I/O	TIM1_CH1	IN1
42	PA9	I/O	TIM1_CH2	IN2
43	PA10	I/O	TIM1_CH3	IN3
45	PA12	I/O	TIM1_ETR	
46	PA13 *	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14 *	I/O	SYS_JTCK-SWCLK	TCK

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
51	PC10 **	I/O	GPIO_Output	EN1
52	PC11 **	I/O	GPIO_Output	EN2
53	PC12 **	I/O	GPIO_Output	EN3
55	PB3 *	I/O	SYS_JTDO-TRACESWO	SWO
56	PB4	I/O	TIM16_CH1	CurrRef
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

** The pin is affected with an I/O function

* The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

IN2: IN2 Single-ended
IN9: IN9 Single-ended
IN11: IN11 Single-ended
IN12: IN12 Single-ended
mode: IN15

5.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	**Synchronous clock mode divided by 1 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**5 ***
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 12 ***
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0
Rank	**2 ***
Channel	**Channel 9 ***
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0
Rank	**3 ***

Channel	**Channel 11 ***
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0
Rank	**4 ***
Channel	**Channel 15 ***
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0
Rank	**5 ***
Channel	Channel 2
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.2. SYS

Timebase Source: SysTick

5.3. TIM1

Clock Source : Internal Clock
Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Use ETR as Clearing Source: ETR IO as Clearing Source

5.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Input Source ETR
Clear Input Polarity	Non inverted
Clear Input Prescaler	No division
Clear Input Filter	0
Clear Channel 1	**Enable ***
Clear Channel 2	**Enable ***
Clear Channel 3	**Enable ***

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

5.4. TIM2

Clock Source : Internal Clock

5.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**640 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**1199 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

5.5. TIM15

mode: Clock Source

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**9999 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1129 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.6. TIM16

mode: Activated

Channel1: PWM Generation CH1

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**499 ***
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

5.7. USART2

Mode: Asynchronous

5.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	**576000 ***

Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC3	ADC1_IN9	Analog mode	No pull up pull down	n/a	BemfFdb1
	PA1	ADC1_IN2	Analog mode	No pull up pull down	n/a	BUSV
	PA7	ADC1_IN15	Analog mode	No pull up pull down	n/a	BemfFdb3
	PB0	ADC1_IN11	Analog mode	No pull up pull down	n/a	BemfFdb2
	PB1	ADC1_IN12	Analog mode	No pull up pull down	n/a	POTENTIOMETER
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull up pull down	Low	IN1
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull up pull down	Low	IN2
	PA10	TIM1_CH3	Alternate Function Push Pull	No pull up pull down	Low	IN3
	PA12	TIM1_ETR	Alternate Function Push Pull	No pull up pull down	Low	
TIM16	PB4	TIM16_CH1	Alternate Function Push Pull	No pull up pull down	Low	CurrRef
USART2	PA2	USART2_TX	Alternate Function Push Pull	*	Low	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	*	Low	USART_RX
Single Mapped Signals	PC14 - OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15 - OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
	PC0	ADC1_IN6	Analog mode	No pull up pull down	n/a	CurrFdbC
	PC1	ADC1_IN7	Analog mode	No pull up pull down	n/a	CurrFdbB
	PA0	ADC1_IN1	Analog mode	No pull up pull down	n/a	CurrFdbA
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
	PB3	SYS_JTDO-TRACESWO	n/a	n/a	n/a	SWO
GPIO	PC13	GPIO_EXTI13	**External Interrupt Mode with Falling edge trigger detection**	No pull up pull down	n/a	Button
	PA6	GPIO_Input	Input mode	No pull up pull down	n/a	DIAGEN
	PB2	GPIO_Output	Output Push Pull	No pull up pull down	Low	LEDRED
	PB13	GPIO_Output	Output Push Pull	No pull up pull down	Low	LED

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC6	GPIO_Output	Output Push Pull	No pull up pull down	Low	TEST2
	PC8	GPIO_Output	Output Push Pull	No pull up pull down	Low	TEST
	PC10	GPIO_Output	Output Push Pull	No pull up pull down	Low	EN1
	PC11	GPIO_Output	Output Push Pull	No pull up pull down	Low	EN2
	PC12	GPIO_Output	Output Push Pull	No pull up pull down	Low	EN3

6.2. DMA configuration

DMA request	Stream	Direction	Priority
USART2_TX	DMA1_Channel7	Memory To Peripheral	Low
USART2_RX	DMA1_Channel6	Peripheral To Memory	Low
ADC1	DMA1_Channel1	Peripheral To Memory	Low

USART2_TX: DMA1_Channel7 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_RX: DMA1_Channel6 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel6 global interrupt	true	0	0
DMA1 channel7 global interrupt	true	0	0
ADC1 interrupt	true	0	0
TIM1 break and TIM15 interrupts	true	0	0
TIM2 global interrupt	true	1	0
USART2 global interrupt	true	3	0
EXTI line[15:10] interrupts	true	0	0
PVD interrupt through EXTI line16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 update and TIM16 interrupts	unused		
TIM1 trigger, commutation and TIM17 interrupts	unused		
TIM1 capture compare interrupt	unused		
Floating point unit interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F3
Line	STM32F302
MCU	STM32F302R8Tx
Datasheet	025147_Rev5

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	BLDC_DRIVE
Project Folder	/home/damian/stm32/BLDC_DRIVE
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F3 V1.6.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No