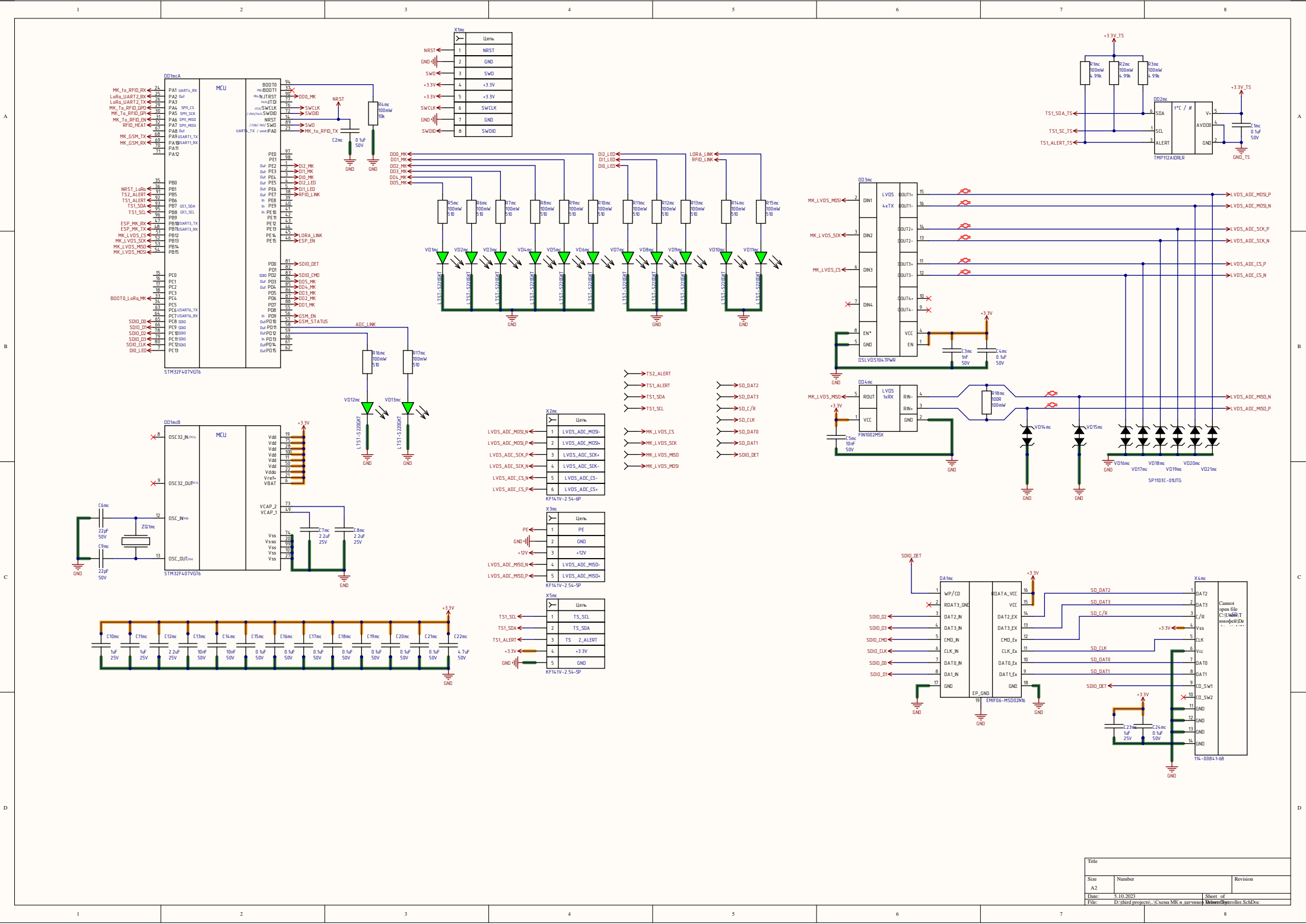
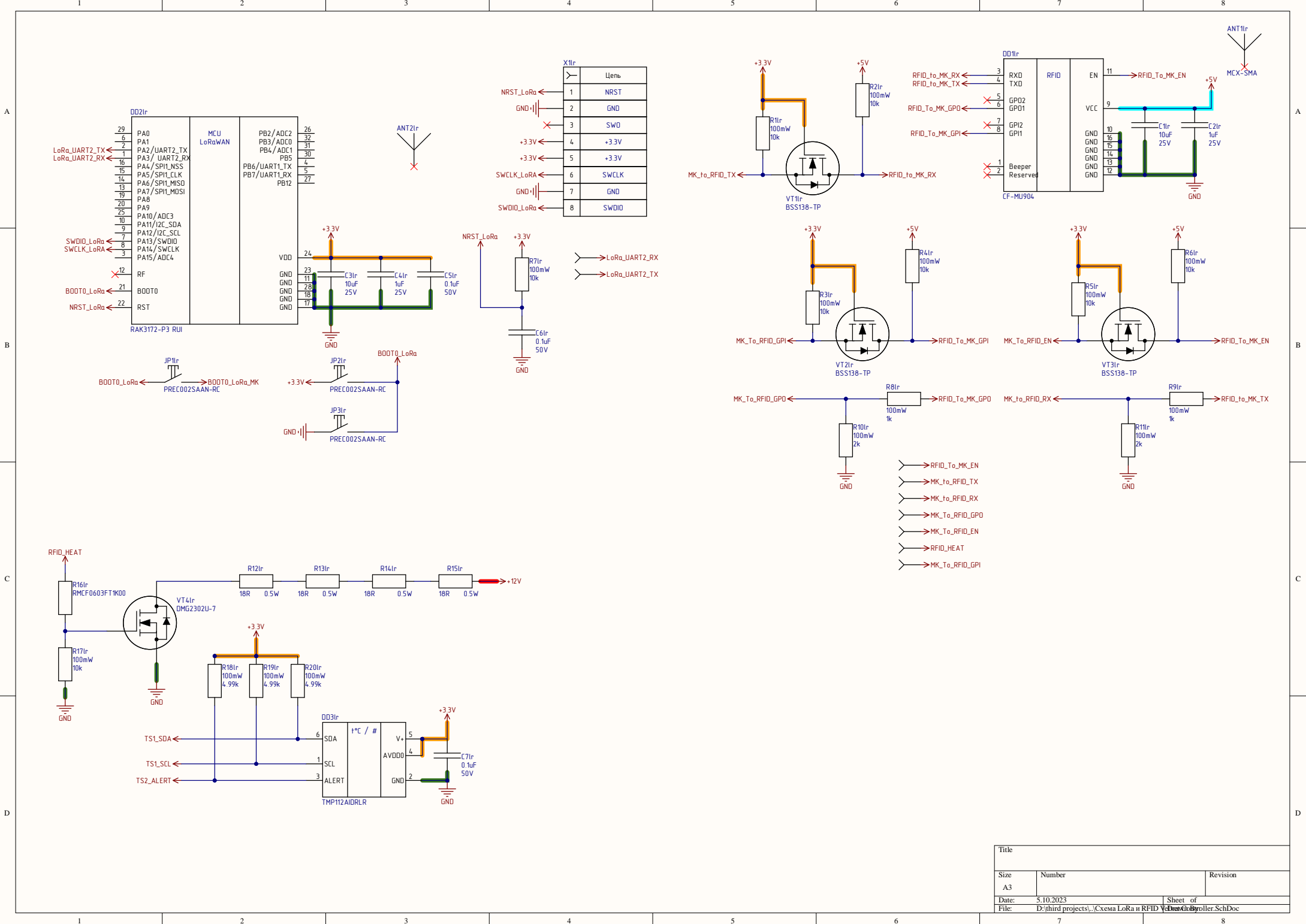


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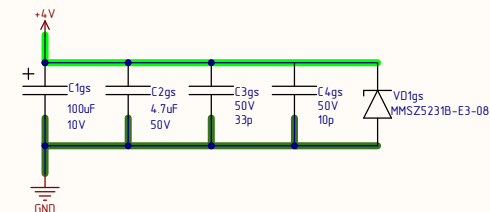
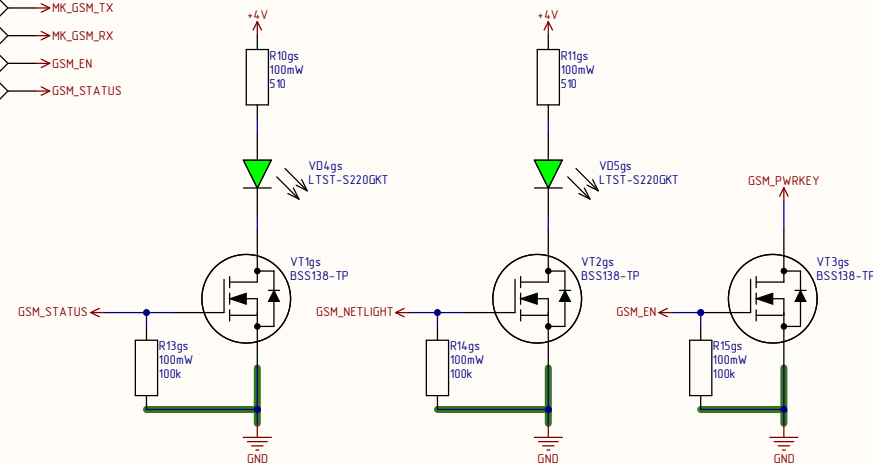
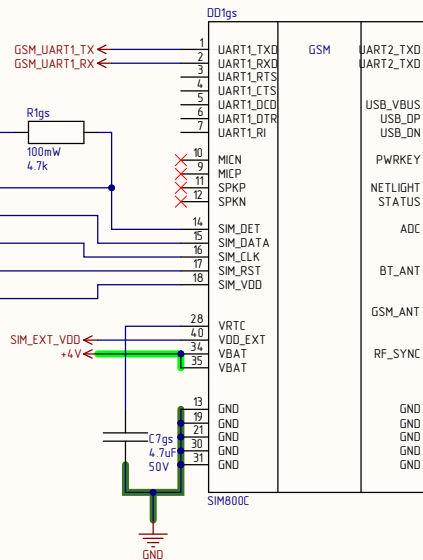
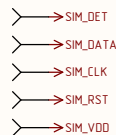
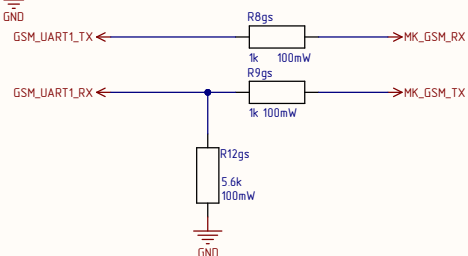


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XS1gs	
Uem	SW
DETECT	C7
I/O	C3
CLK	C2
RST	C1
Vdd	C6
Vpp	C4
RFU	C8
RFU	C5
GND	1
FREE PAD	2
FREE PAD	3
FREE PAD	4
FREE PAD	5

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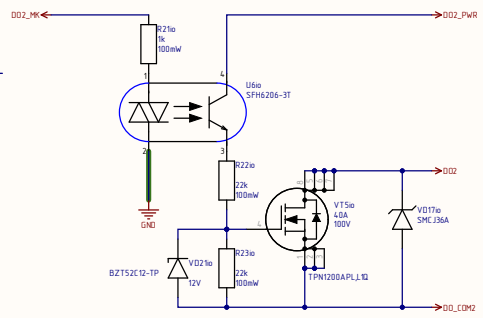
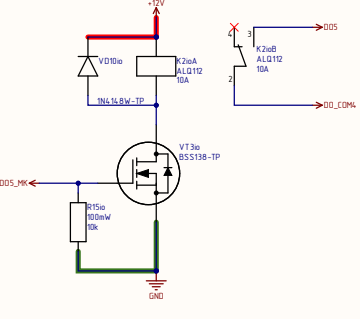
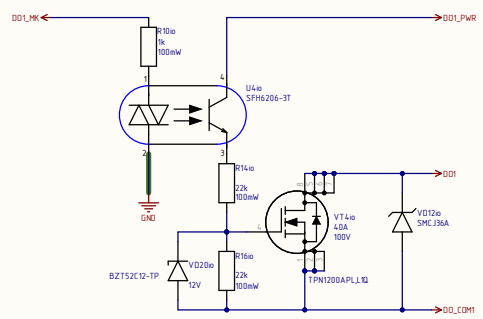
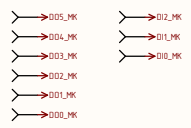
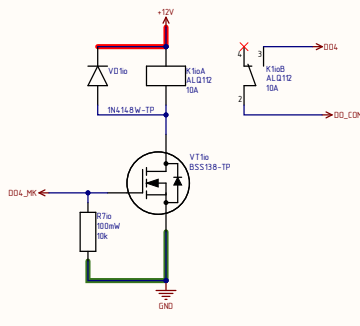
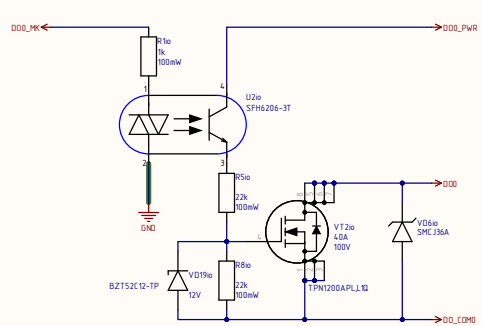
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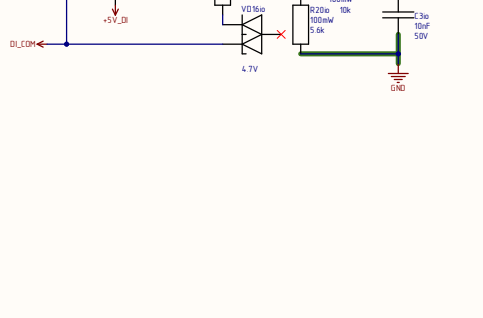
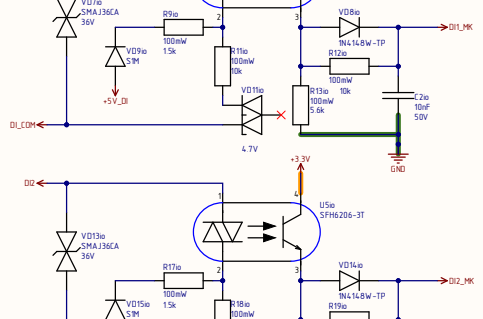
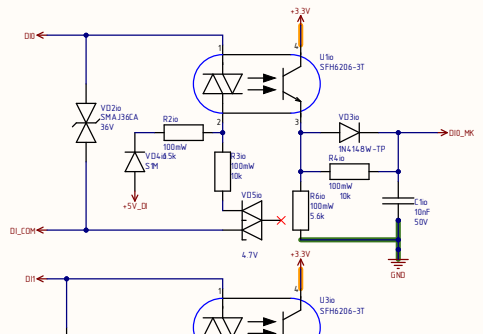
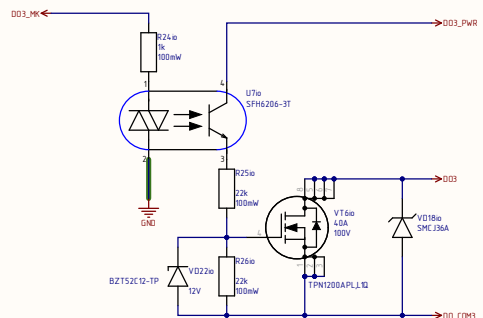
D



X1a	U1a
1	+PwR
2	-PwR
3	PE
4	D0
5	D01
6	D02
7	D0_C00B
8	+5V_D

X2a	U2a
1	GND_D
2	D00_PwR
3	D00
4	D0_C00B
5	D01_PwR
6	D01
7	D0_C00B
8	D02_PwR

X3a	U3a
1	D02
2	D0_C00B
3	D03_PwR
4	D03
5	D0_C00B
6	D0_C00B
7	D04
8	D05



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