



# TPS6303x High Efficiency Single Inductor Buck-Boost Converter With 1-A Switches

## 1 Features

- Input Voltage Range: 1.8 V to 5.5 V
- Fixed and Adjustable Output Voltage Options from 1.2 V to 5.5 V
- Up to 96% Efficiency
- 800-mA Output Current at 3.3 V in Step-Down Mode ( $V_{IN} = 3.6 \text{ V to } 5.5 \text{ V}$ )
- Up to 500-mA Output Current at 3.3 V in Boost Mode ( $V_{IN} > 2.4 \text{ V}$ )
- Automatic Transition Between Step-Down and Boost Mode
- Device Quiescent Current less than 50  $\mu\text{A}$
- Power-Save Mode for Improved Efficiency at Low Output Power
- Forced Fixed Frequency Operation and Synchronization Possible
- Load Disconnect During Shutdown
- Overtemperature Protection
- Available in a Small 2.5-mm  $\times$  2.5-mm 10-Pin VSON Package (QFN)

## 2 Applications

- All Two-Cell and Three-Cell Alkaline, NiCd or NiMH or Single-Cell Li Battery Powered Products
- Portable Audio Players
- Mobile Phones
- Personal Medical Products
- White LEDs

## 3 Description

The TPS6303x devices provide a power supply solution for products powered by either a two-cell or three-cell alkaline, NiCd or NiMH battery, or a one-cell Li-ion or Li-polymer battery. Output currents can go as high as 600 mA while using a single-cell Li-ion or Li-polymer battery, and discharge it down to 2.5 V or lower. The buck-boost converter is based on a fixed frequency, pulse width modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. At low load currents, the converter enters power-save mode to maintain high efficiency over a wide load current range. The power-save mode can be disabled, forcing the converter to operate at a fixed switching frequency. The maximum average current in the switches is limited to a typical value of 1000 mA. The output voltage is programmable using an external resistor divider, or is fixed internally on the chip. The converter can be disabled to minimize battery drain. During shutdown, the load is disconnected from the battery.

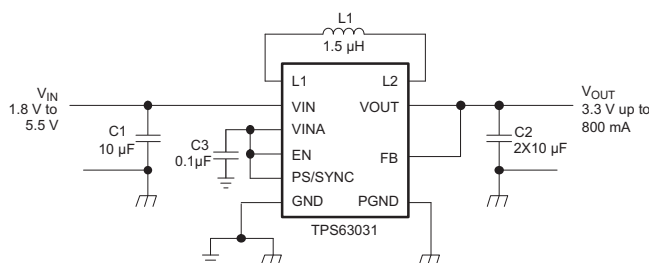
The TPS6303x devices operate over a free air temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The devices are packaged in a 10-pin VSON package measuring 2.5 mm  $\times$  2.5 mm (DSK).

### Device Information<sup>(1)</sup>

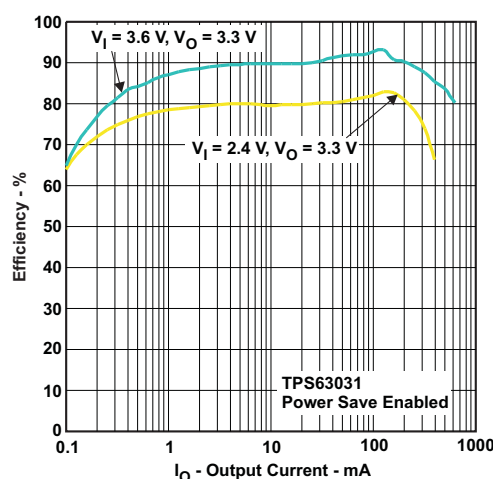
| PART NUMBER          | PACKAGE   | BODY SIZE (NOM)          |
|----------------------|-----------|--------------------------|
| TPS63030<br>TPS63031 | VSON (10) | 2.50 mm $\times$ 2.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Typical Application Schematic



### Efficiency vs Output Current



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

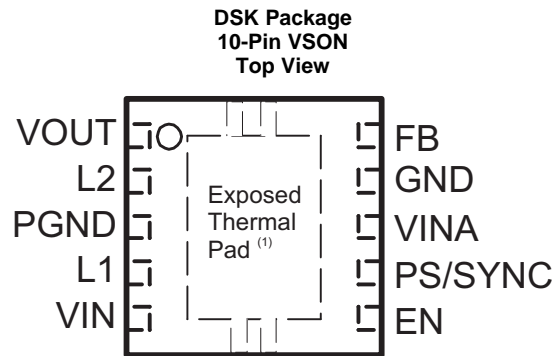
| Changes from Revision B (March 2012) to Revision C  | Page |
|---|------|
| <ul style="list-style-type: none"> <li>Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section</li> </ul> | 1    |

## 5 Output Voltage Options<sup>(1)</sup>

| OUTPUT VOLTAGE<br>DC/DC | PACKAGE MARKING | PACKAGE     | PART NUMBER <sup>(1)</sup> |
|-------------------------|-----------------|-------------|----------------------------|
| Adjustable              | CEE             | 10-Pin VSON | TPS63030DSK                |
| 3.3 V                   | CEF             |             | TPS63031DSK                |

- (1) Contact the factory to check availability of other fixed output voltage versions.  
(1) The DSK package is available taped and reeled. Add R suffix to device type (for example, TPS63030DSKR) to order quantities of 3000 devices per reel. Add T suffix to device type (for example, TPS63030DSKT) to order quantities of 250 devices per reel.

## 6 Pin Configuration and Functions



- (1) The exposed thermal pad is connected to PGND.

### Pin Functions

| PIN                 |     | I/O | DESCRIPTION   |
|---------------------|-----|-----|---|
| NAME                | NO. |     |   |
| EN                  | 6   | IN  | Enable input (1 enabled, 0 disabled)  |
| FB                  | 10  | IN  | Voltage feedback of adjustable versions, must be connected to VOUT on fixed output voltage versions |
| GND                 | 9   | —   | Control / logic ground  |
| L1                  | 4   | IN  | Connection for inductor   |
| L2                  | 2   | IN  | Connection for inductor   |
| PGND                | 3   | —   | Power ground  |
| PS/SYNC             | 7   | IN  | Enable / disable power save mode (1 disabled, 0 enabled, clock signal for synchronization)          |
| VIN                 | 5   | IN  | Supply voltage for power stage  |
| VINA                | 8   | IN  | Supply voltage for control stage  |
| VOUT                | 1   | OUT | Buck-boost converter output   |
| Exposed Thermal Pad | —   | —   | The exposed thermal pad is connected to PGND.   |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|  | MIN  | MAX | UNIT |
|--|------|-----|------|
| Input voltage on VIN, VINA, L1, L2, VOUT, ILIM, EN, FB, SS | −0.3 | 7   | V    |
| Operating virtual junction temperature, T <sub>J</sub>     | −40  | 150 | °C   |
| Storage temperature, T <sub>stg</sub>                      | −65  | 150 | °C   |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

|                    |                         | VALUE  | UNIT |
|--------------------|-------------------------|--|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | 2000 |
|                    |                         | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | 1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

|  | MIN | MAX | UNIT |
|--|-----|-----|------|
| Supply voltage at VIN, VINA                            | 1.8 | 5.5 | V    |
| Operating free air temperature, T <sub>A</sub>         | −40 | 85  | °C   |
| Operating virtual junction temperature, T <sub>J</sub> | −40 | 125 | °C   |

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | TPS6303x   | UNIT |
|-------------------------------|--|------------|------|
|                               |  | DSK (VSON) |      |
|                               |  | 10 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 60.7       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | —          | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 26         | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | —          | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | —          | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 6.3        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

| PARAMETER                                  |                                    |                                      | TEST CONDITIONS   |  | MIN   | TYP  | MAX   | UNIT |
|--|------------------------------------|--------------------------------------|---|--|-------|------|-------|------|
| DC/DC STAGE                                |                                    |                                      |   |  |       |      |       |      |
| V <sub>IN</sub>                            | Input voltage range                |                                      |   |  | 1.8   |      | 5.5   | V    |
| V <sub>IN</sub>                            | Minimum input voltage for start-up |                                      | 0°C ≤ T <sub>A</sub> ≤ 85°C   |  | 1.6   | 1.8  | 1.9   | V    |
| V <sub>IN</sub>                            | Minimum input voltage for start-up |                                      |   |  | 1.6   | 1.8  | 2.0   | V    |
| V <sub>OUT</sub>                           | TPS63030 output voltage range      |                                      |   |  | 1.2   |      | 5.5   | V    |
| Minimum duty cycle in step-down conversion |                                    |                                      |   |  |       | 30%  | 40%   |      |
| V <sub>FB</sub>                            | TPS63030 feedback voltage          |                                      | PS/SYNC = V <sub>IN</sub>   |  | 495   | 500  | 505   | mV   |
|  | TPS63031 output voltage            |                                      |   |  | 3.267 | 3.3  | 3.333 | V    |
| V <sub>FB</sub>                            | TPS63030 feedback voltage          |                                      | PS/SYNC = GND Referenced to 500 mV  |  | -3%   |      | +6%   |      |
|  | TPS63031 output voltage            |                                      | PS/SYNC = GND Referenced to 3.3 V   |  | -3%   |      | +6%   |      |
| f  | Oscillator frequency               |                                      |   |  | 2200  | 2400 | 2600  | kHz  |
| Frequency range for synchronization        |                                    |                                      |   |  | 2200  | 2400 | 2600  | kHz  |
| I <sub>SW</sub>                            | Average switch current limit       |                                      | V <sub>IN</sub> = V <sub>INA</sub> = 3.6 V, T <sub>A</sub> = 25°C   |  | 900   | 1000 | 1100  | mA   |
| High-side switch ON-resistance             |                                    |                                      | V <sub>IN</sub> = V <sub>INA</sub> = 3.6 V  |  |       | 200  |       | mΩ   |
| Low-side switch ON-resistance              |                                    |                                      | V <sub>IN</sub> = V <sub>INA</sub> = 3.6 V  |  |       | 200  |       | mΩ   |
| Maximum line regulation                    |                                    |                                      |   |  |       | 0.5% |       |      |
| Maximum load regulation                    |                                    |                                      |   |  |       | 0.5% |       |      |
| I <sub>q</sub>                             | Quiescent current                  | V <sub>IN</sub> and V <sub>INA</sub> | I <sub>OUT</sub> = 0 mA, V <sub>EN</sub> = V <sub>IN</sub> = V <sub>INA</sub> = 3.6 V, V <sub>OUT</sub> = 3.3 V |  |       | 25   | 35    | μA   |
|  |                                    | V <sub>OUT</sub>                     |   |  |       | 4    | 6     | μA   |
| TPS63031 FB input impedance                |                                    |                                      | V <sub>EN</sub> = HIGH  |  |       | 1    |       | MΩ   |
| I <sub>S</sub>                             | Shutdown current                   |                                      | V <sub>EN</sub> = 0 V, V <sub>IN</sub> = V <sub>INA</sub> = 3.6 V   |  |       | 0.1  | 0.9   | μA   |
| CONTROL STAGE                              |                                    |                                      |   |  |       |      |       |      |
| V <sub>UVLO</sub>                          | Under voltage lockout threshold    |                                      | V <sub>INA</sub> voltage decreasing   |  | 1.4   | 1.5  | 1.6   | V    |
| V <sub>IL</sub>                            | EN, PS/SYNC input low voltage      |                                      |   |  |       |      | 0.4   | V    |
| V <sub>IH</sub>                            | EN, PS/SYNC input high voltage     |                                      |   |  | 1.2   |      |       | V    |
| EN, PS/SYNC input current                  |                                    |                                      | Clamped on GND or V <sub>INA</sub>  |  |       | 0.01 | 0.1   | μA   |
| Overtemperature protection                 |                                    |                                      |   |  |       | 140  |       | °C   |
| Overtemperature hysteresis                 |                                    |                                      |   |  |       | 20   |       | °C   |

## 7.6 Typical Characteristics

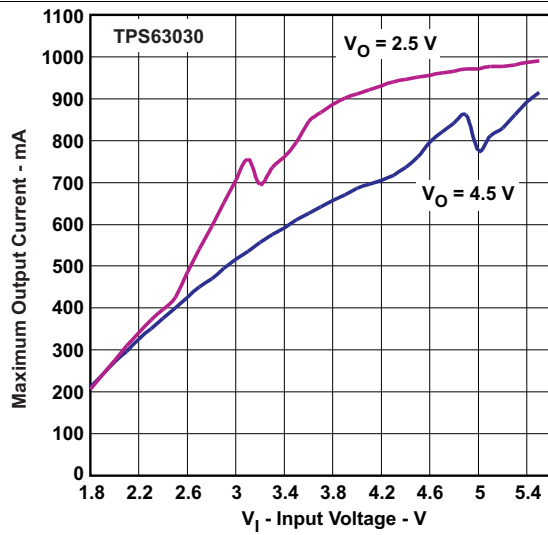


Figure 1. Maximum Output Current vs Input Voltage, TPS63030

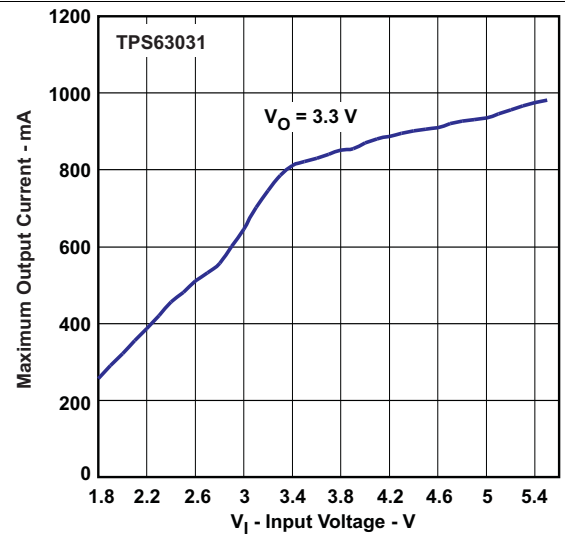
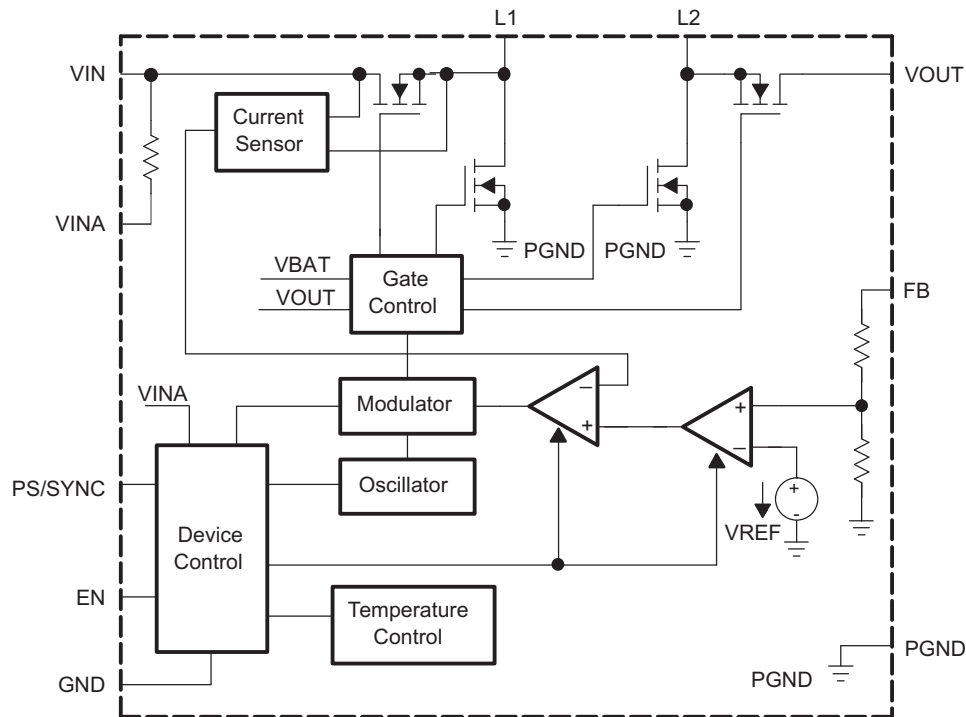


Figure 2. Maximum Output Current vs Input Voltage, TPS63031







## 8.4 Device Functional Modes

### 8.4.1 Soft-Start and Short Circuit Protection

After being enabled, the device starts operating. The average current limit ramps up from an initial 400 mA following the output voltage increasing. At an output voltage of about 1.2 V, the current limit is at its nominal value. If the output voltage does not increase, the current limit will not increase. There is no timer implemented. Thus the output voltage overshoot at start-up, as well as the inrush current, is kept at a minimum. The device ramps up the output voltage in a controlled manner even if a very large capacitor is connected at the output. When the output voltage does not increase above 1.2 V, the device assumes a short circuit at the output and keeps the current limit low to protect itself and the application. At a short at the output during operation the current limit also will be decreased accordingly. At 0 V at the output, for example, the output current will not exceed about 400 mA.

### 8.4.2 Buck-Boost Operation

To regulate the output voltage properly at all possible input voltage conditions, the device automatically switches from step-down operation to boost operation and back as required by the configuration. It always uses one active switch, one rectifying switch, one switch permanently on, and one switch permanently off. Therefore, it operates as a step-down converter (buck) when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all 4 switches are permanently switching. Controlling the switches this way allows the converter to maintain high efficiency at the most important point of operation, when input voltage is close to the output voltage. The RMS current through the switches and the inductor is kept at a minimum, to minimize switching and conduction losses. Switching losses are also kept low by using only one active and one passive switch. For the remaining 2 switches, one is kept permanently on and the other is kept permanently off, thus causing no switching losses.

### 8.4.3 Power-Save Mode and Synchronization

The PS/SYNC pin can be used to select different operation modes. To enable power-save, PS/SYNC must be set low. Power-save mode is used to improve efficiency at light load. If power-save mode is enabled, the converter stops operating if the average inductor current gets lower than about 100 mA and the output voltage is at or above its nominal value. If the output voltage decreases below its nominal value, the device ramps up the output voltage again by starting operation using a programmed average inductor current higher than required by the current load condition. Operation can last for one or several pulses. The converter again stops operating once the conditions for stopping operation are met again.

The power save mode can be disabled by programming high at the PS/SYNC. Connecting a clock signal at PS/SYNC forces the device to synchronize to the connected clock frequency. Synchronization is done by a phase-locked loop (PLL), so synchronizing to lower and higher frequencies compared to the internal clock works without any issues. The PLL can also tolerate missing clock pulses without the converter malfunctioning. The PS/SYNC input supports standard logic thresholds.

## 9 Application and Implementation

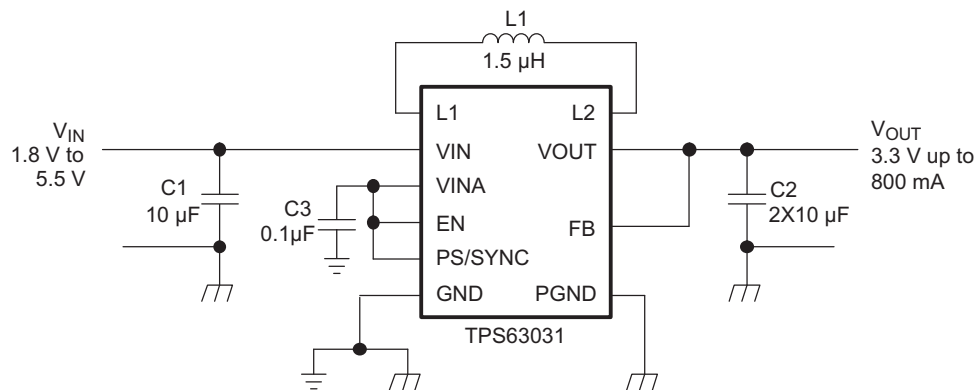
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TPS63036 is a buck-boost converter suitable for applications that need a regulated output voltage from an input supply that is higher or lower than the input supply.

### 9.2 Typical Application



**Figure 5. Typical Application Circuit for Adjustable Output Voltage Option**

#### 9.2.1 Design Requirements

The design guideline provides a component selection to operate the device within the [Recommended Operating Conditions](#).

[Table 1](#) shows the list of components for the application curves.

**Table 1. List of Components**

| REFERENCE | DESCRIPTION   | MANUFACTURER                |
|-----------|---|-----------------------------|
|           | TPS6303 0 / 1   | Texas Instruments           |
| L1        | 1.5 µH, 3 mm x 3 mm x 1.5 mm                                      | LPS3015-1R5, Coilcraft      |
| C1        | 10 µF 6.3V, 0603, X7R ceramic                                     | GRM188R60J106KME84D, Murata |
| C2        | 2 x 10 µF 6.3V, 0603, X7R ceramic                                 | GRM188R60J106KME84D, Murata |
| C3        | 0.1 µF, X7R ceramic   |                             |
| R1, R2    | Depending on the output voltage at TPS63030, not used at TPS63031 |                             |

#### 9.2.2 Detailed Design Procedure

##### 9.2.2.1 Programming the Output Voltage

Within the TPS6303x family there are fixed and adjustable output voltage versions available. To properly configure the fixed output voltage devices, the FB pin is used to sense the output voltage. This means that it must be connected directly to VOUT. At the adjustable output voltage versions, an external resistor divider is used to adjust the output voltage. The resistor divider must be connected between VOUT, FB and GND. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 500 mV. The maximum recommended value for the output voltage is 5.5 V. The current through the resistive divider should be about 100

times greater than the current into the FB pin. The typical current into the FB pin is 0.01  $\mu\text{A}$ , and the voltage across the resistor between FB and GND,  $R_2$ , is typically 500 mV. Based on those two values, the recommended value for  $R_2$  should be lower than 500 k $\Omega$ , in order to set the divider current at 1  $\mu\text{A}$  or higher. TI recommends to keep the value for this resistor in the range of 200 k $\Omega$ . From that, the value of the resistor connected between VOUT and FB,  $R_1$ , depending on the needed output voltage ( $V_{\text{OUT}}$ ), can be calculated using [Equation 1](#).

$$R_1 = R_2 \times \left( \frac{V_{\text{OUT}}}{V_{\text{FB}}} - 1 \right) \quad (1)$$

### 9.2.2.2 Inductor Selection

The inductor selection is affected by several parameter like inductor ripple current, output voltage ripple, transition point into power-save mode, and efficiency. See [Table 2](#) for typical inductors.

**Table 2. List of Recommended Inductors**

| VENDOR     | INDUCTOR SERIES |
|------------|-----------------|
| Coilcraft  | LPS3015         |
|            | EPL3010         |
| Murata     | LQH3NP          |
| Tajo Yuden | NR3015          |

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a high impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady state operation is calculated using [Equation 3](#). Only the equation which defines the switch current in boost mode is shown, because this provides the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost} \quad D = \frac{V_{\text{OUT}} - V_{\text{IN}}}{V_{\text{OUT}}} \quad (2)$$

$$I_{\text{PEAK}} = \frac{I_{\text{out}}}{\eta \times (1 - D)} + \frac{V_{\text{in}} \times D}{2 \times f \times L}$$

where

- D = Duty Cycle in Boost mode
- f = Converter switching frequency (typical 2.5MHz)
- L = Inductor value
- $\eta$  = Estimated converter efficiency (use the number from the efficiency curves or 0.90 as an assumption) (3)

#### NOTE

The calculation must be done for the minimum input voltage which is possible to have in boost mode.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. TI recommends to choose an inductor with a saturation current 20% higher than the value calculated using [Equation 3](#). Possible inductors are listed in [Table 2](#).

### 9.2.2.3 Capacitor Selection

#### 9.2.2.3.1 Input Capacitor

At least a 4.7  $\mu\text{F}$  input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended.

### 9.2.2.3.2 Bypass Capacitor

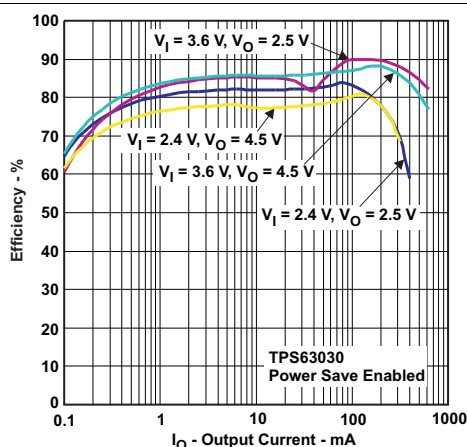
To make sure that the internal control circuits are supplied with a stable low noise supply voltage, a capacitor can be connected between VINA and GND. Using a ceramic capacitor with a value of 0.1  $\mu\text{F}$  is recommended. The value of this capacitor should not be higher than 0.22  $\mu\text{F}$ .

### 9.2.2.3.3 Output Capacitor

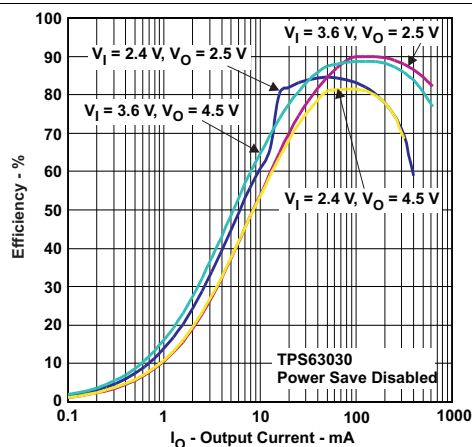
For the output capacitor, use of a small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC is recommended. The recommended nominal output capacitance value is 10  $\mu\text{F}$ .

There is also no upper limit for the output capacitance value. Larger capacitors causes lower output voltage ripple as well as lower output voltage drop during load transients.

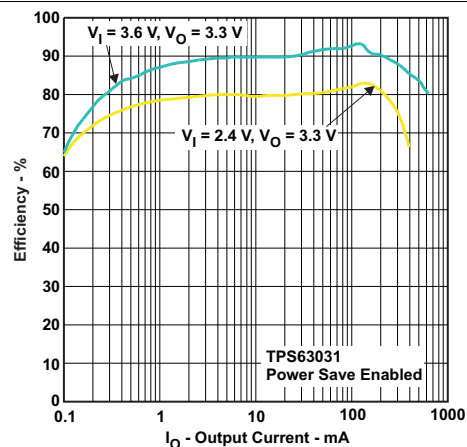
## 9.2.3 Application Curves



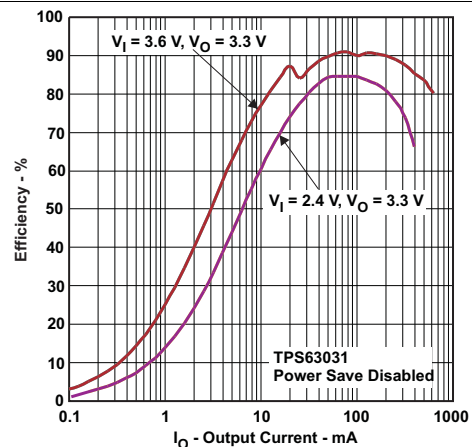
**Figure 6. Efficiency vs Output Current, TPS63030, Power-Save Enabled**



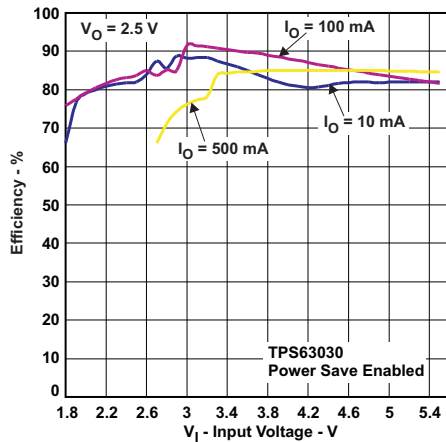
**Figure 7. Efficiency vs Output Current, TPS63030, Power-Save Disabled**



**Figure 8. Efficiency vs Output Current, TPS63031, Power-Save Enabled**

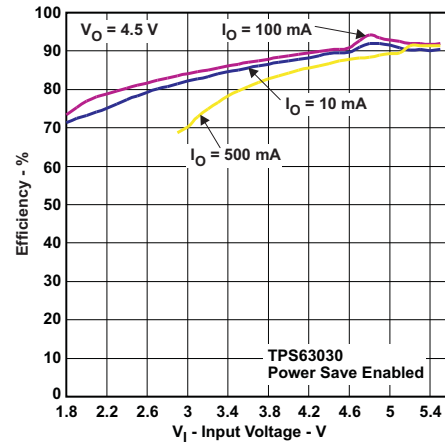


**Figure 9. Efficiency vs Output Current, TPS63031, Power-Save Disabled**



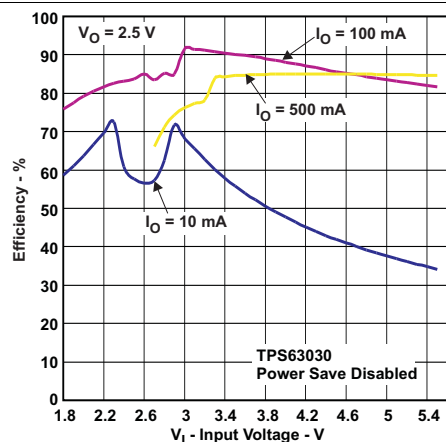
$V_{OUT} = 2.5\text{ V}$

**Figure 10. Efficiency vs Input Voltage, TPS63030, Power-Save Enabled**



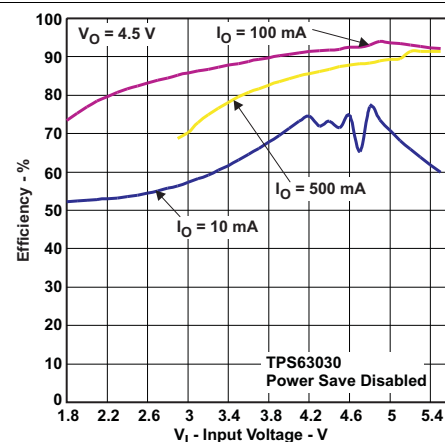
$V_{OUT} = 4.5\text{ V}$

**Figure 11. Efficiency vs Input Voltage, TPS63030, Power-Save Enabled**



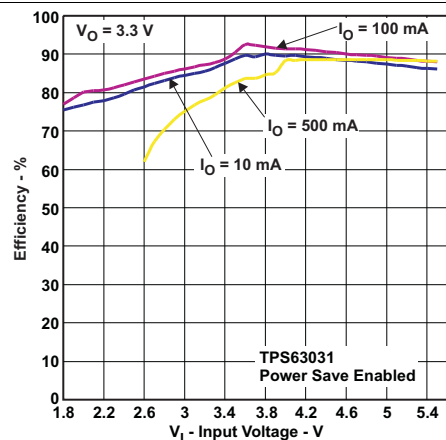
$V_{OUT} = 2.5\text{ V}$

**Figure 12. Efficiency vs Input Voltage, TPS63030, Power-Save Disabled**



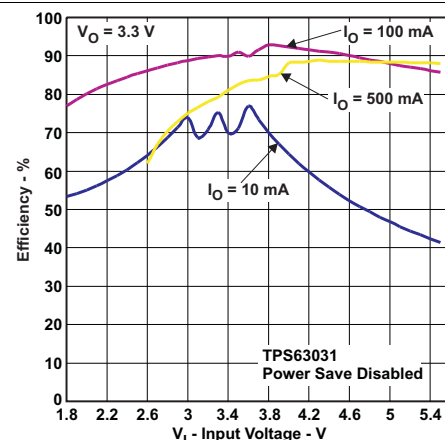
$V_{OUT} = 4.5\text{ V}$

**Figure 13. Efficiency vs Input Voltage, TPS63030, Power-Save Disabled**



$V_{OUT} = 3.3\text{ V}$

**Figure 14. Efficiency vs Input Voltage, TPS63031, Power-Save Enabled**

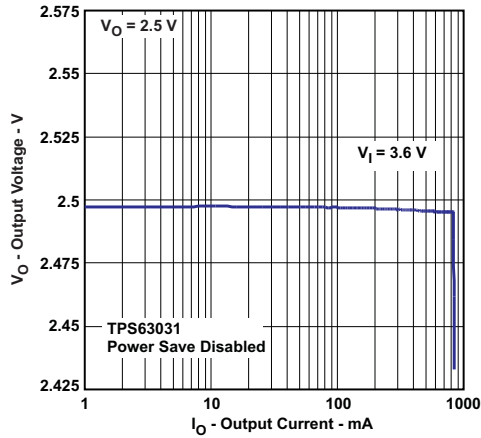
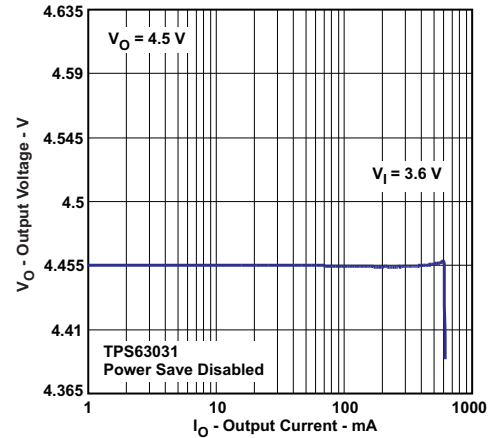
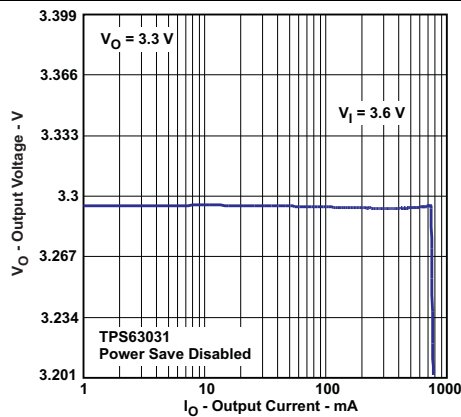
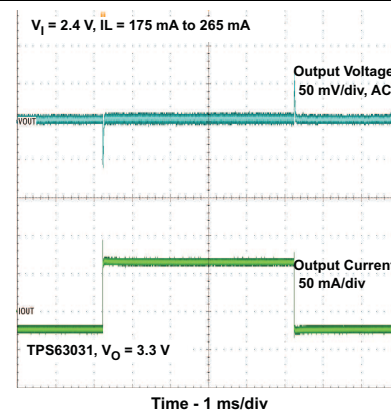
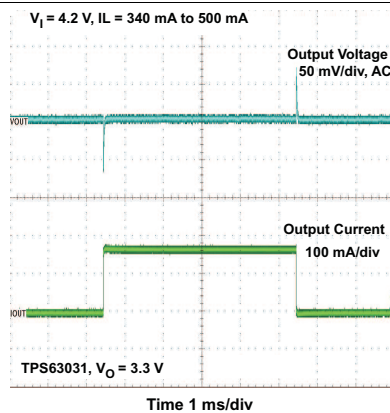
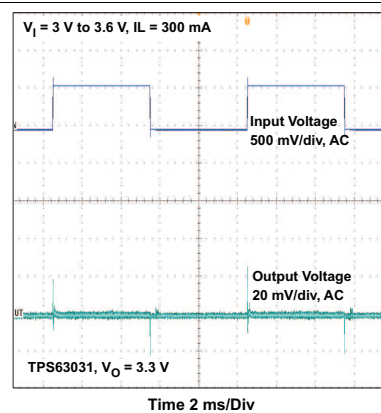


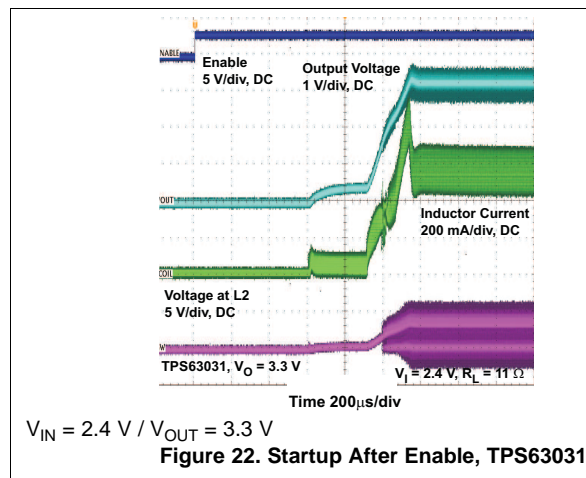
$V_{OUT} = 3.3\text{ V}$

**Figure 15. Efficiency vs Input Voltage, TPS63031, Power-Save Disabled**

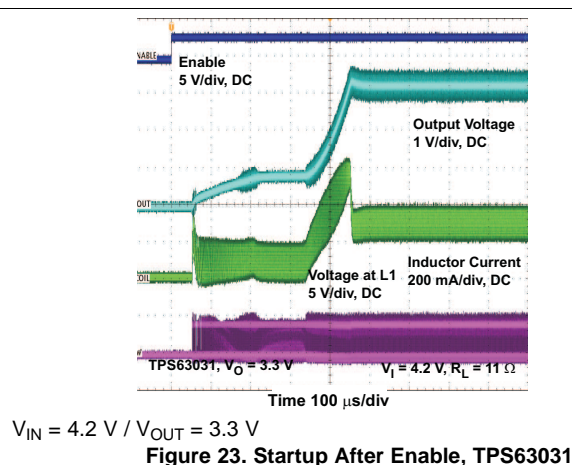
**TPS63030, TPS63031**

SLVS696C –OCTOBER 2008–REVISED OCTOBER 2015

[www.ti.com](http://www.ti.com)

 $V_{IN} = 3.6 \text{ V} / V_{OUT} = 2.5 \text{ V}$ 
**Figure 16. Output Voltage vs Output Current, TPS63031, Power-Save Disabled**

 $V_{IN} = 3.6 \text{ V} / V_{OUT} = 4.5 \text{ V}$ 
**Figure 17. Output Voltage vs Output Current, TPS63031, Power-Save Disabled**

 $V_{IN} = 3.6 \text{ V} / V_{OUT} = 3.3 \text{ V}$ 
**Figure 18. Output Voltage vs Output Current, TPS63031, Power-Save Disabled**

 $V_{IN} = 2.4 \text{ V} / V_{OUT} = 3.3 \text{ V}$ 
**Figure 19. Load Transient Response, TPS63031**

 $V_{IN} = 4.2 \text{ V} / V_{OUT} = 3.3 \text{ V}$ 
**Figure 20. Load Transient Response, TPS63031**

 $V_{IN} = 3.0 \text{ V} / V_{OUT} = 3.3 \text{ V}$ 
**Figure 21. Line Transient Response, TPS63031**



**Figure 22. Startup After Enable, TPS63031**



**Figure 23. Startup After Enable, TPS63031**

## 10 Power Supply Recommendations

The TPS6303x devices have no special requirements for its input power supply. The output current of the input power supply needs to be rated according to the supply voltage, output voltage and output current of the TPS6303x.

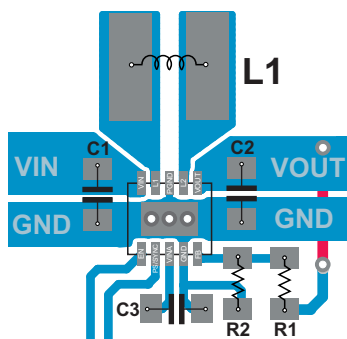
## 11 Layout

### 11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, TI recommends to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

### 11.2 Layout Example



**Figure 24. Layout Recommendation**

### 11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the exposed thermal pad
- Introducing airflow in the system

For more details on how to use the thermal parameters in the dissipation ratings table please check the *Thermal Characteristics Application Note* ([SZZA017](#)) and the *Semiconductor and IC Package Thermal Metrics Application Note* ([SPRA953](#)).



## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Third-Party Products Disclaimer

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### 12.2 Documentation Support

#### 12.2.1 Related Documentation

For related documentation see the following:

*Thermal Characteristics Application Note* ([SZZA017](#))

### 12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 3. Related Links**

| PARTS    | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| TPS63030 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TPS63031 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.5 Trademarks

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All other trademarks are the property of their respective owners.

### 12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS63030DSKR     | ACTIVE        | SON          | DSK                | 10   | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CEE                     | <a href="#">Samples</a> |
| TPS63030DSKRG4   | ACTIVE        | SON          | DSK                | 10   | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CEE                     | <a href="#">Samples</a> |
| TPS63030DSKT     | ACTIVE        | SON          | DSK                | 10   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CEE                     | <a href="#">Samples</a> |
| TPS63030DSKTG4   | ACTIVE        | SON          | DSK                | 10   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CEE                     | <a href="#">Samples</a> |
| TPS63031DSKR     | ACTIVE        | SON          | DSK                | 10   | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CEF                     | <a href="#">Samples</a> |
| TPS63031DSKT     | ACTIVE        | SON          | DSK                | 10   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CEF                     | <a href="#">Samples</a> |
| TPS63031DSKTG4   | ACTIVE        | SON          | DSK                | 10   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CEF                     | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

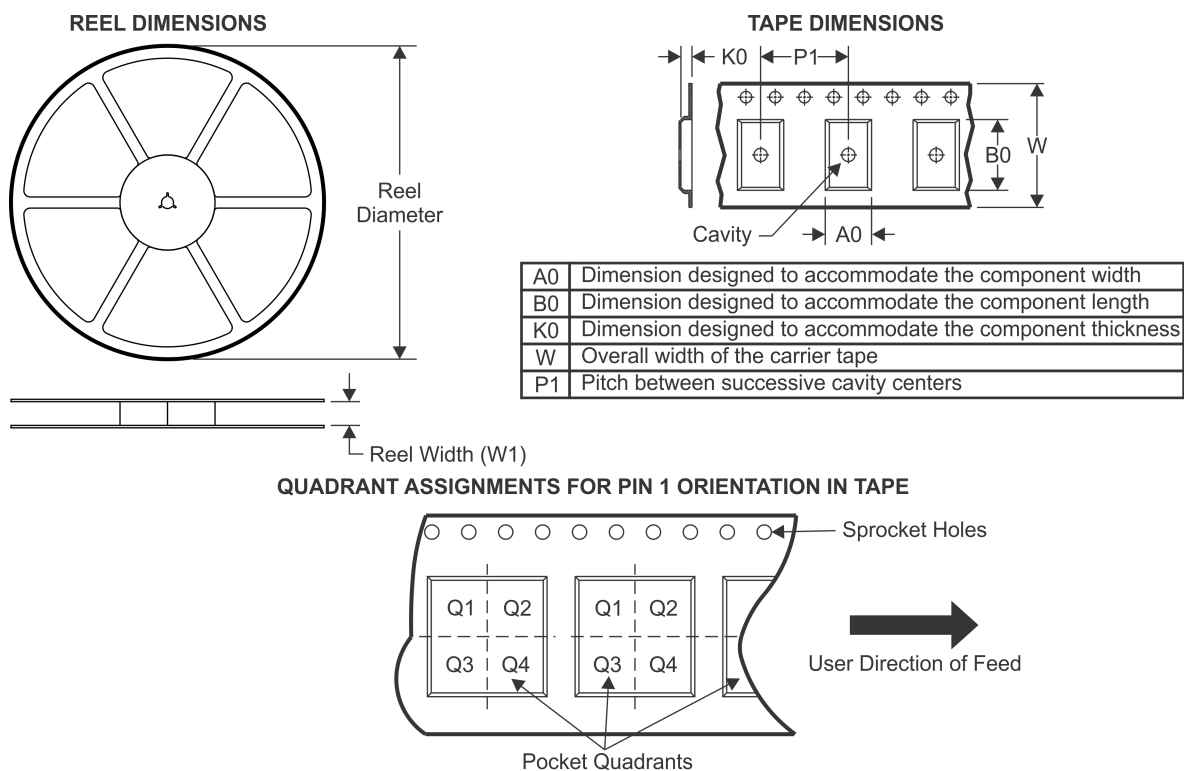
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS63030DSKR | SON          | DSK             | 10   | 3000 | 180.0              | 8.4                | 2.8     | 2.8     | 1.0     | 4.0     | 8.0    | Q2            |
| TPS63030DSKR | SON          | DSK             | 10   | 3000 | 178.0              | 8.4                | 2.75    | 2.75    | 0.95    | 4.0     | 8.0    | Q2            |
| TPS63030DSKT | SON          | DSK             | 10   | 250  | 178.0              | 8.4                | 2.75    | 2.75    | 0.95    | 4.0     | 8.0    | Q2            |
| TPS63030DSKT | SON          | DSK             | 10   | 250  | 180.0              | 8.4                | 2.8     | 2.8     | 1.0     | 4.0     | 8.0    | Q2            |
| TPS63031DSKR | SON          | DSK             | 10   | 3000 | 178.0              | 8.4                | 2.75    | 2.75    | 0.95    | 4.0     | 8.0    | Q2            |
| TPS63031DSKR | SON          | DSK             | 10   | 3000 | 180.0              | 8.4                | 2.8     | 2.8     | 1.0     | 4.0     | 8.0    | Q2            |
| TPS63031DSKT | SON          | DSK             | 10   | 250  | 180.0              | 8.4                | 2.8     | 2.8     | 1.0     | 4.0     | 8.0    | Q2            |
| TPS63031DSKT | SON          | DSK             | 10   | 250  | 178.0              | 8.4                | 2.75    | 2.75    | 0.95    | 4.0     | 8.0    | Q2            |

## TAPE AND REEL BOX DIMENSIONS

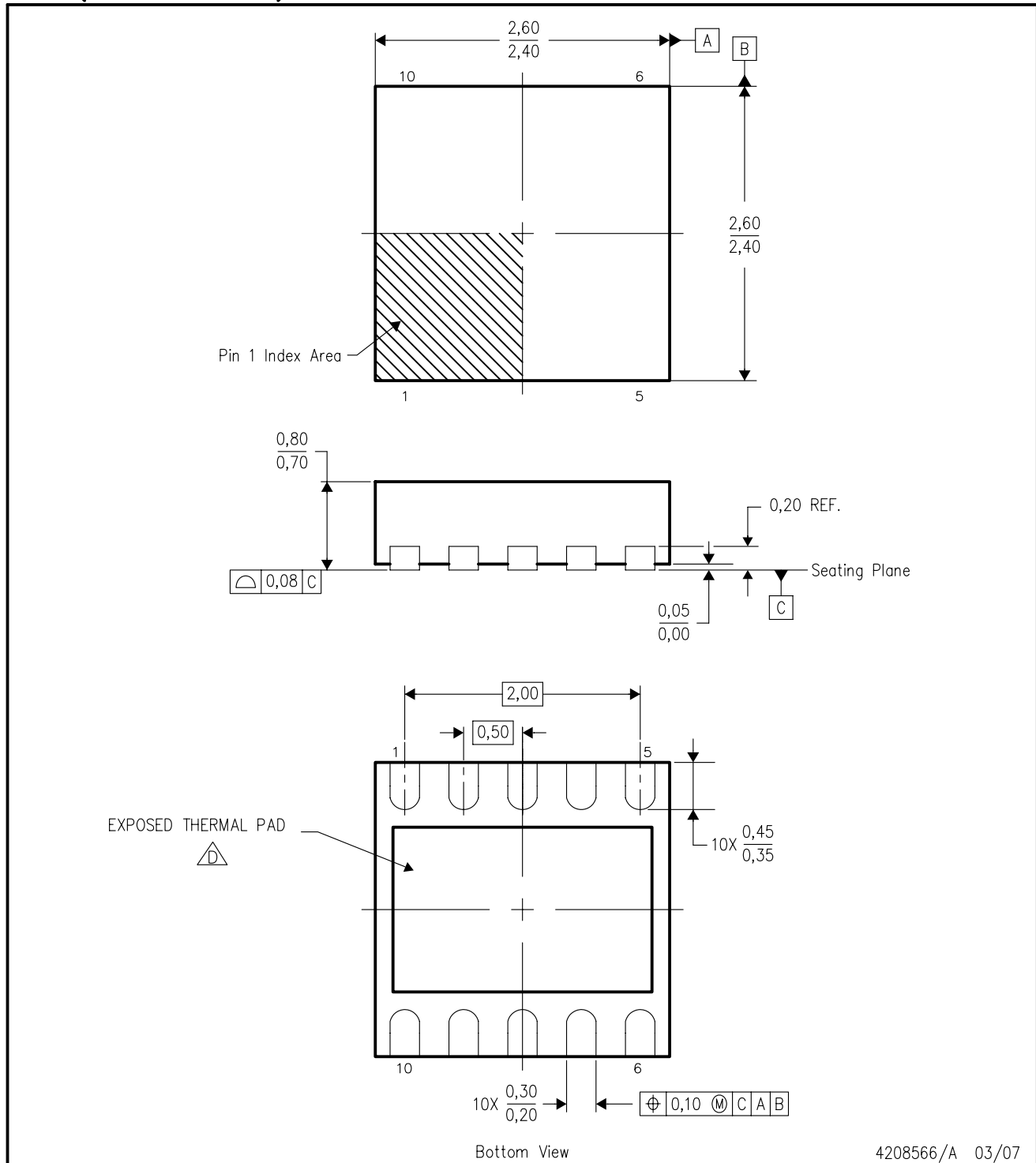


\*All dimensions are nominal


| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS63030DSKR | SON          | DSK             | 10   | 3000 | 210.0       | 185.0      | 35.0        |
| TPS63030DSKR | SON          | DSK             | 10   | 3000 | 205.0       | 200.0      | 33.0        |
| TPS63030DSKT | SON          | DSK             | 10   | 250  | 205.0       | 200.0      | 33.0        |
| TPS63030DSKT | SON          | DSK             | 10   | 250  | 210.0       | 185.0      | 35.0        |
| TPS63031DSKR | SON          | DSK             | 10   | 3000 | 205.0       | 200.0      | 33.0        |
| TPS63031DSKR | SON          | DSK             | 10   | 3000 | 210.0       | 185.0      | 35.0        |
| TPS63031DSKT | SON          | DSK             | 10   | 250  | 210.0       | 185.0      | 35.0        |
| TPS63031DSKT | SON          | DSK             | 10   | 250  | 205.0       | 200.0      | 33.0        |

DSK (S-PDSO-N10)

PLASTIC QUAD FLATPACK



4208566/A 03/07

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Small Outline No-Lead (SON) package configuration.
  -  D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

## THERMAL PAD MECHANICAL DATA

DSK (R-PWSON-N10)

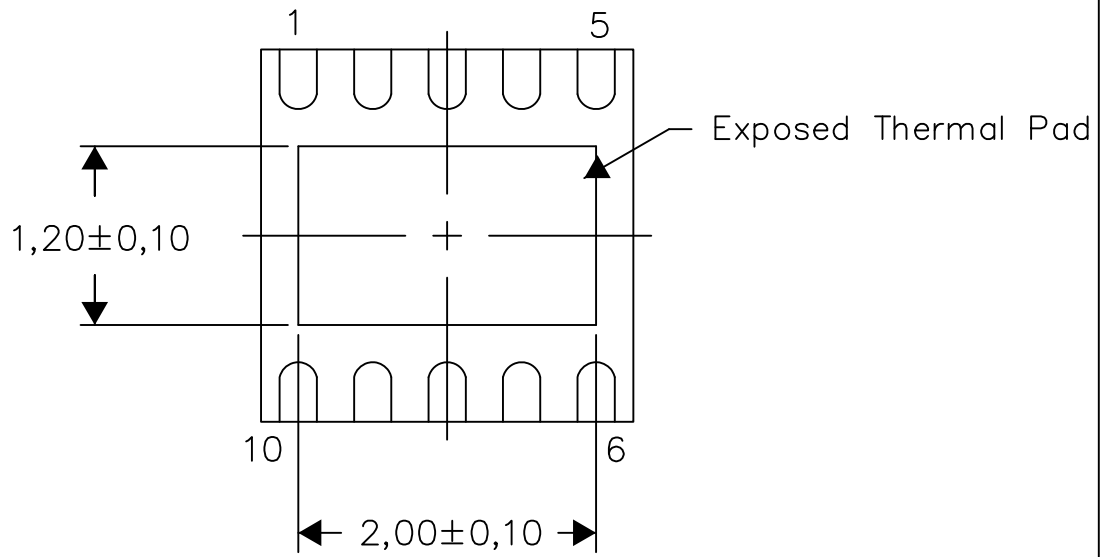
PLASTIC SMALL OUTLINE NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

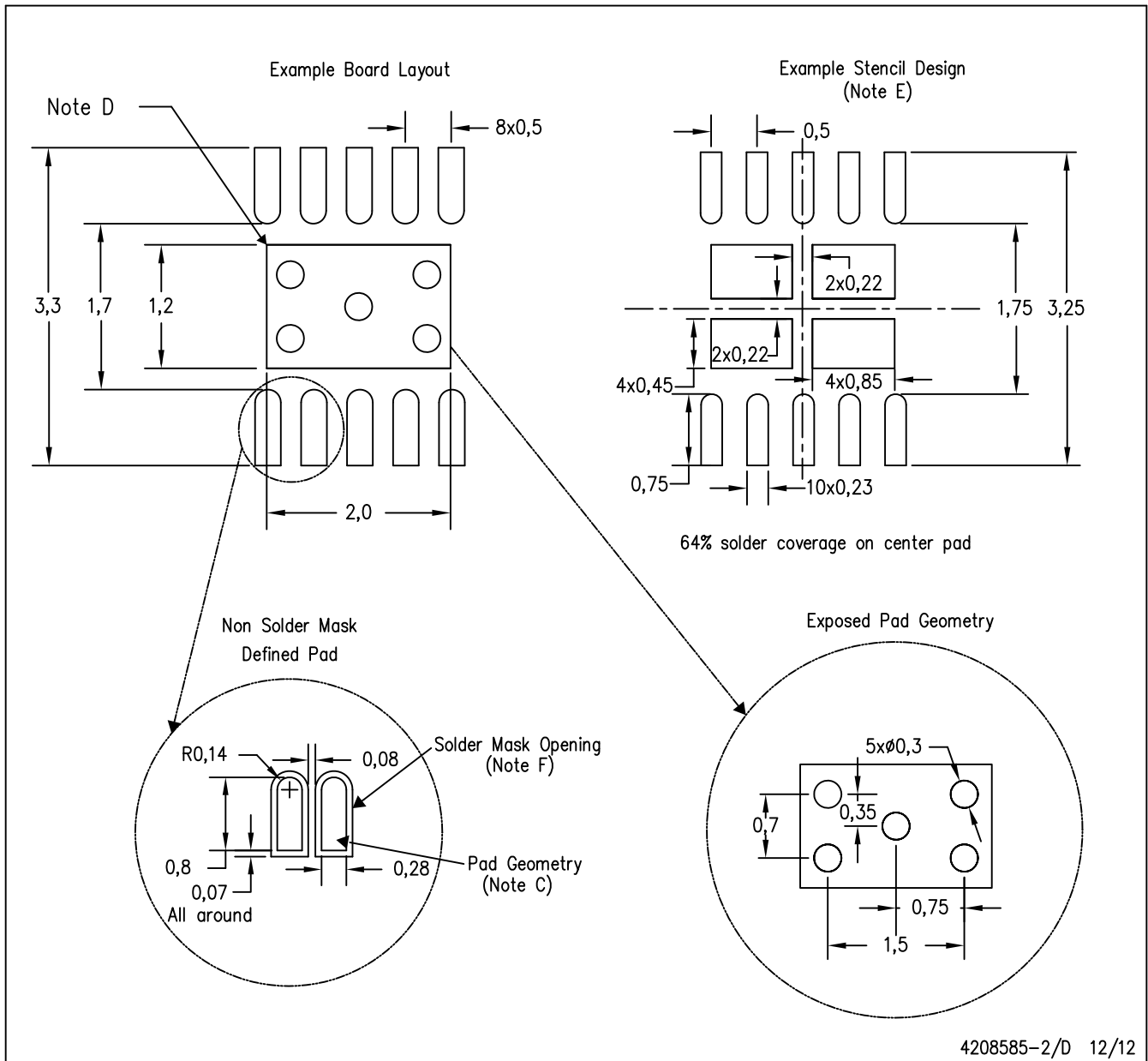
4208579-2/E 12/12

NOTE: All linear dimensions are in millimeters



DSK (R-PWSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-SM-782 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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