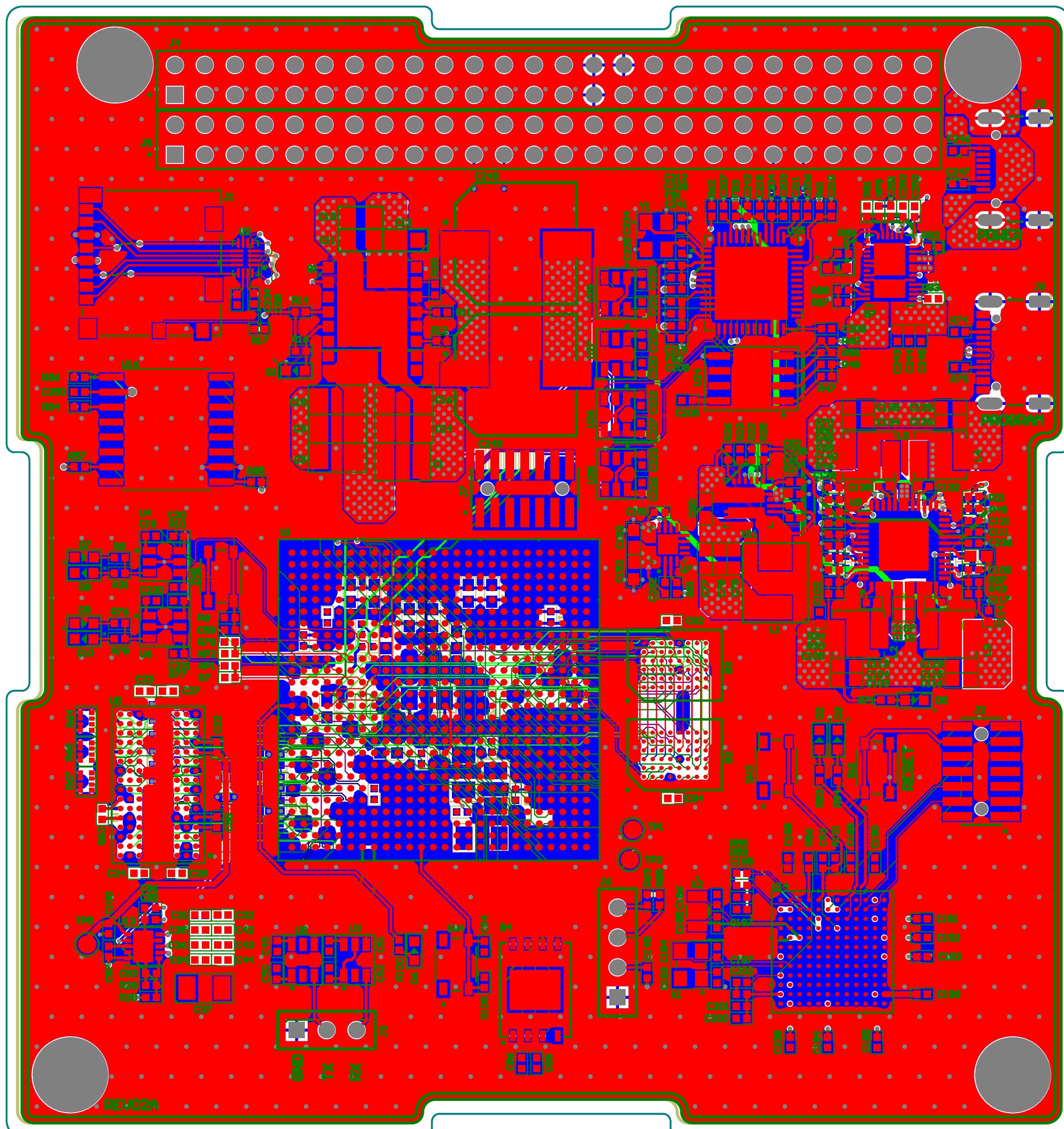
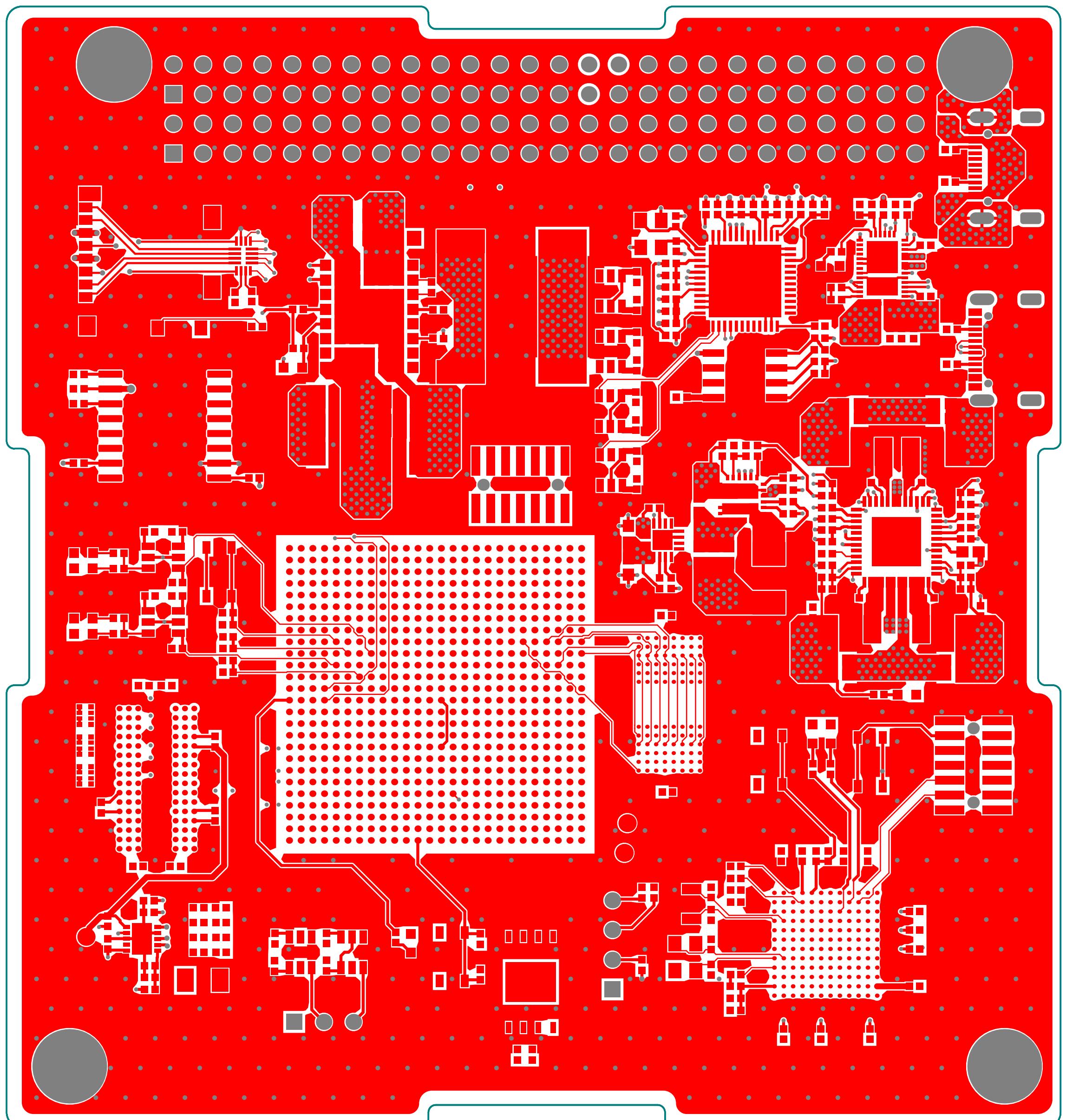


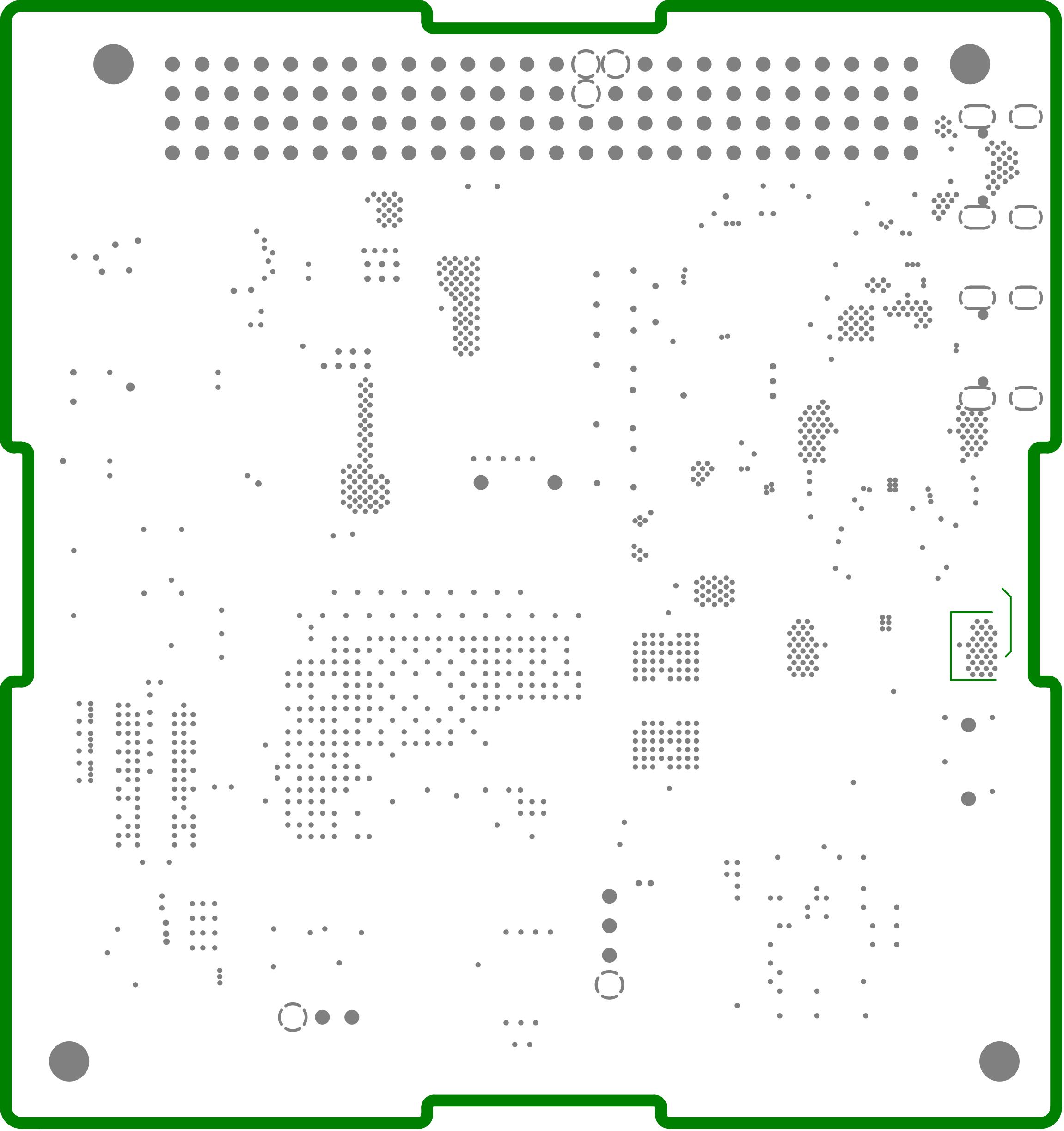


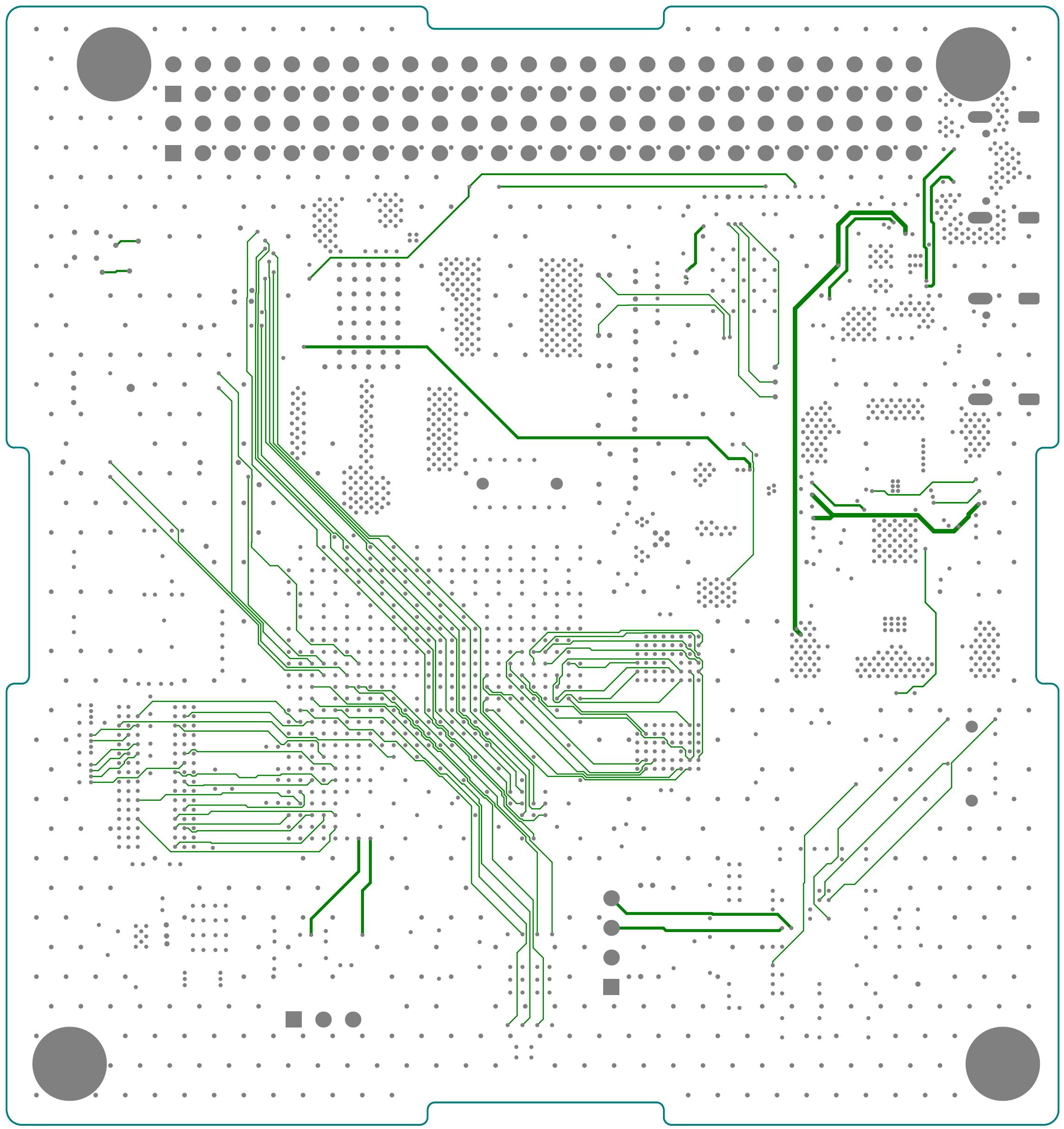
## Projeto FPGAgeing

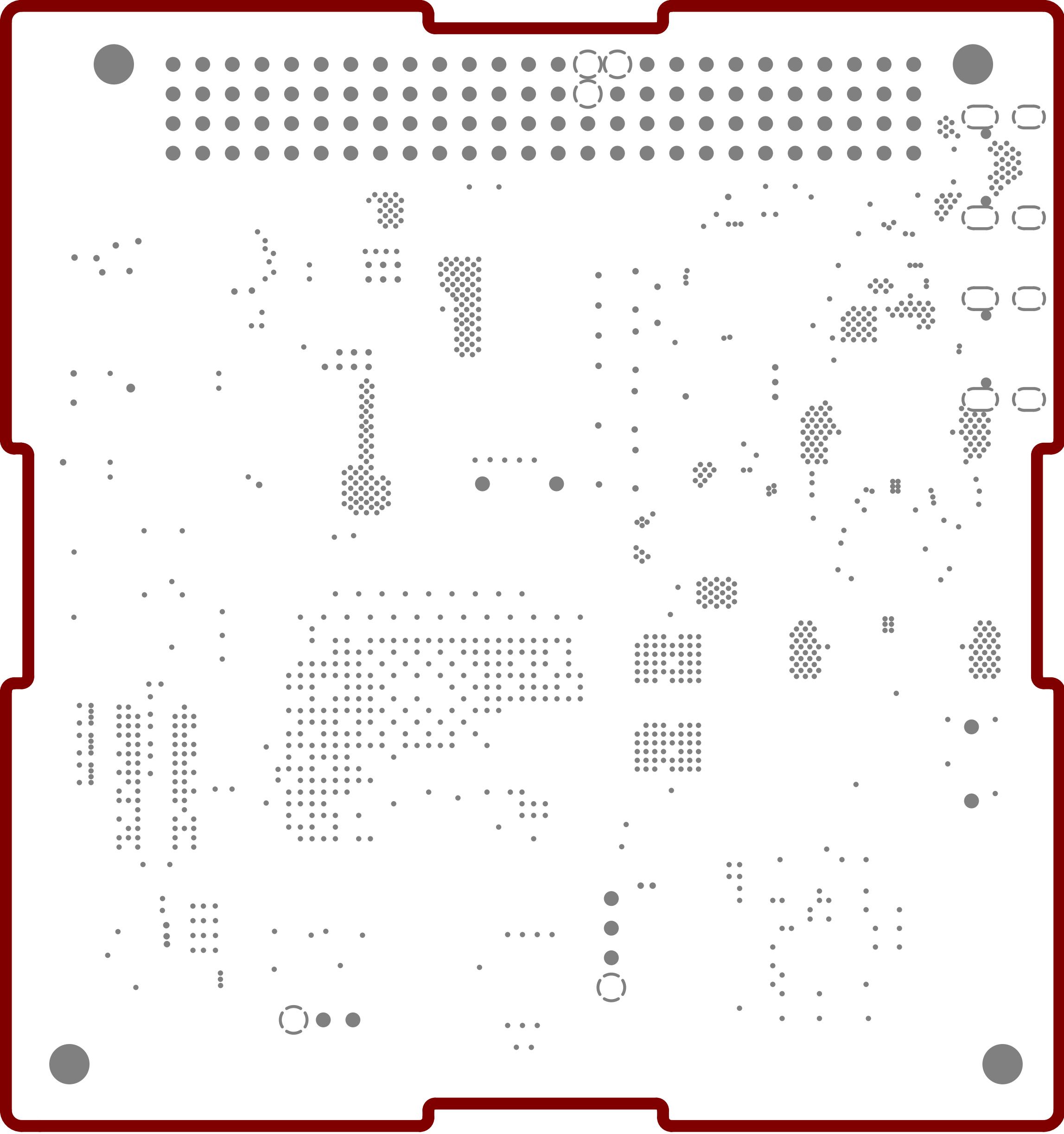
Autor: Julio Vitorino  
Orientação: Jarbas Silveira

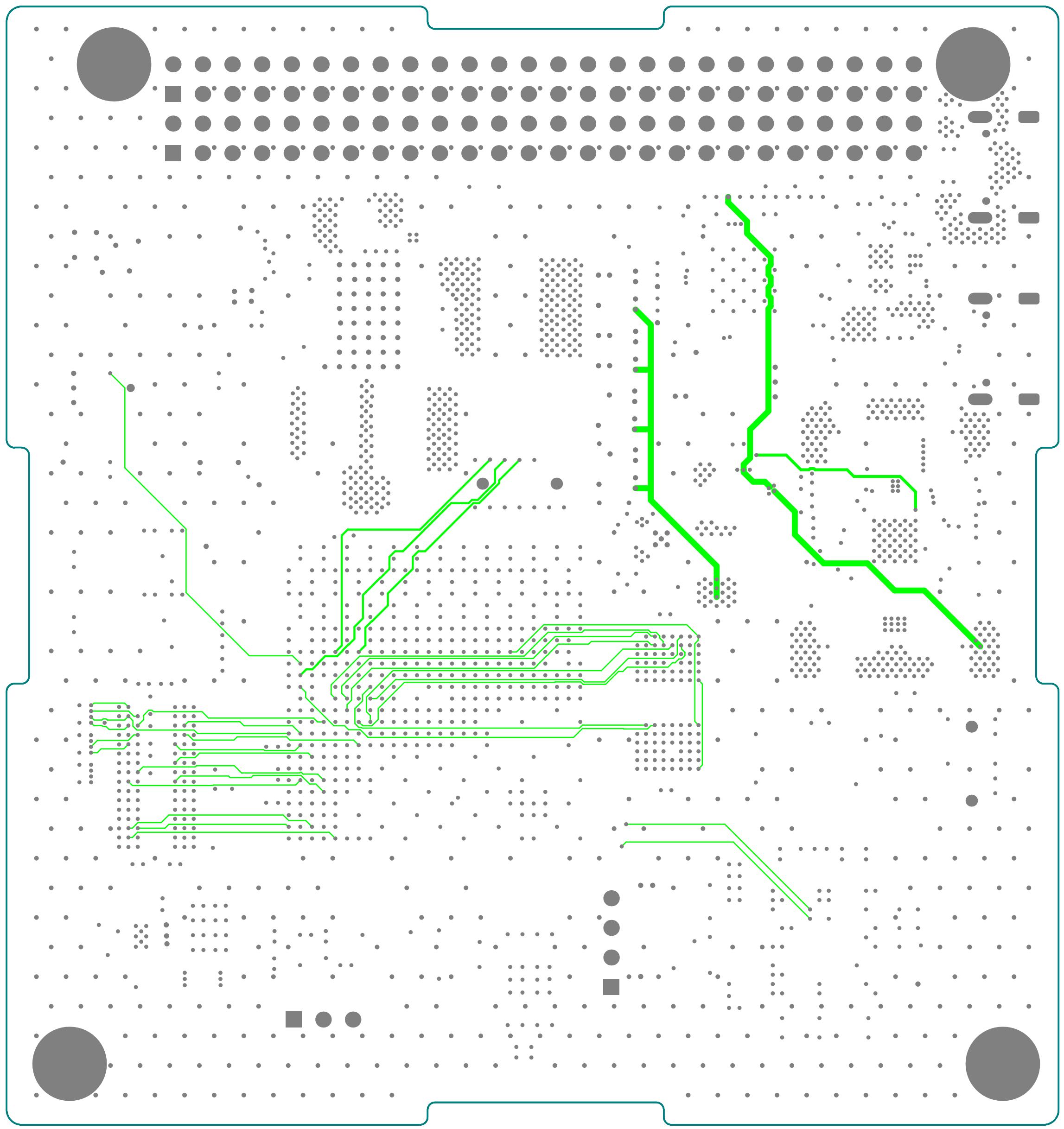


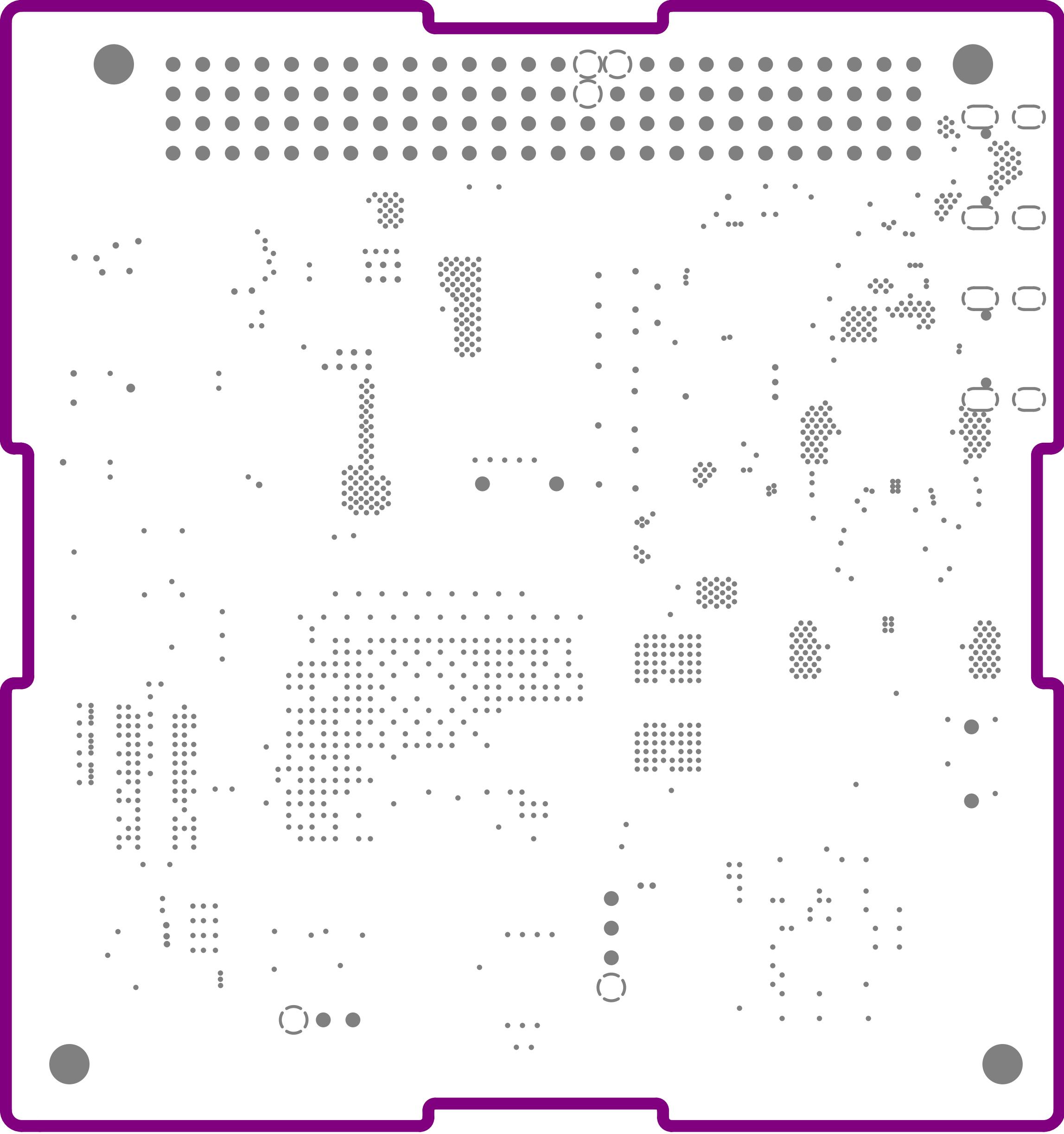


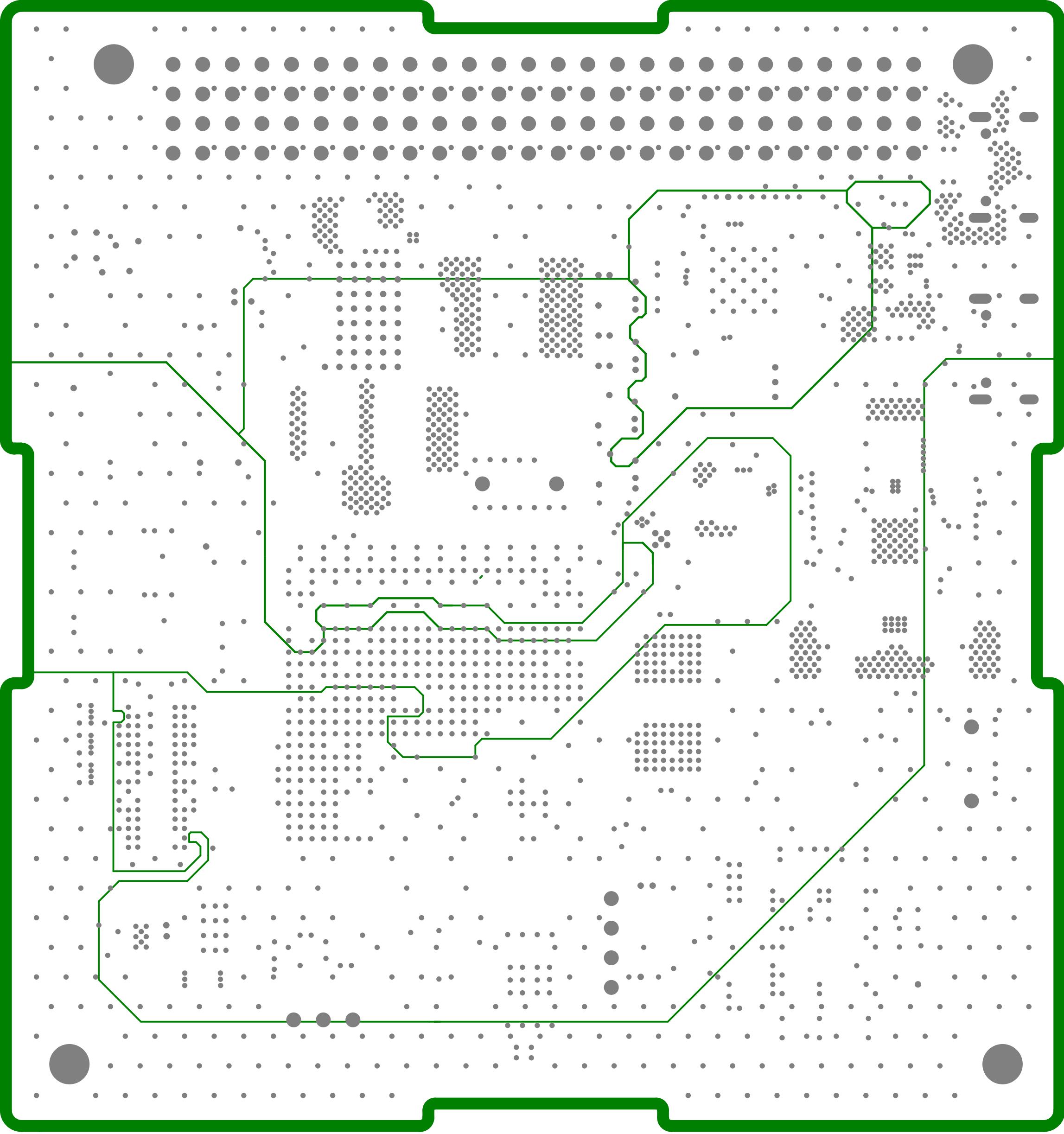


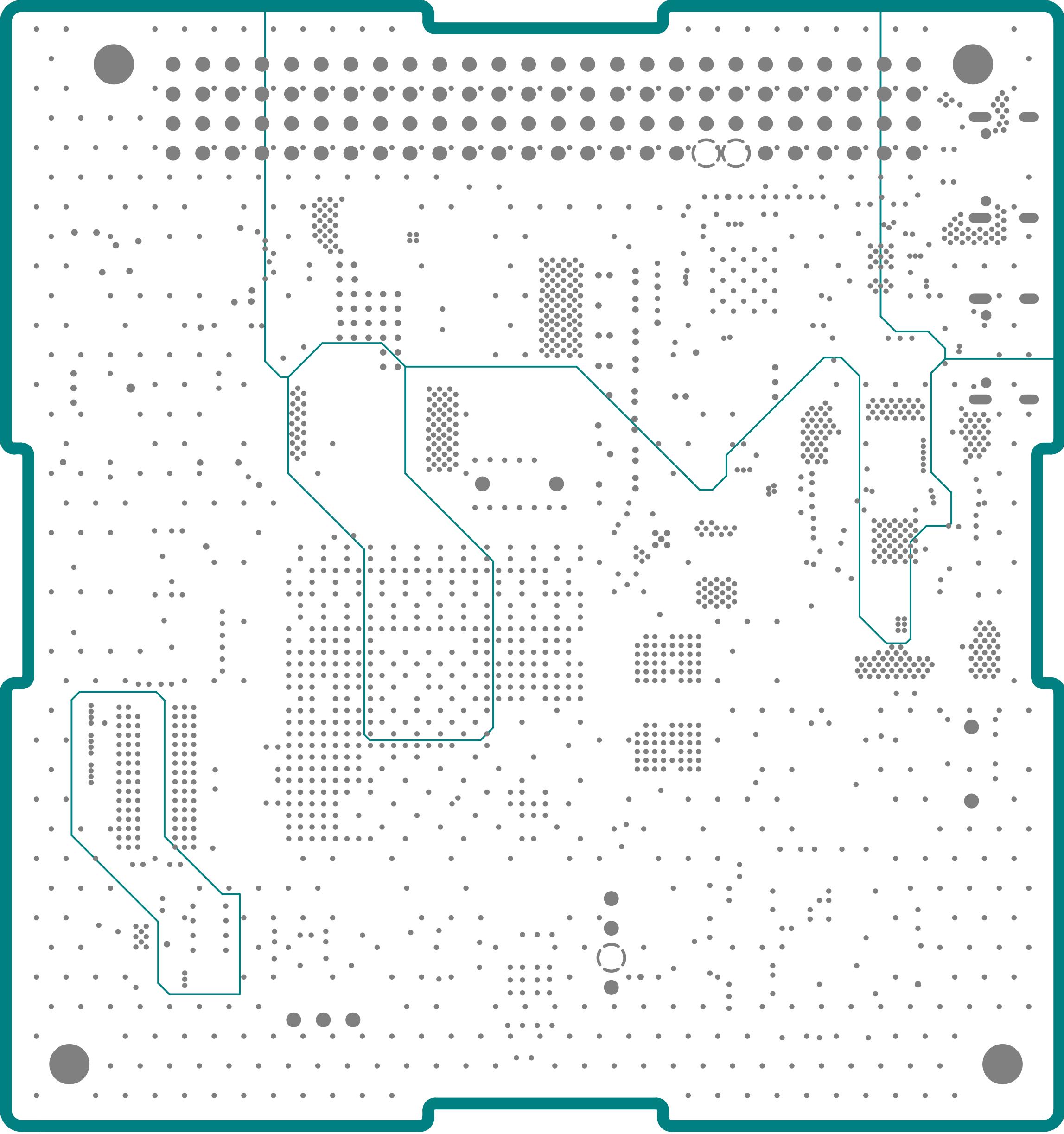


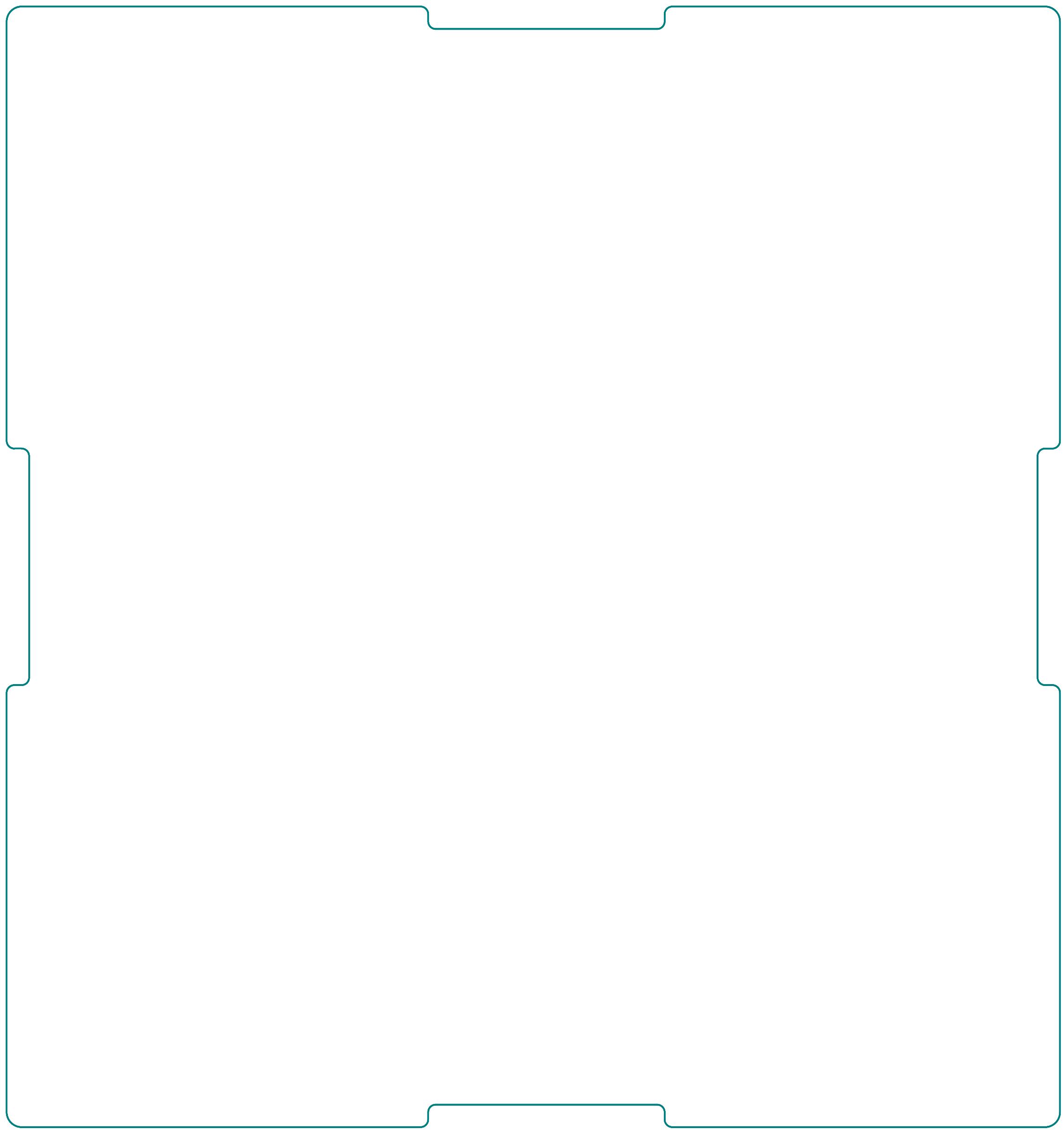


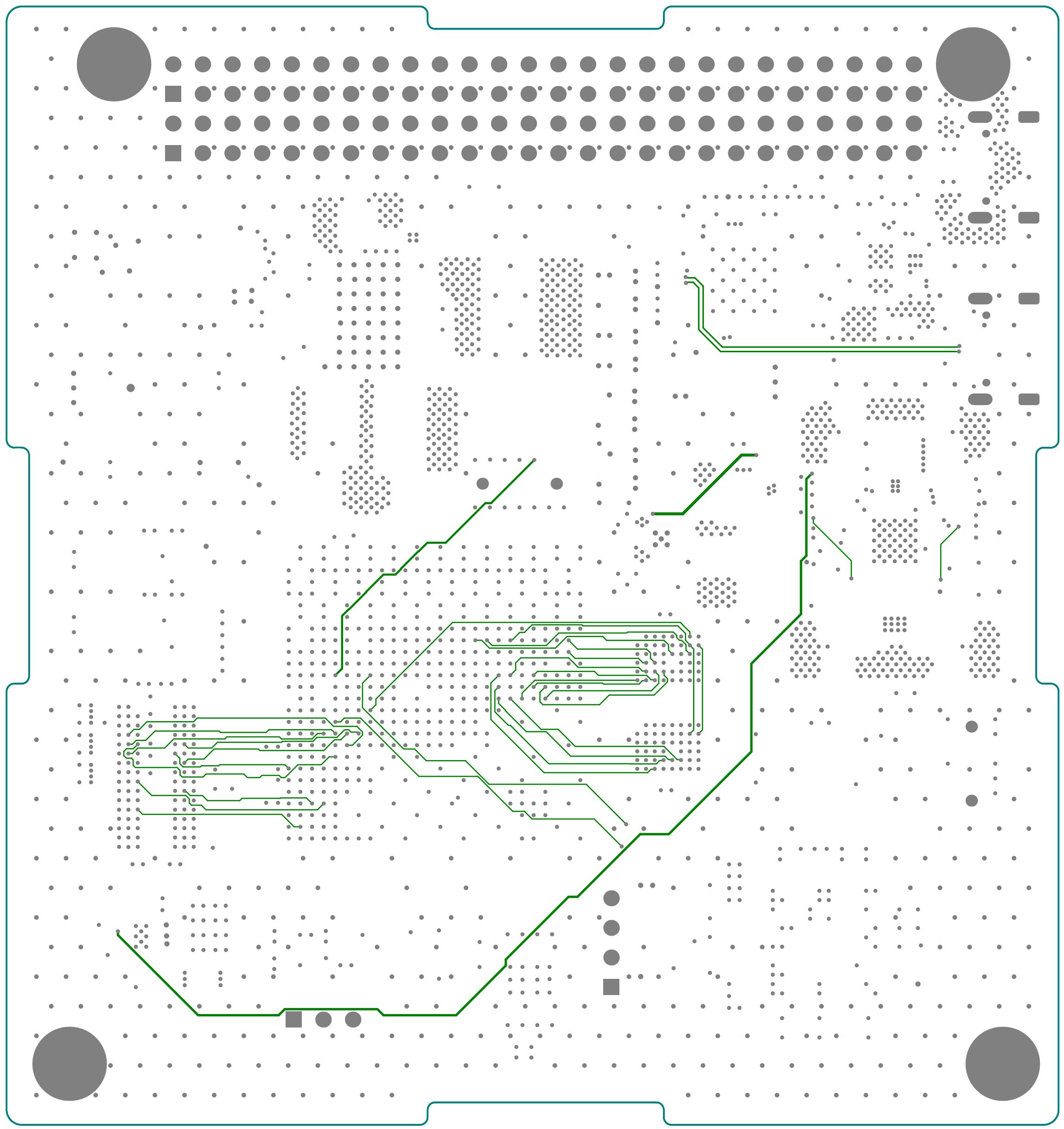


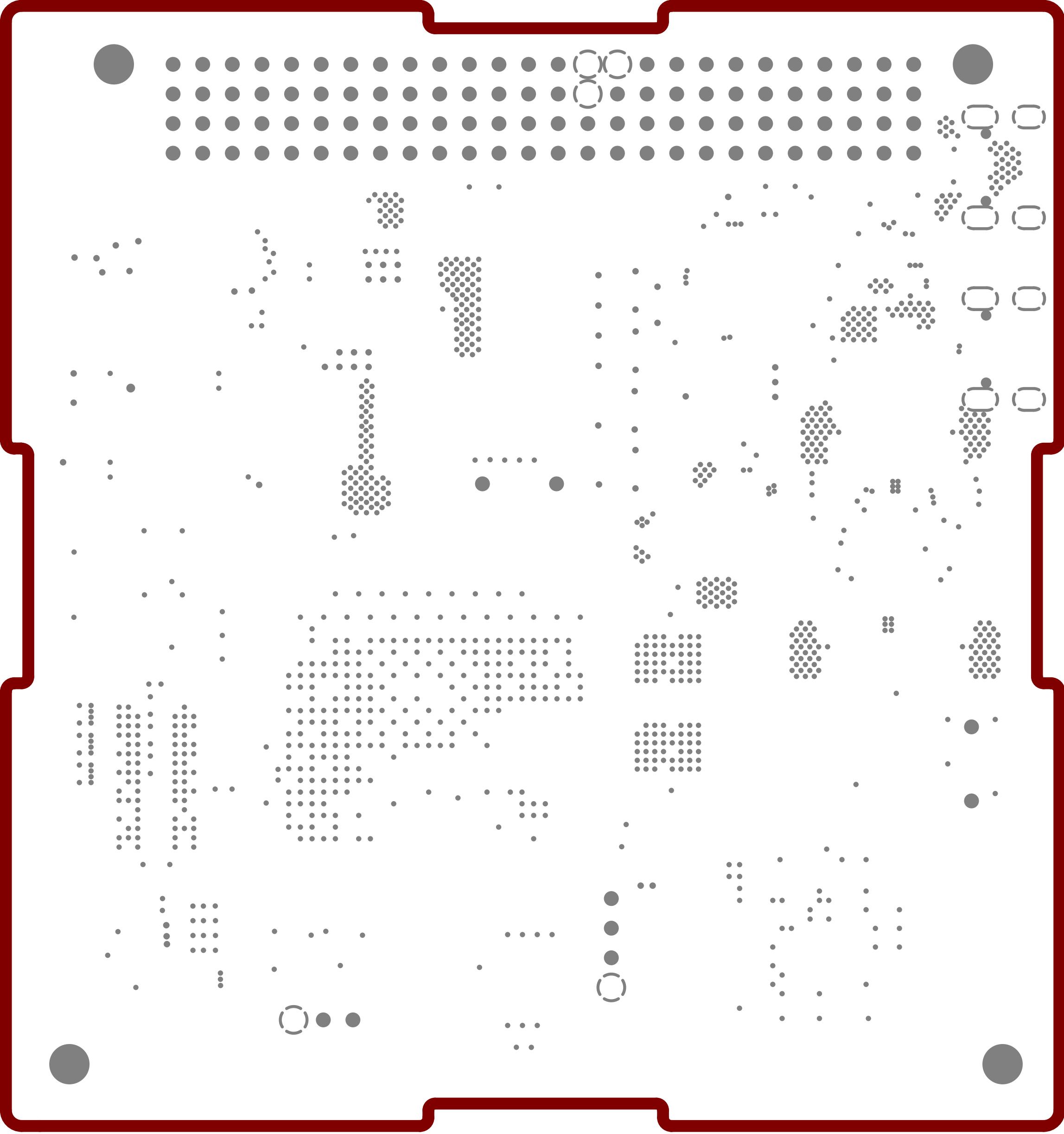


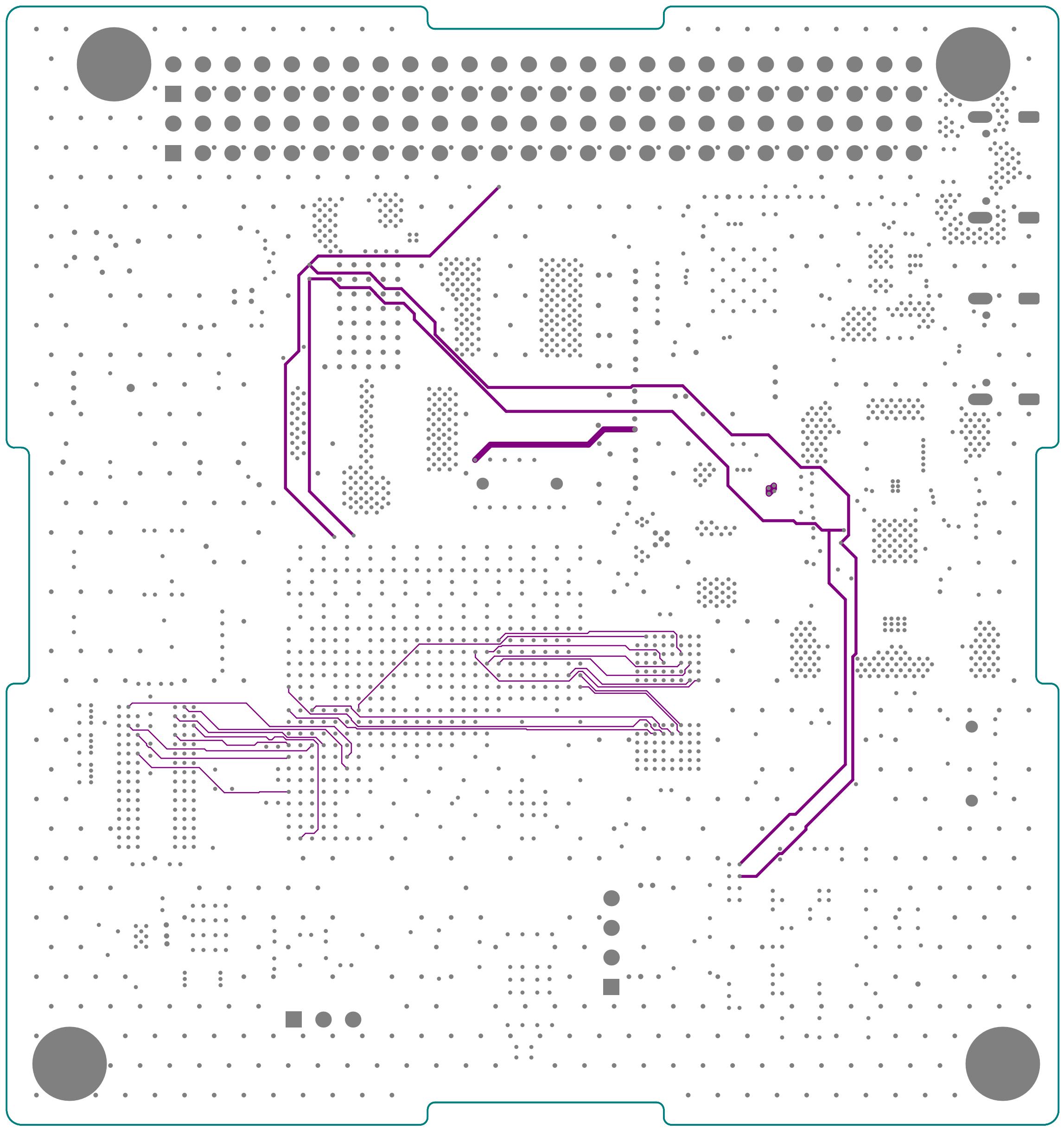


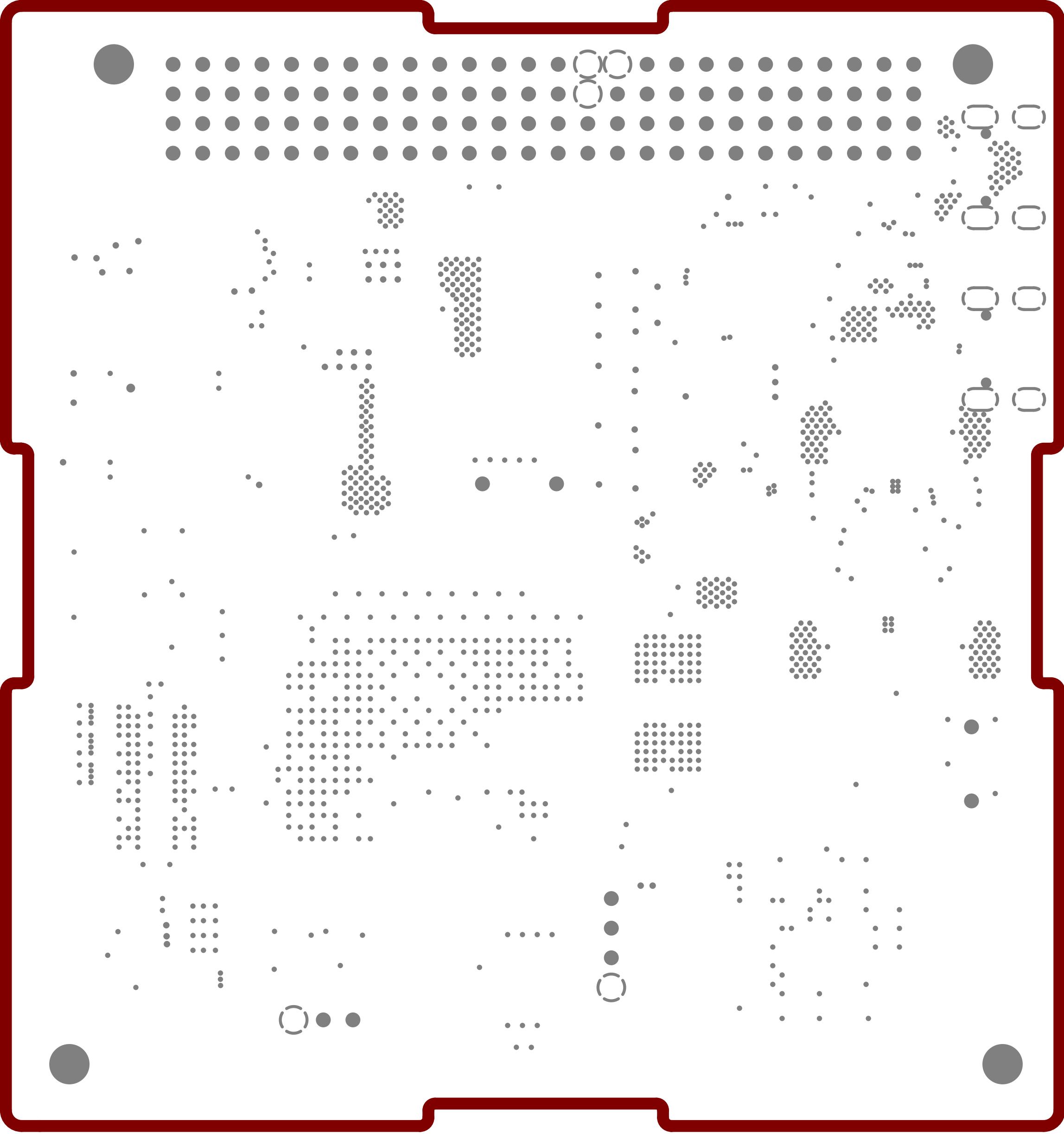


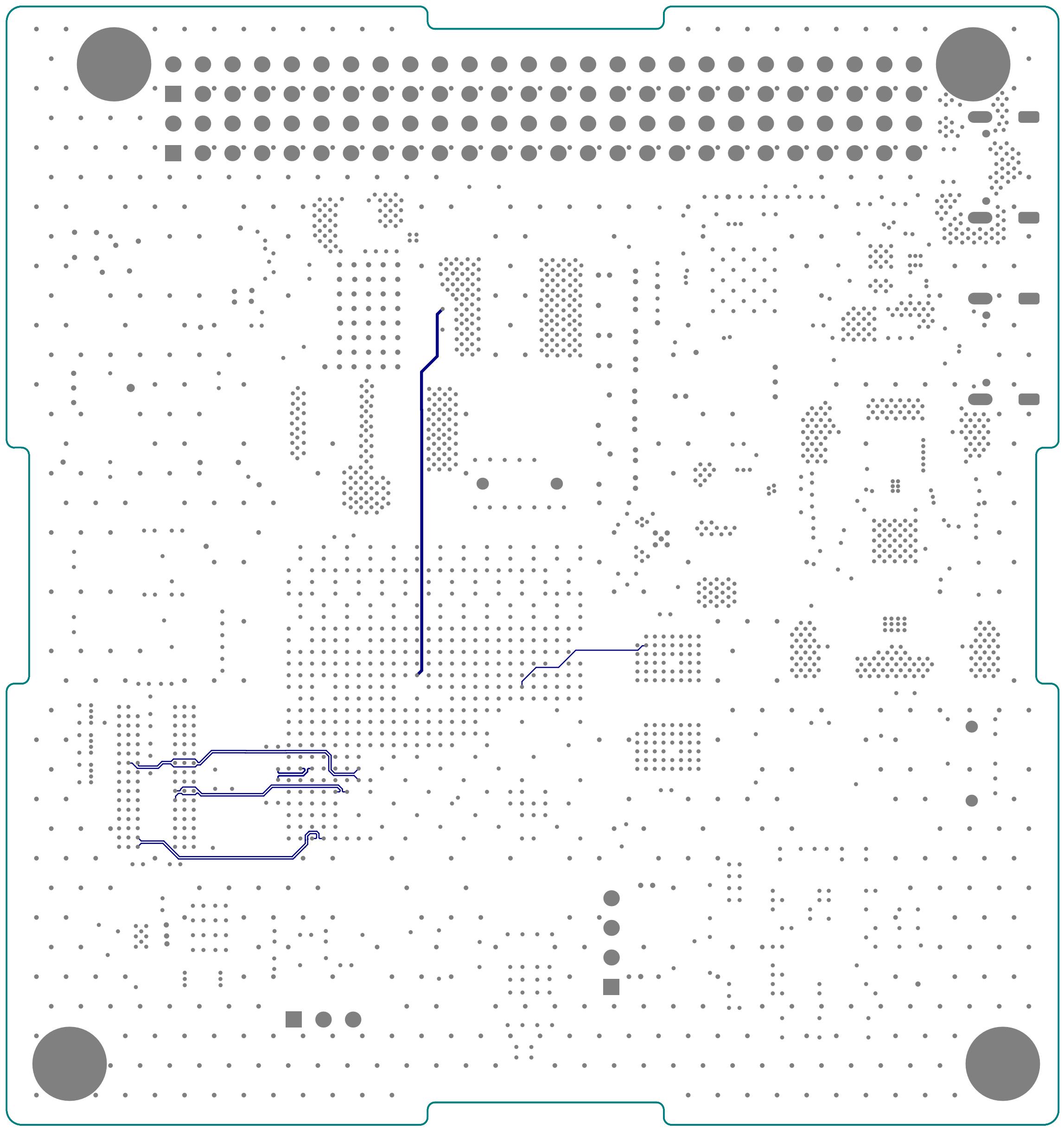


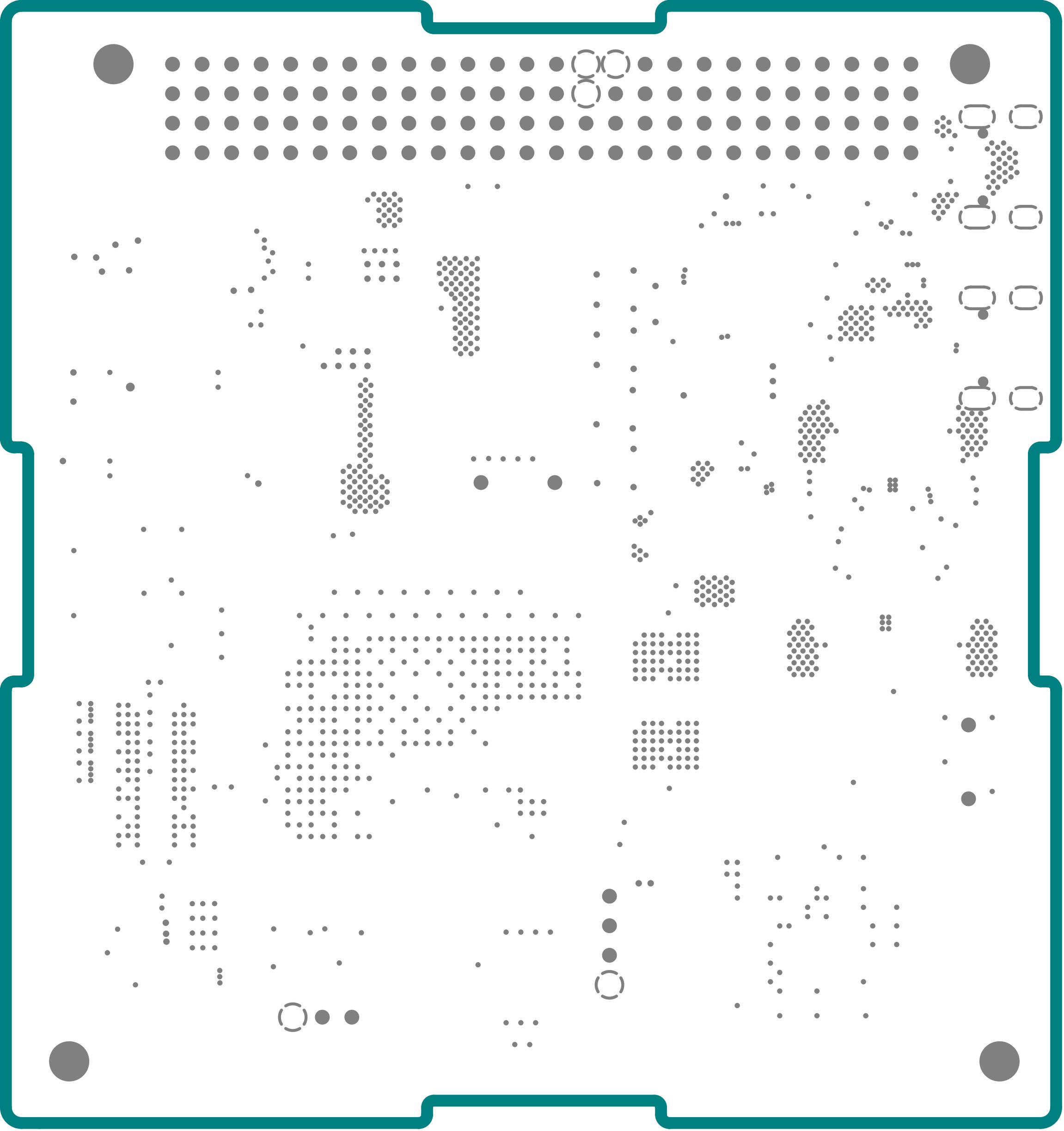


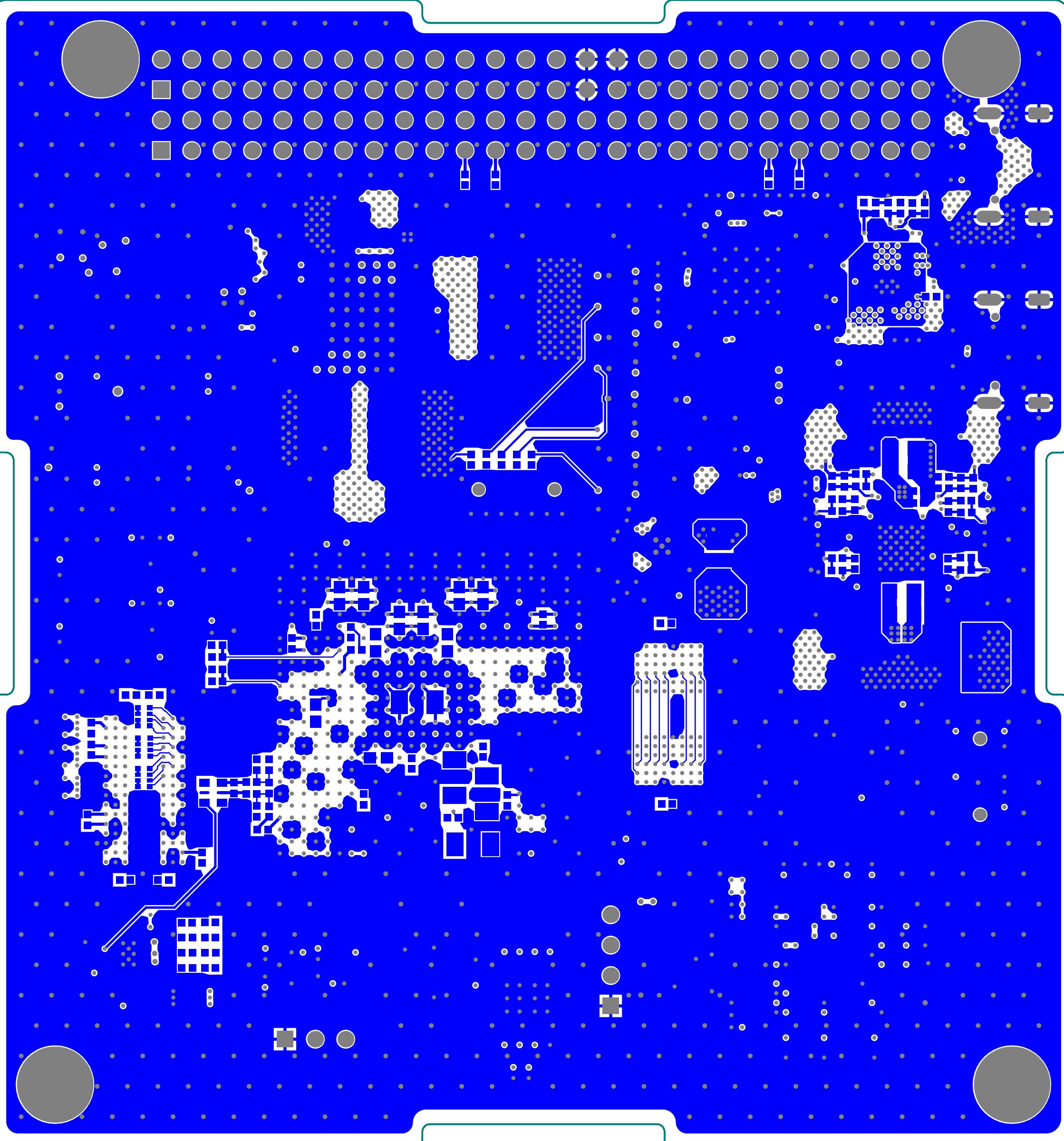












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Nome da Sheet: "

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Campus do Pici - Bloco 723, S/N - Pici, Fortaleza - CE, 60455-970

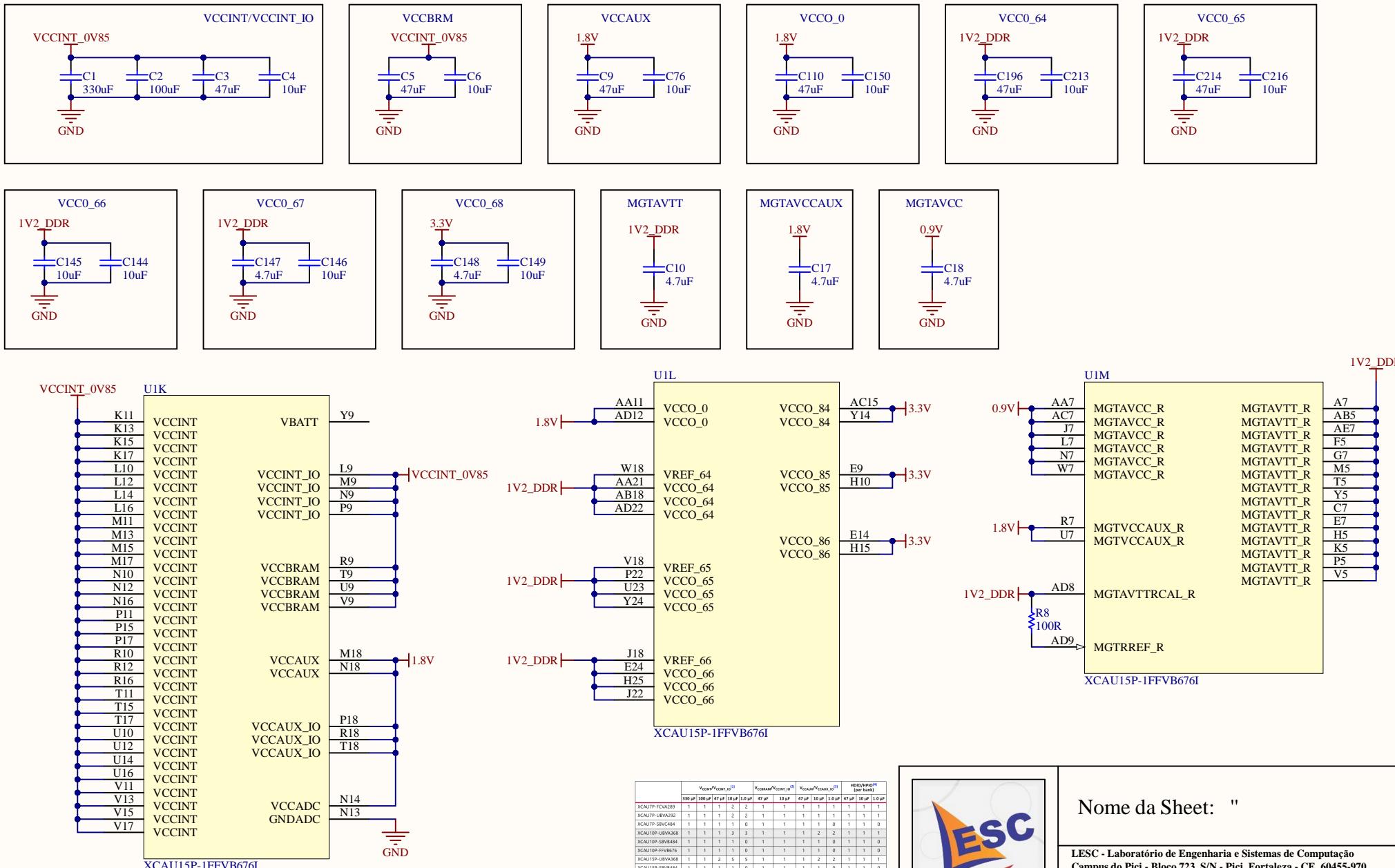
Data:

Projetista: Julio Vitorino

PCB Design: Julio Vitorino

Revision:

Size:



Nome da Sheet: "

	$\text{Y}_{\text{CMB}}$	$\text{Y}_{\text{CMB}} \cdot \text{Y}_{\text{CMB}}$ <sup>(II)</sup>	$\text{Y}_{\text{CMB}} \text{Y}_{\text{CMB}}$	$\text{Y}_{\text{CMB}} \text{Y}_{\text{CMB}}$ <sup>(II)</sup>	$\text{HDO}/\text{HDHO}$
	10 <sup>-10</sup> $\mu\text{Jy}$	10 <sup>-10</sup> $\mu\text{Jy}$	10 <sup>-10</sup> $\mu\text{Jy}$	10 <sup>-10</sup> $\mu\text{Jy}$	10 <sup>-10</sup> $\mu\text{Jy}$
CAU117-FCV4A29	1	1	1	1	1
CAU117-LBV4A29	1	1	2	2	1
CAU117-SPV4A6	1	1	1	0	1
CAU119-UVA368	1	1	3	3	1
CAU119-UVA484	1	1	1	0	1
CAU119-FVB76	1	1	1	0	1
CAU119-UVA368	1	2	5	5	1
CAU119-UVA484	1	1	1	0	1
CAU120-FVB76	1	1	0	1	1
CAU120-FVB784	1	2	4	0	1
CAU120-FVB786	1	1	1	2	0
CAU120-UVA484	1	1	2	0	1

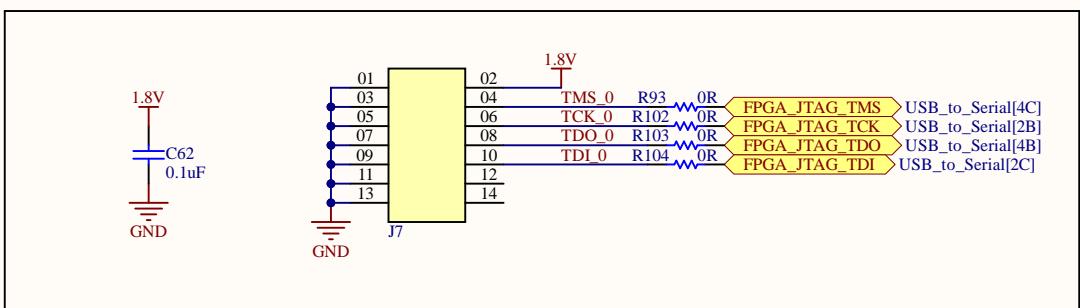
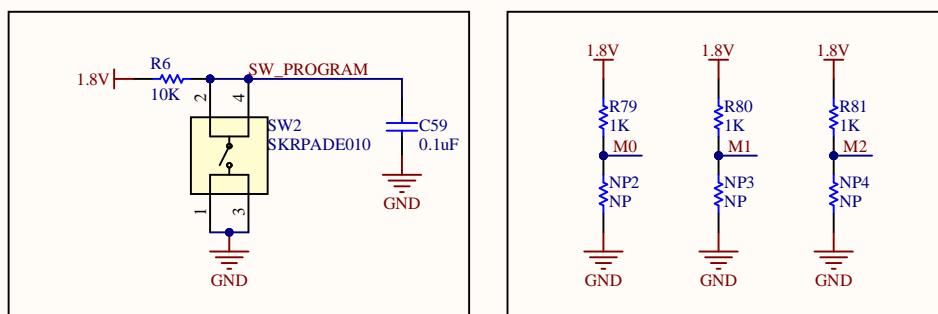
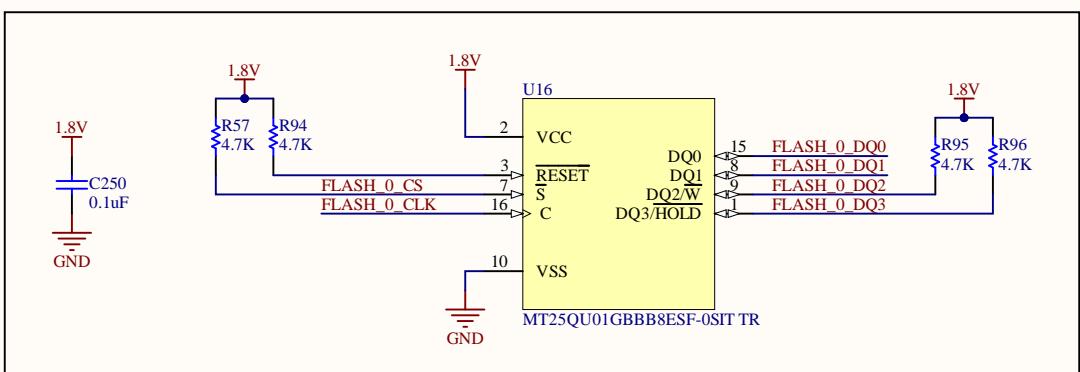
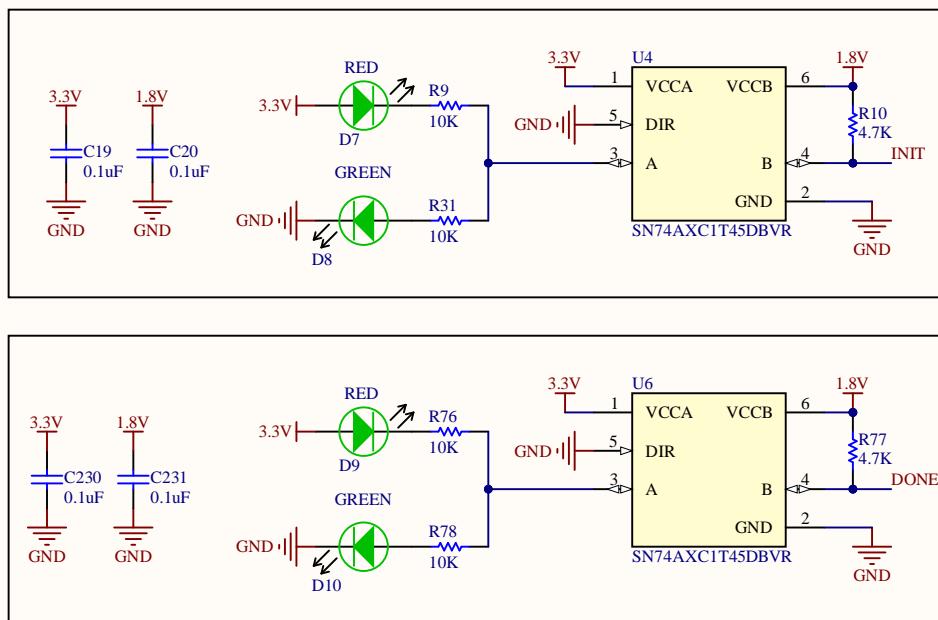
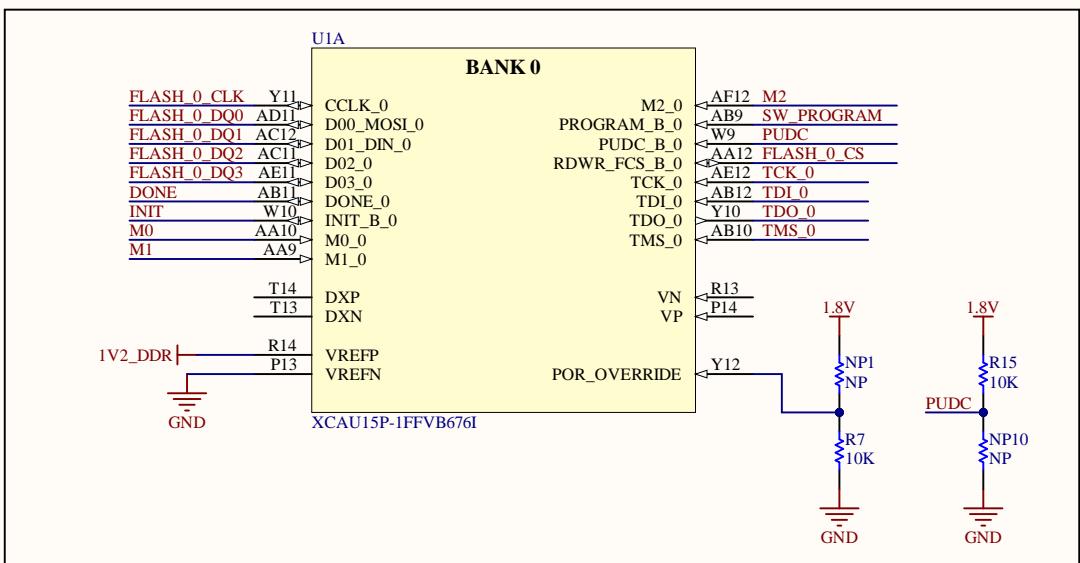
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Data:

Projeto de Julio Vitorino

Position

Revision:  
Size: A4



Nome da Sheet: "

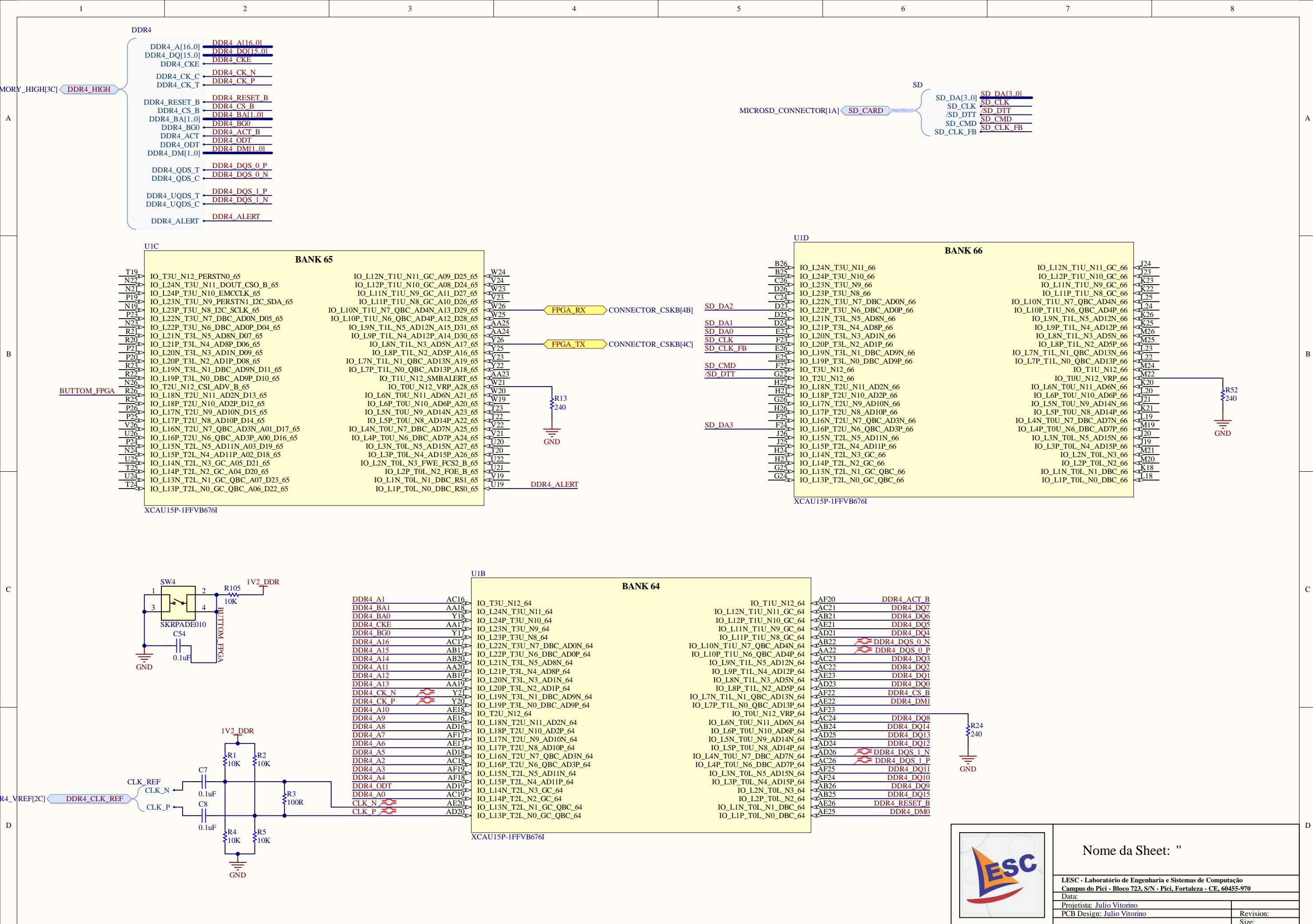
LESC - Laboratório de Engenharia e Sistemas de Computação  
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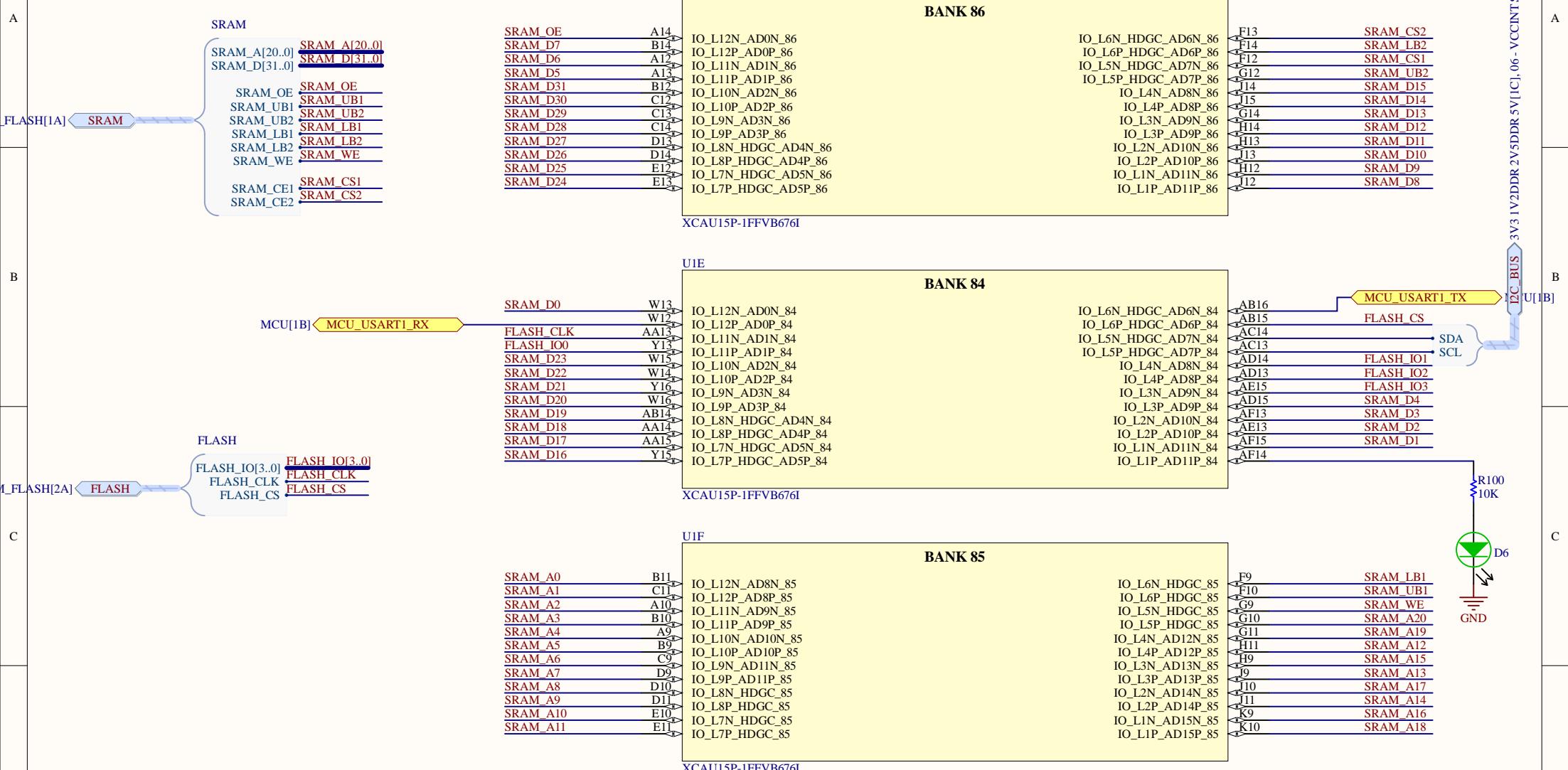
Data:

Projetista: Julio Vitorino

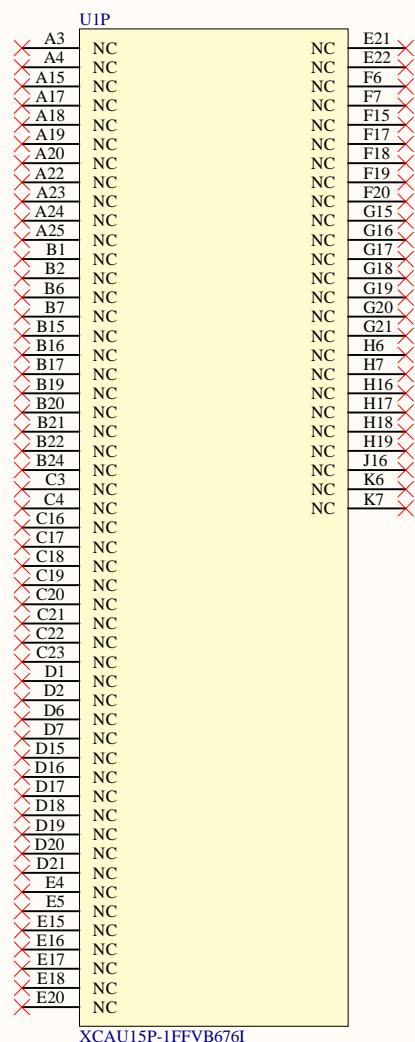
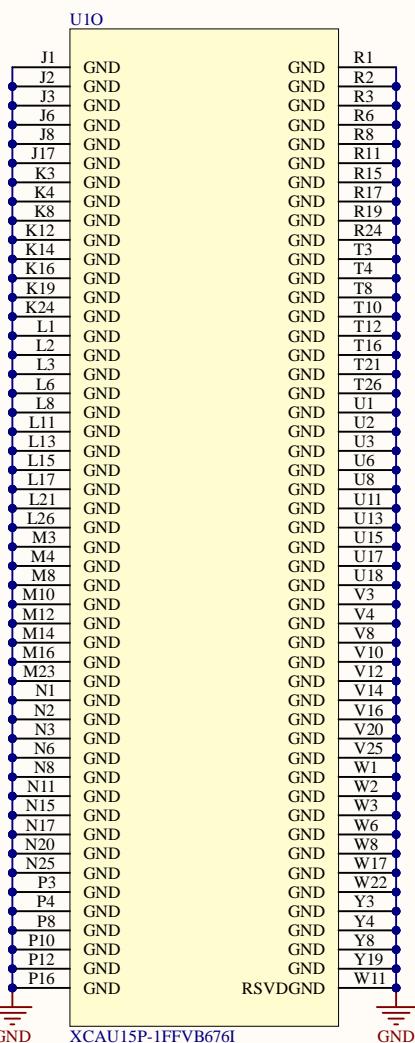
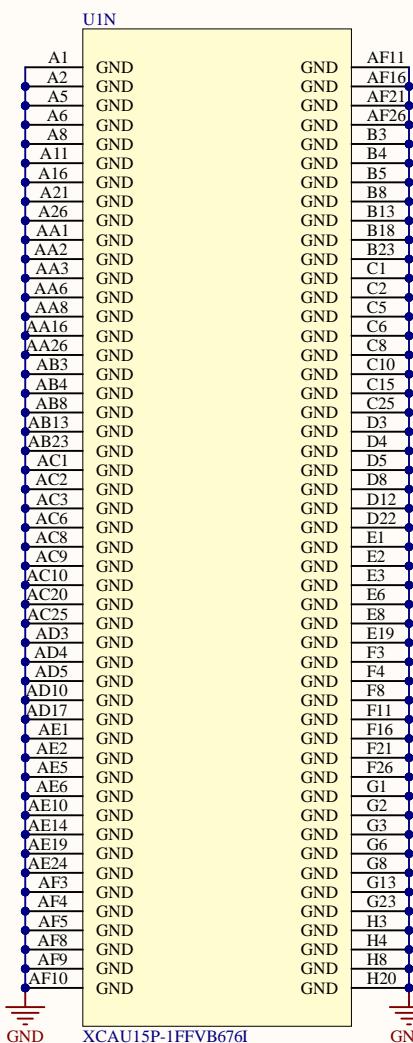
PCB Design: Julio Vitorino

Revision:  
Size: A4

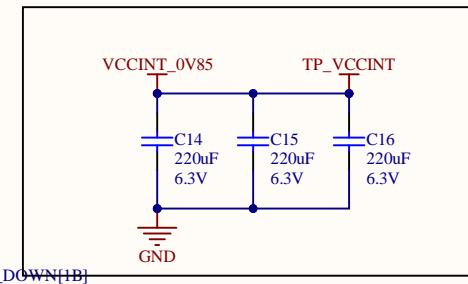
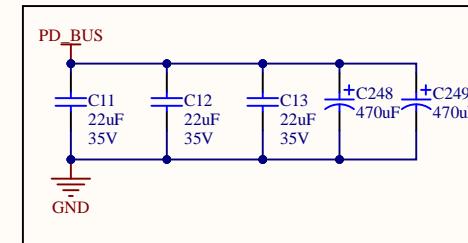
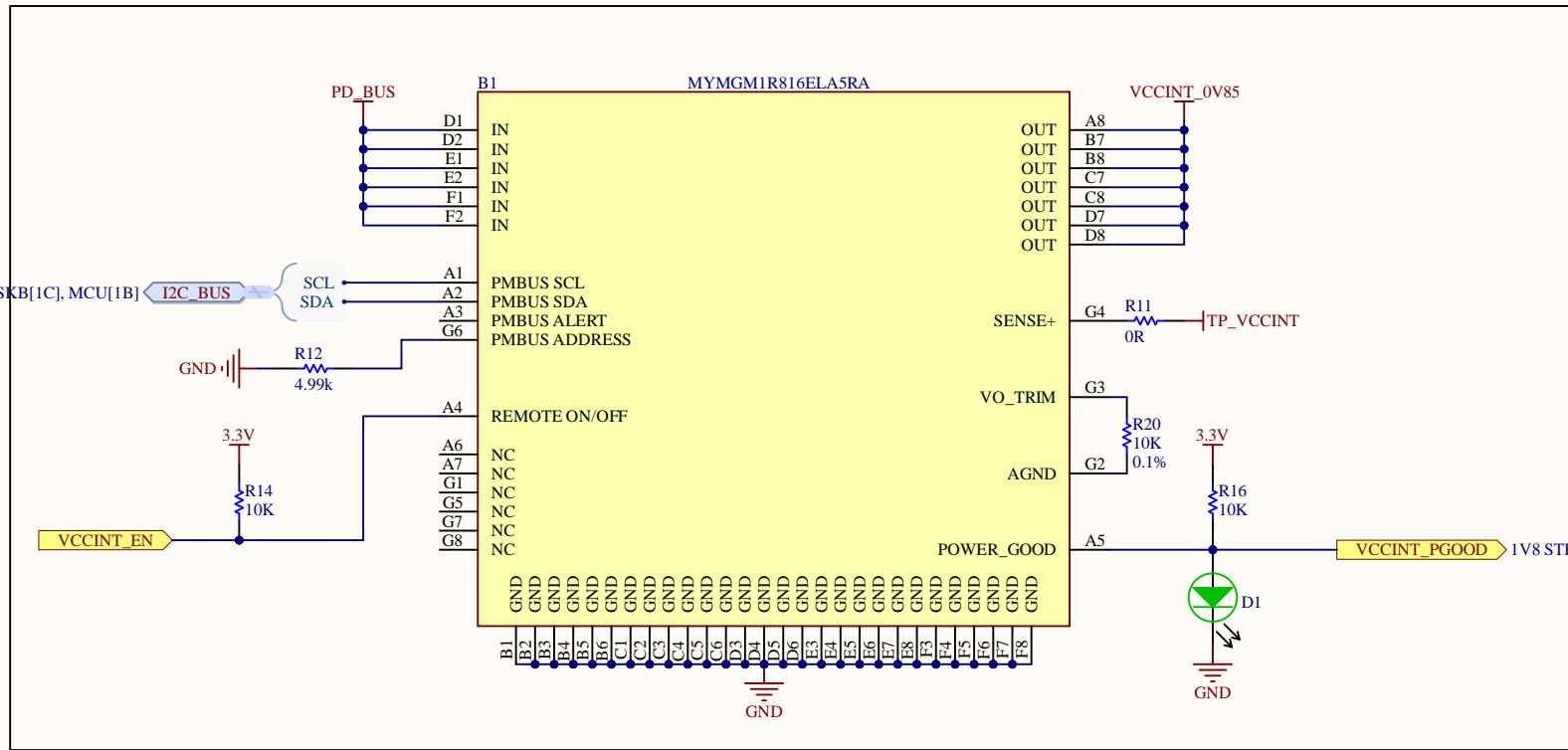




A



Title		
Size	Number	Revision
A4		
Date:	11/17/2025	Sheet of
File:	C:\Users\...\06 - FPGA_GND.SchDoc	Drawn By:



Nome da Sheet: "

LESC - Laboratório de Engenharia e Sistemas de Computação  
Campus do Pici - Bloco 723, S/N - Pici, Fortaleza - CE, 60455-970

Data:

Projetista: Julio Vitorino

PCB Design: Julio Vitorino

Revision:

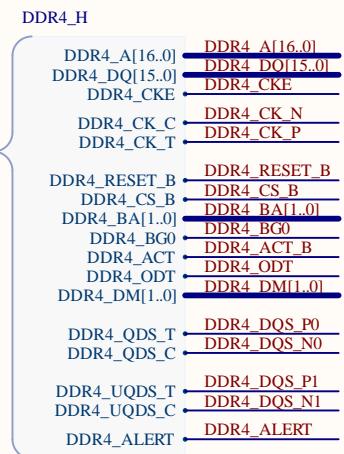
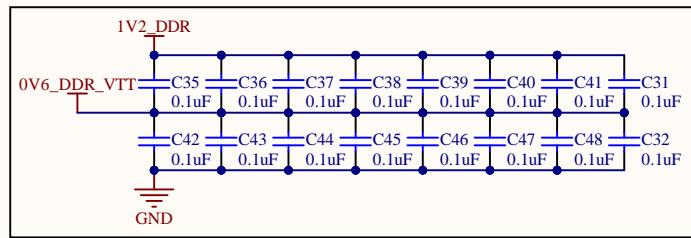
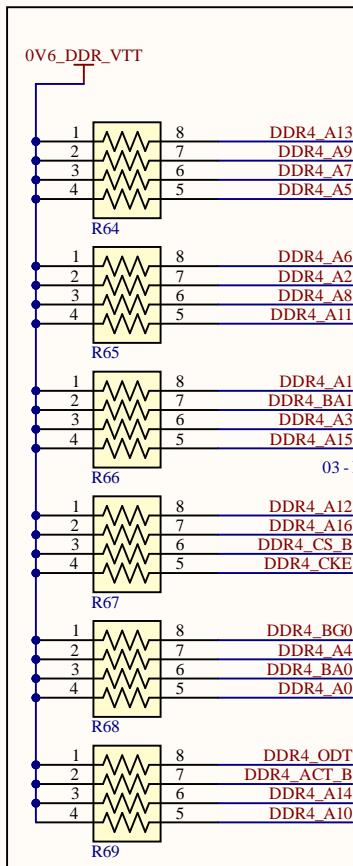
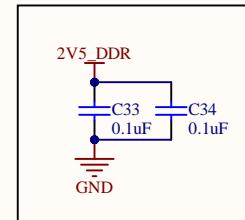
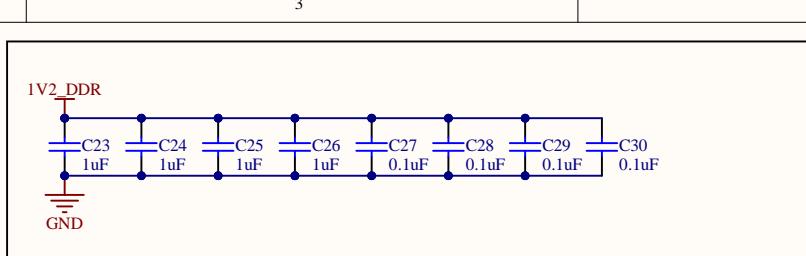
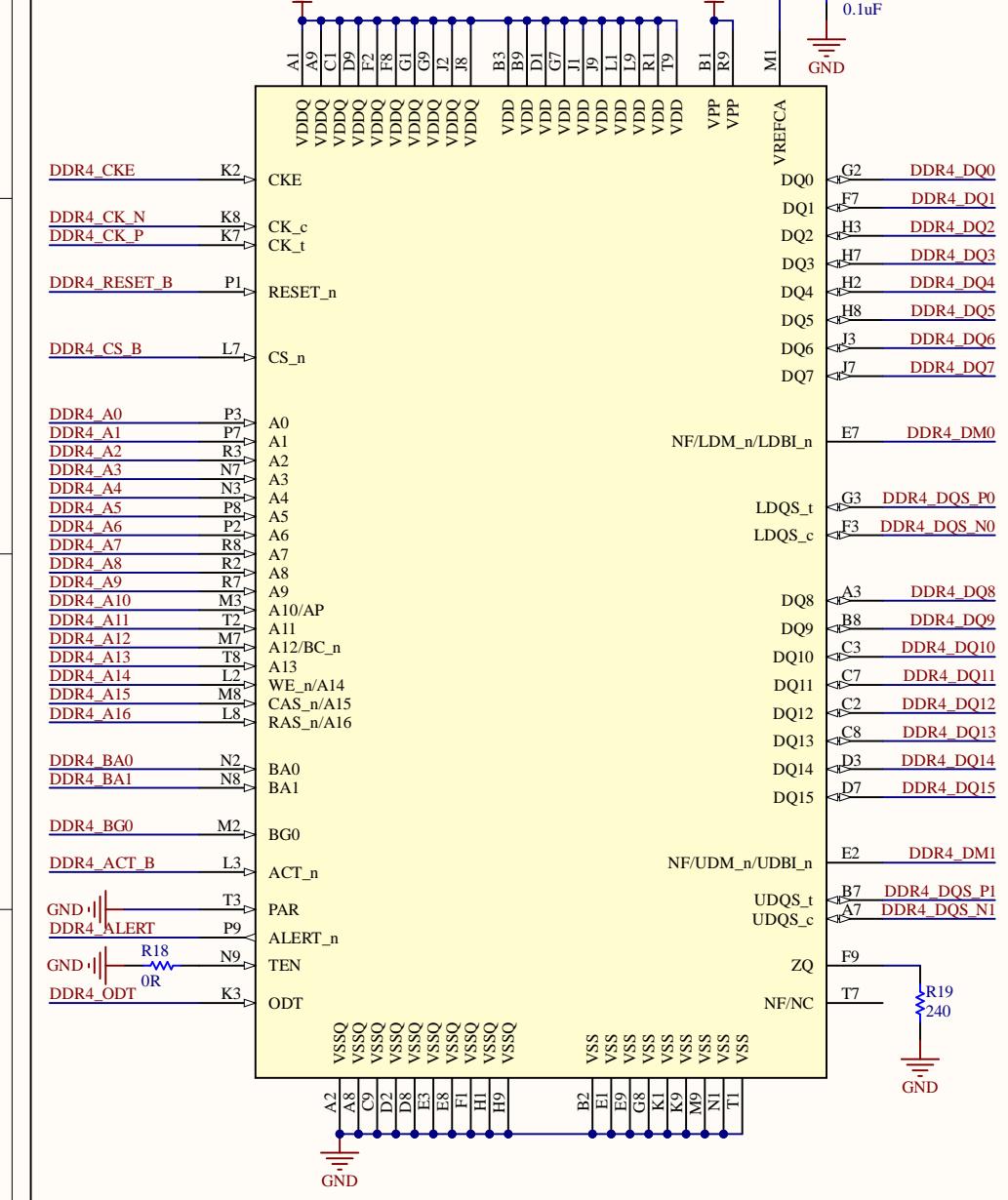
Size: A4

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Nome da Sheet: "

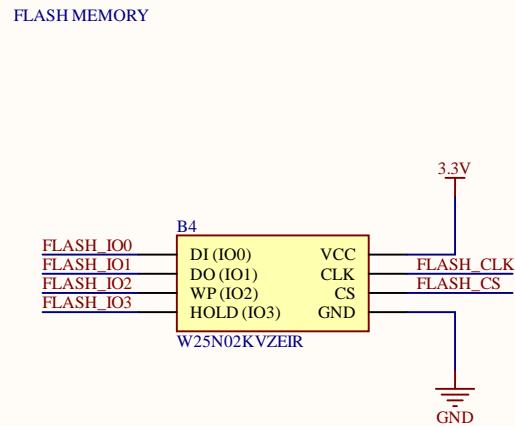
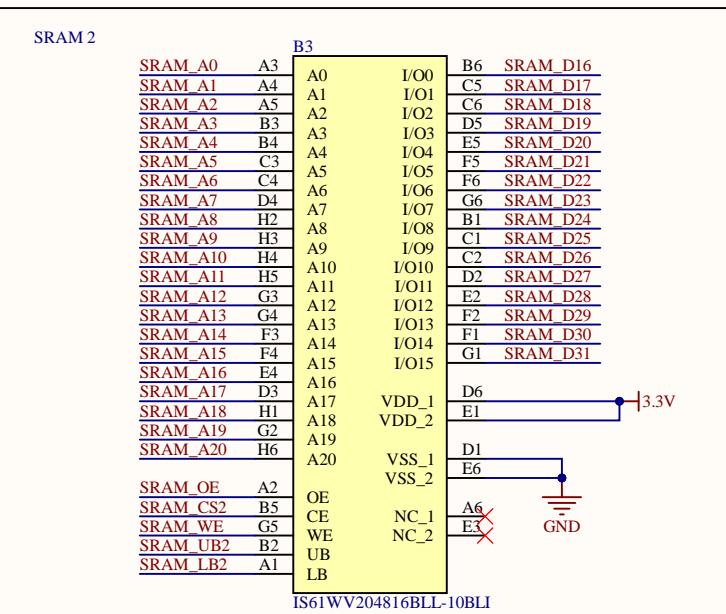
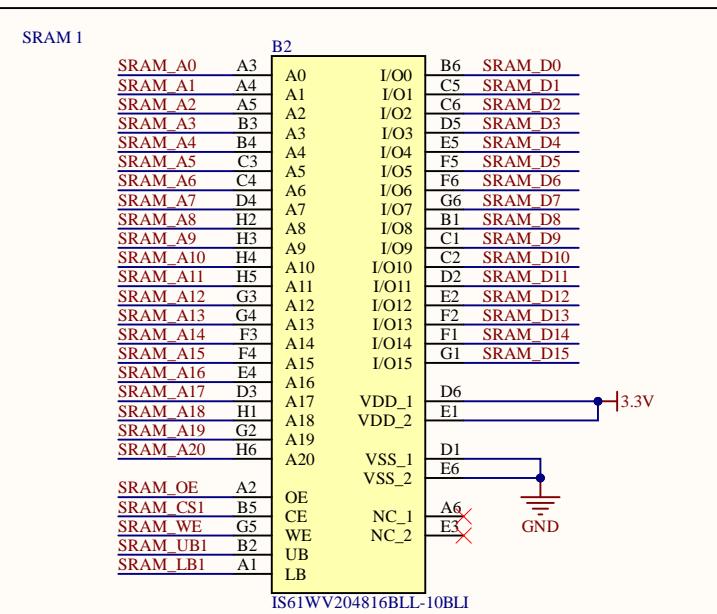
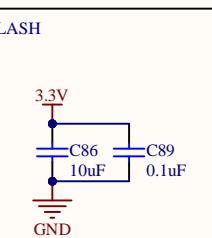
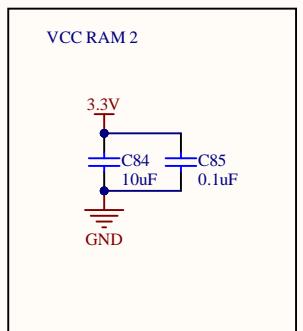
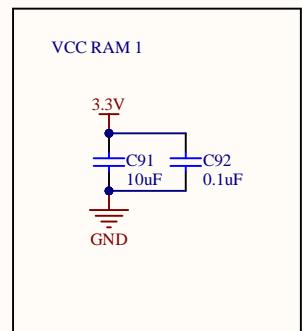
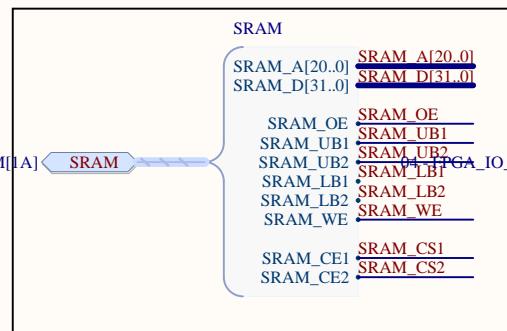
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Campus do Pici - Bloco 723, S/N - Pici, Fortaleza - CE, 60455-970

Data:

Projetista: Julio Vitorino

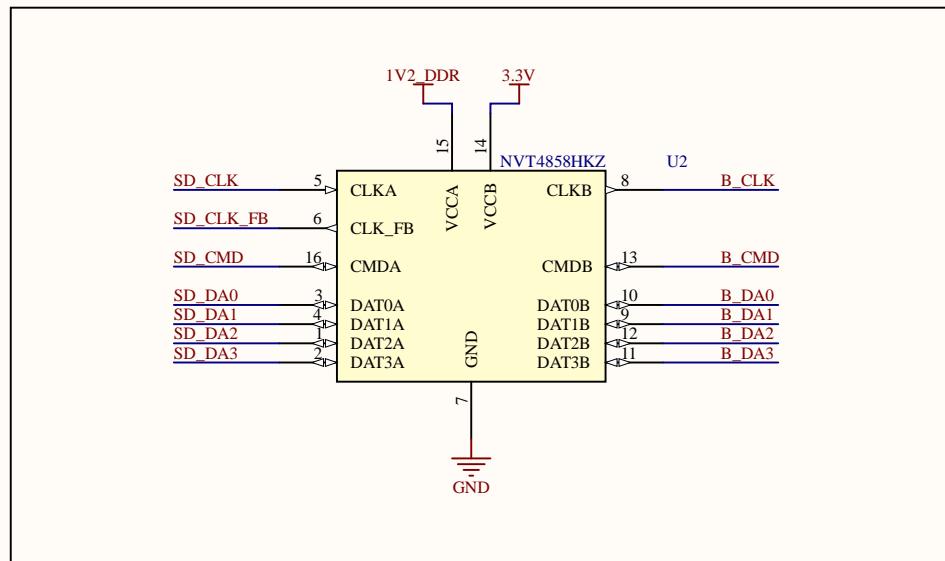
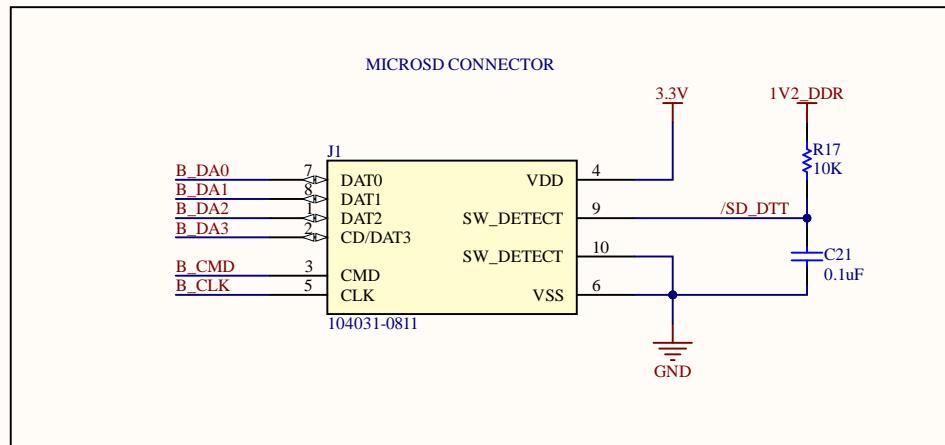
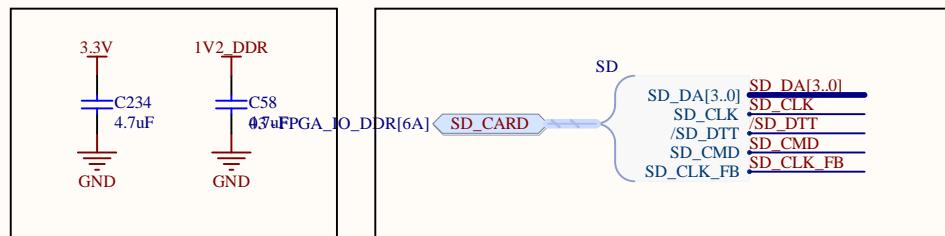
PCB Design: Julio Vitorino

Revision:  
Size: A4



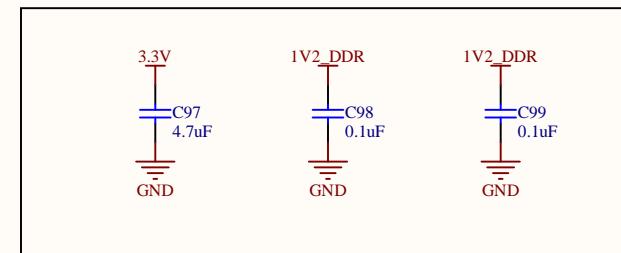
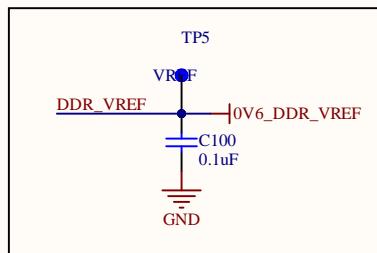
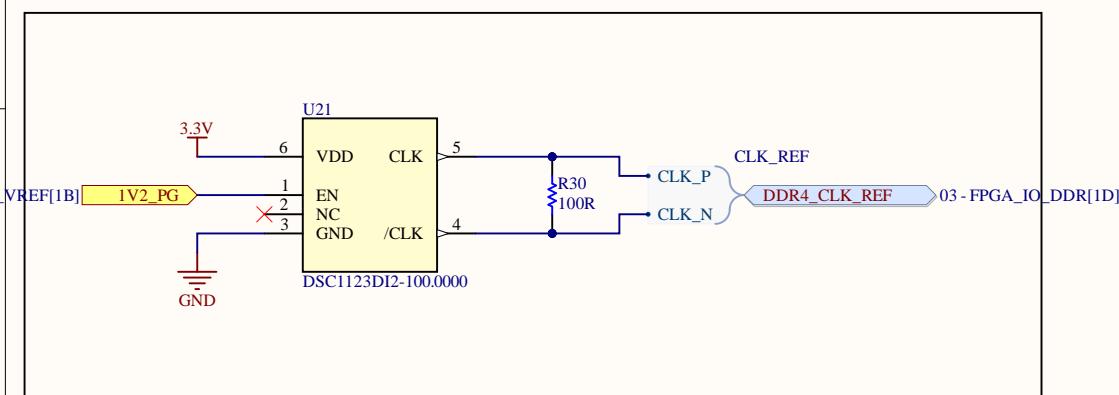
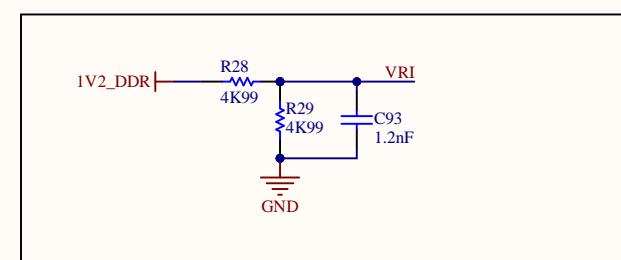
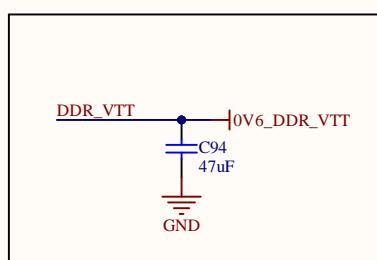
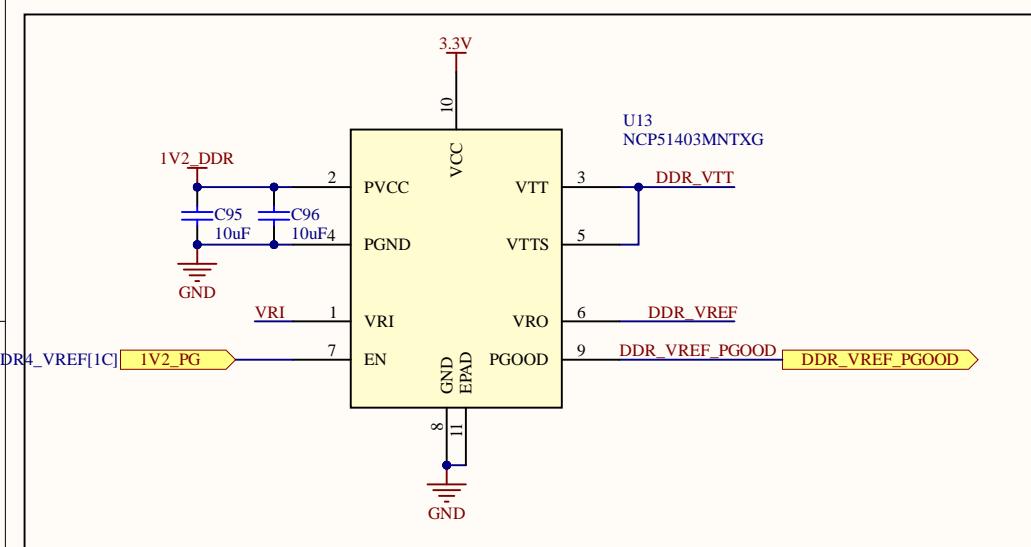
Nome da Sheet: "

LESC - Laboratório de Engenharia e Sistemas de Computação	
Campus do Pici - Bloco 723, S/N - Pici, Fortaleza - CE, 60455-970	
Data:	
Projetista:	Julio Vitorino
PCB Design:	Julio Vitorino
Revision:	
Size:	A4



Nome da Sheet: "

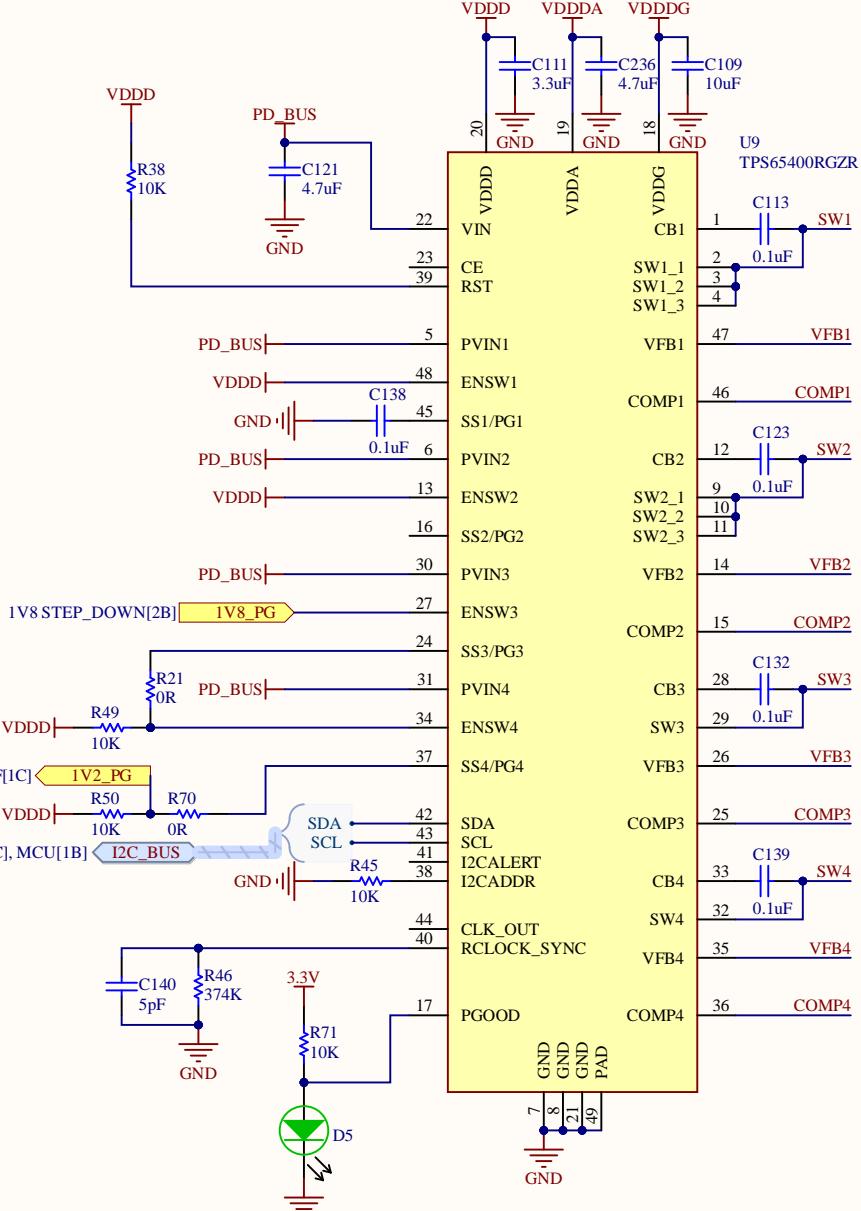
LESC - Laboratório de Engenharia e Sistemas de Computação	
Campus do Pici - Bloco 723, S/N - Pici, Fortaleza - CE, 60455-970	
Data:	
Projetista:	Julio Vitorino
PCB Design:	Julio Vitorino
Revision:	
Size:	A4



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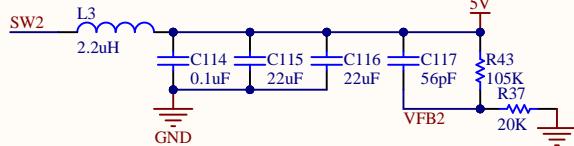
Title		
Size	Number	Revision
A4		
Date:	11/17/2025	Sheet of
File:	C:\Users\...\DDR4_VREF.SchDoc	Drawn By:

A

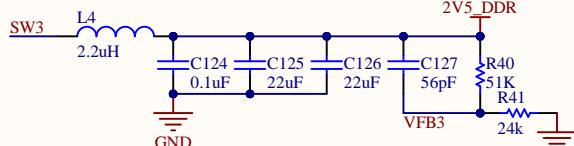


B

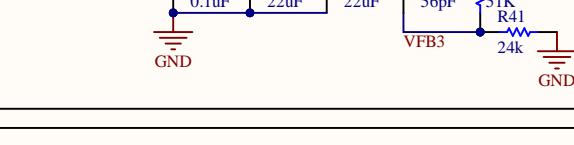
VFB1



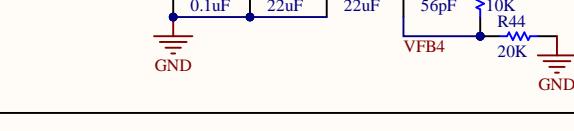
VFB2



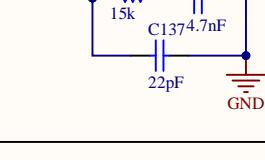
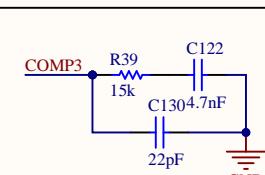
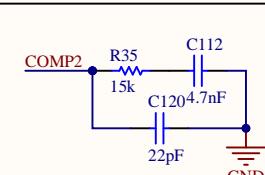
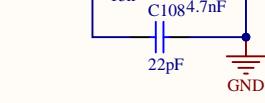
VFB3



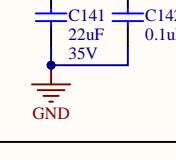
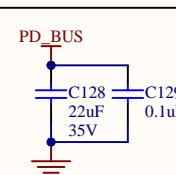
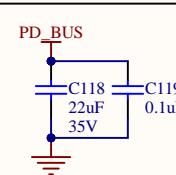
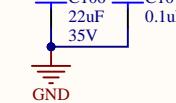
VFB4



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Nome da Sheet: "

LESC - Laboratório de Engenharia e Sistemas de Computação  
Campus do Pici - Bloco 723, S/N - Pici, Fortaleza - CE, 60455-970

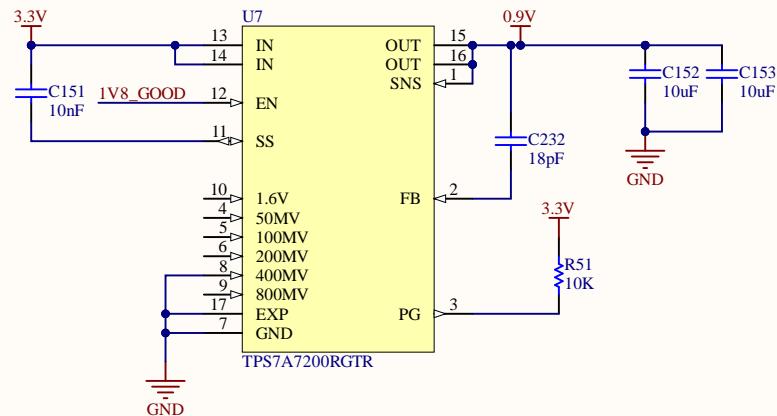
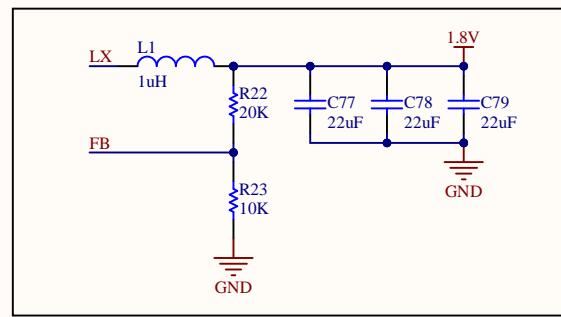
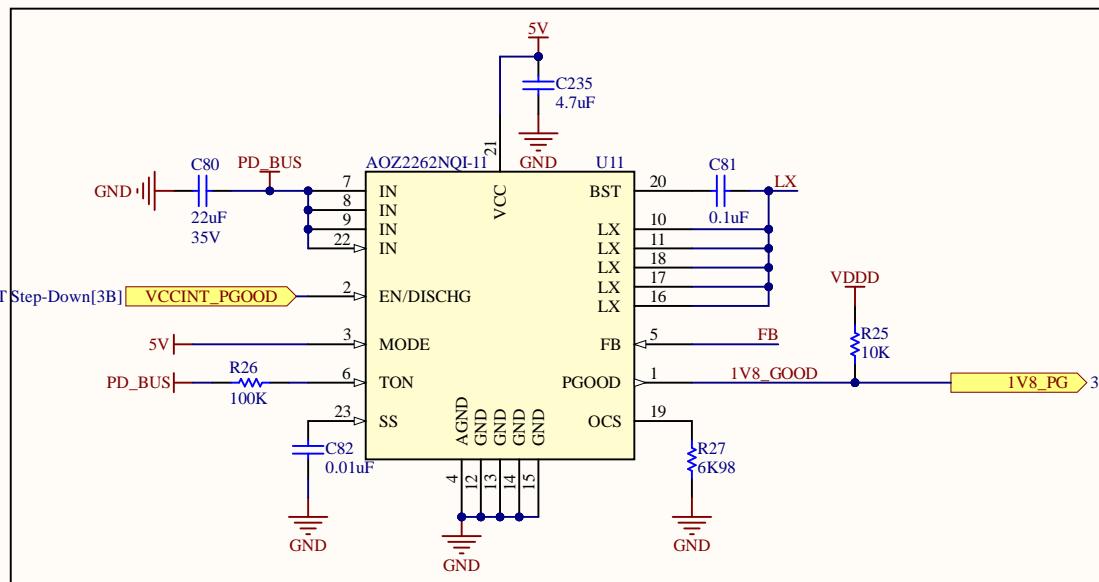
Data:

Projetista: Julio Vitorino

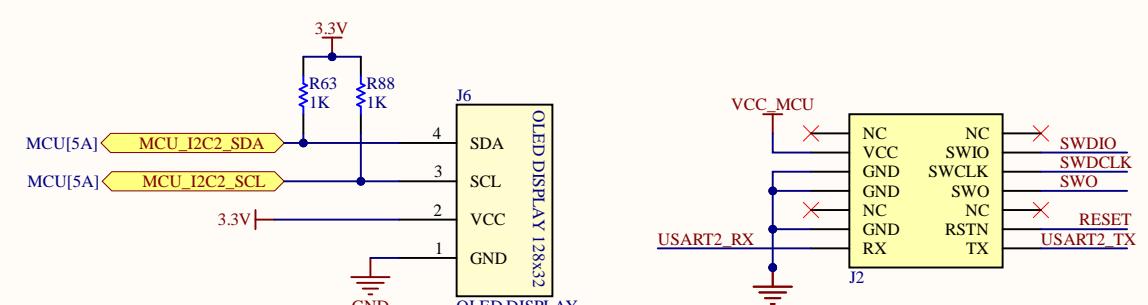
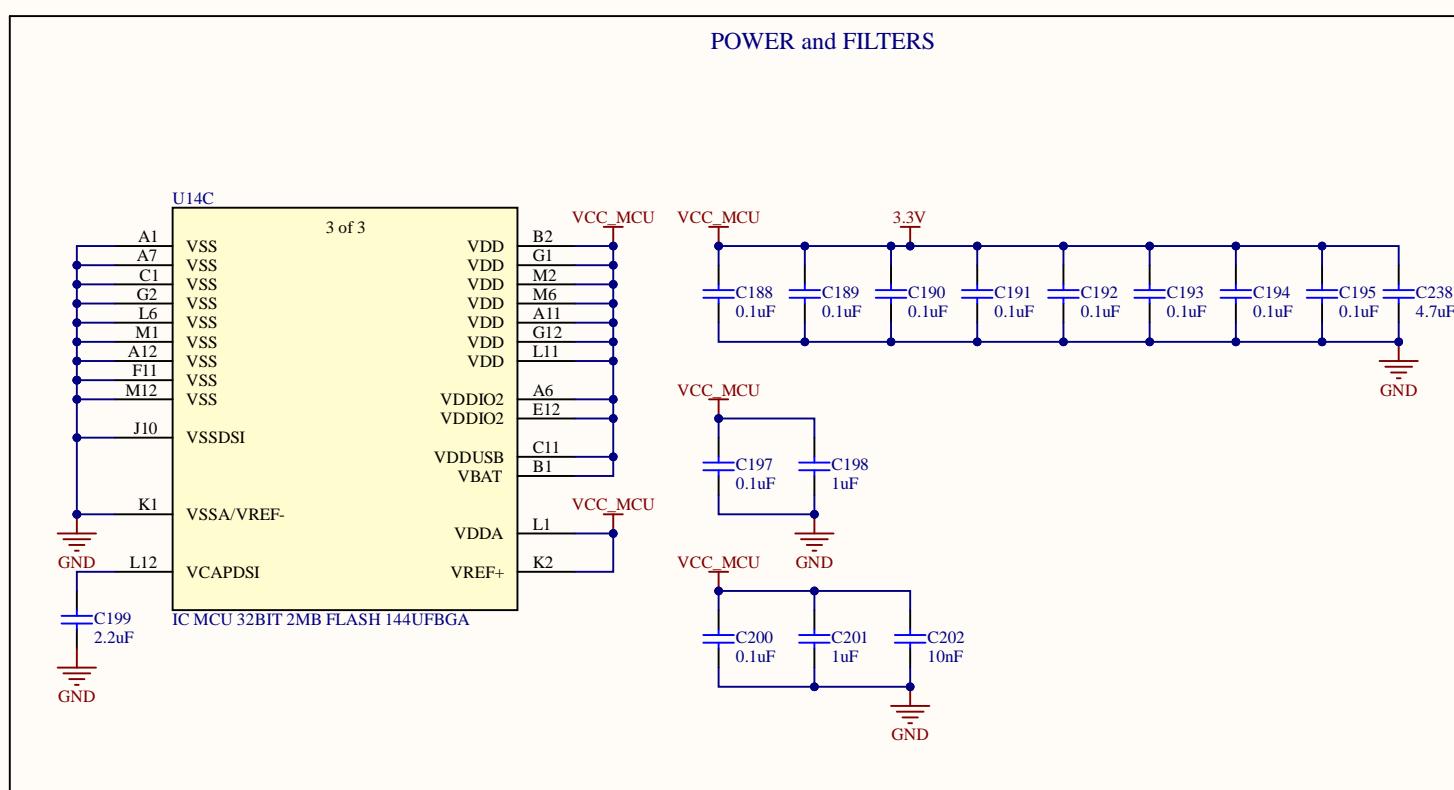
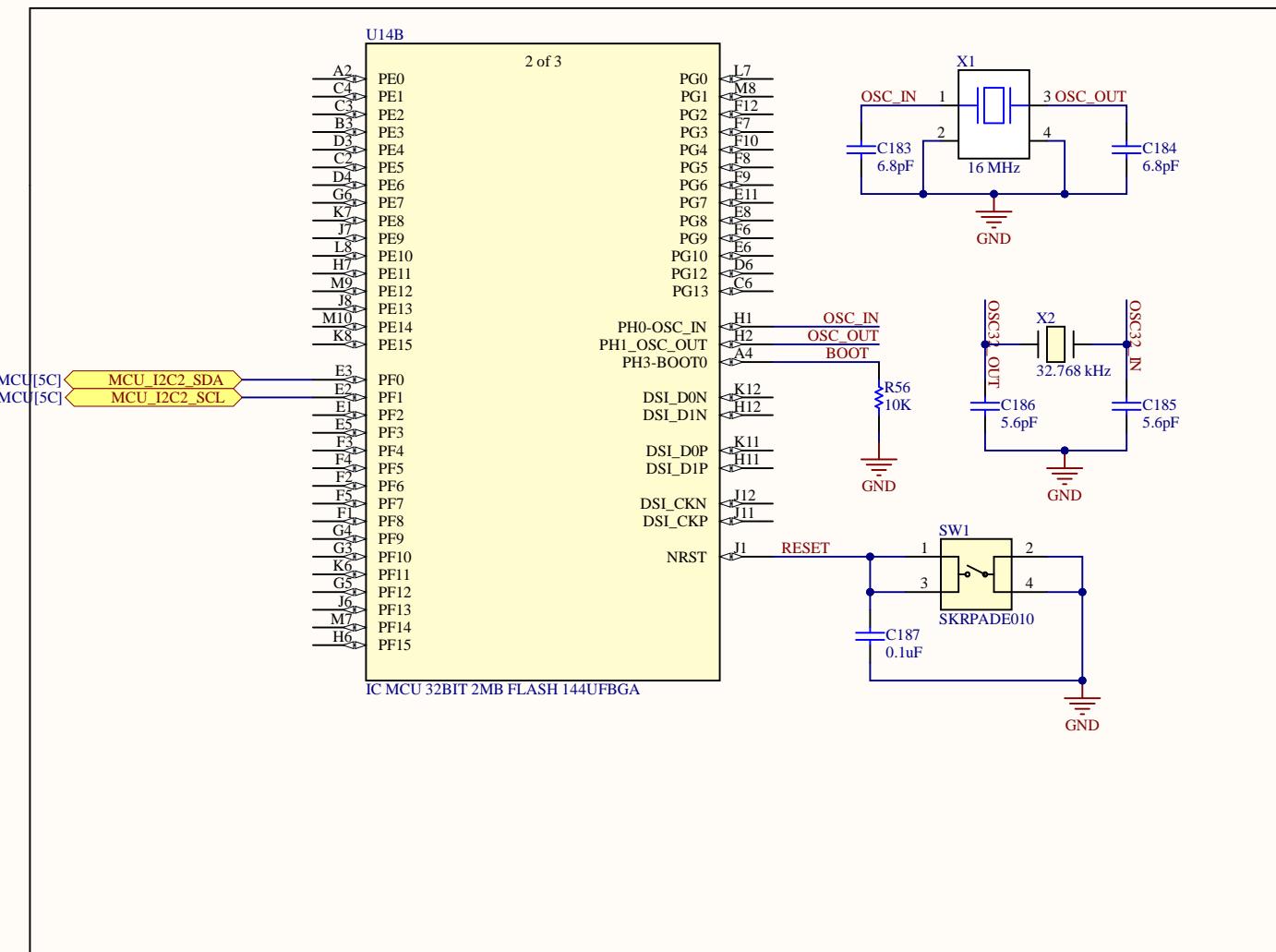
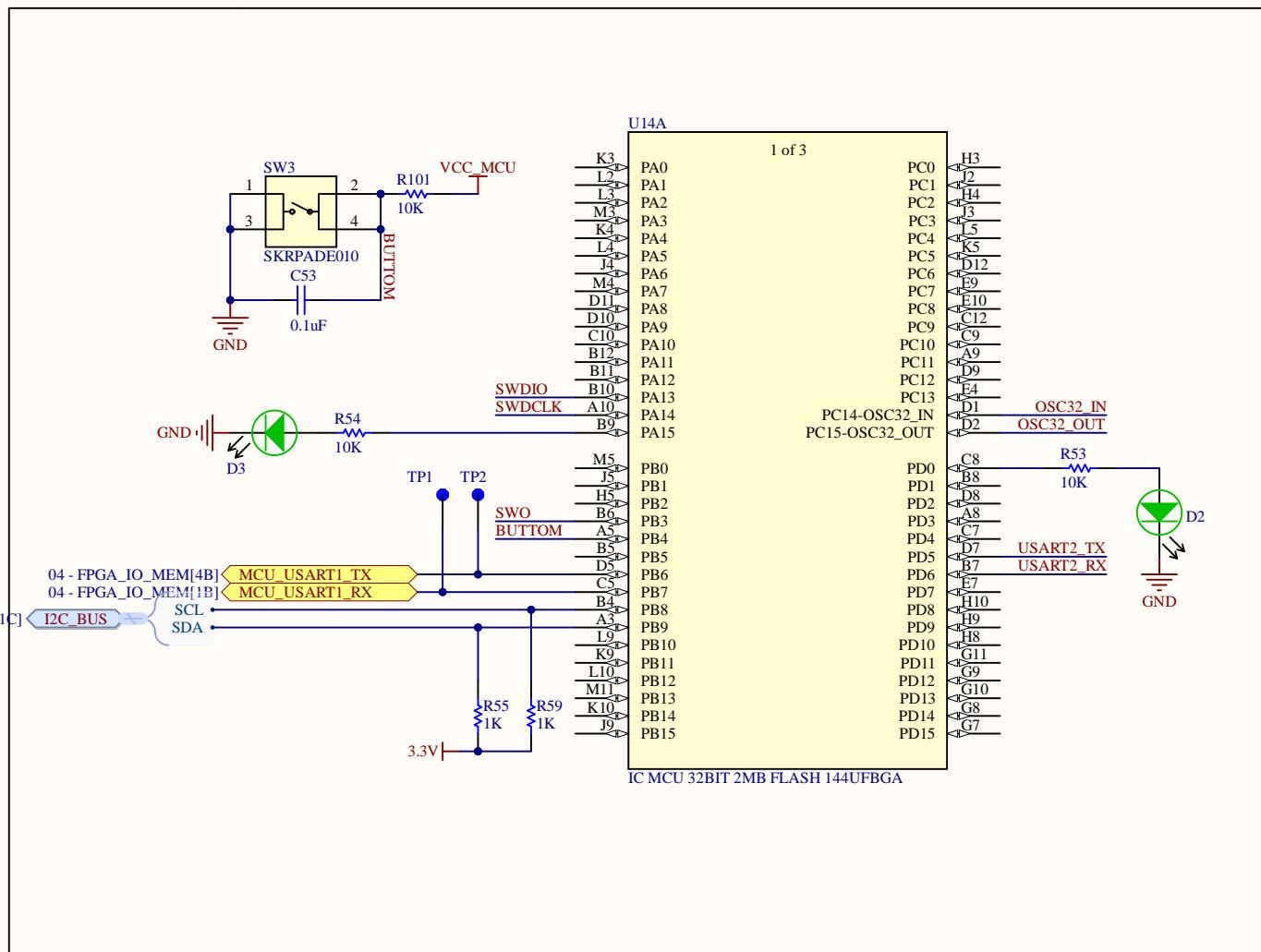
PCB Design: Julio Vitorino

Revision:

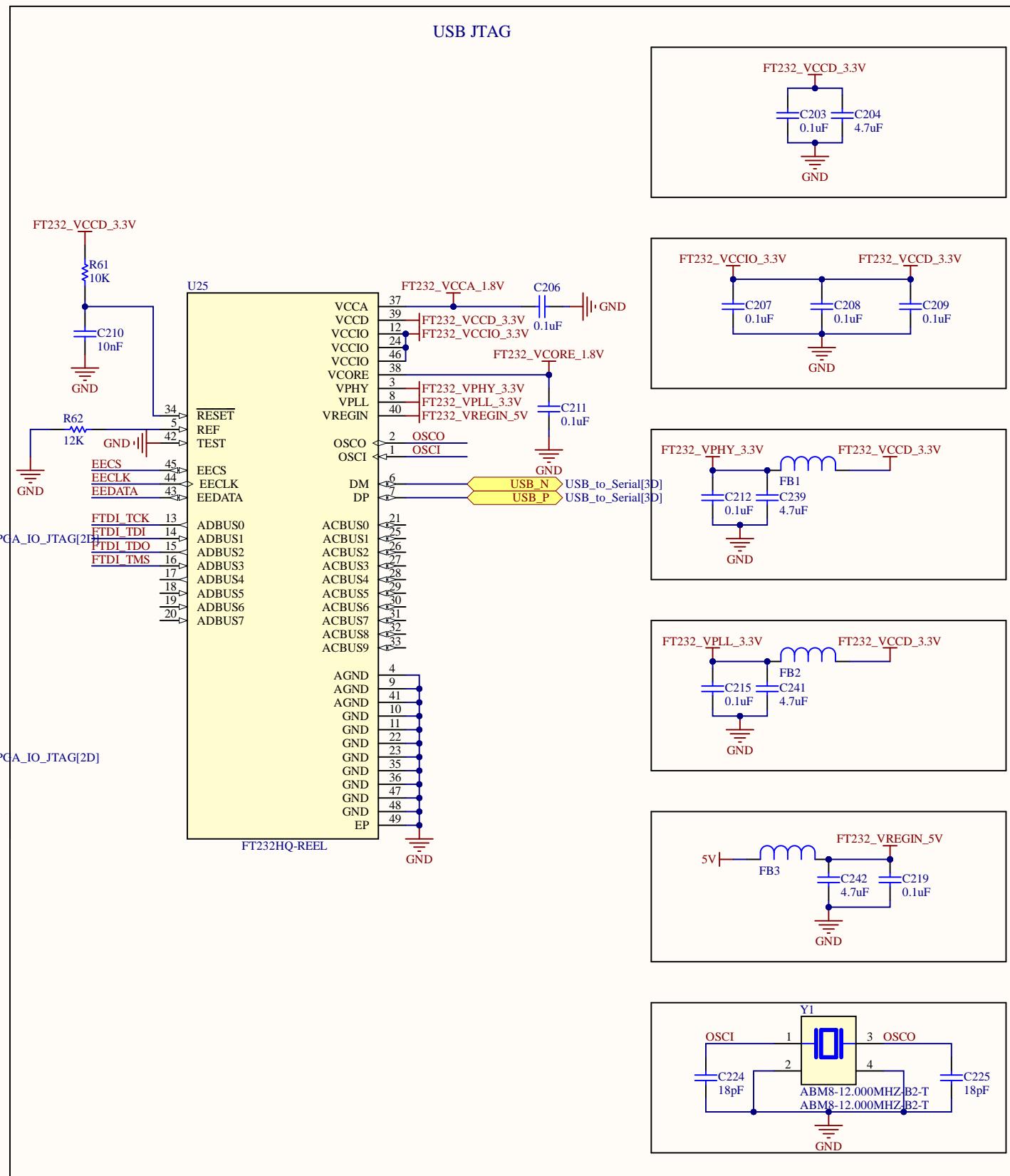
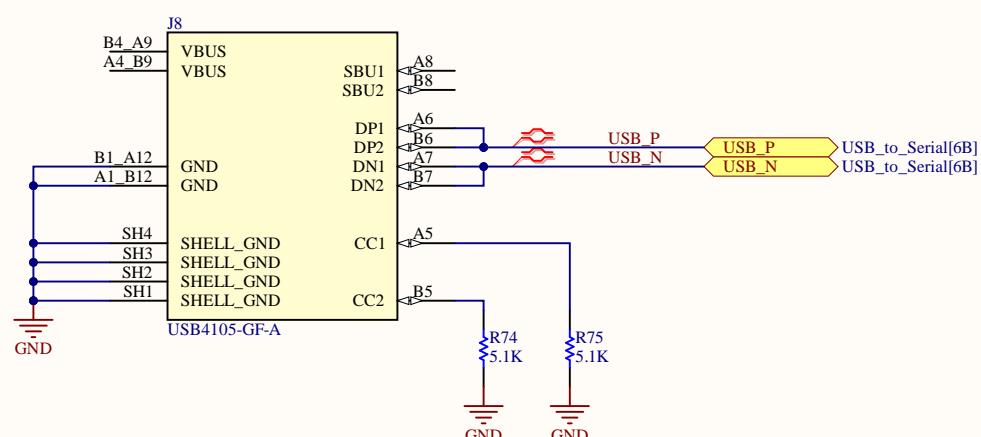
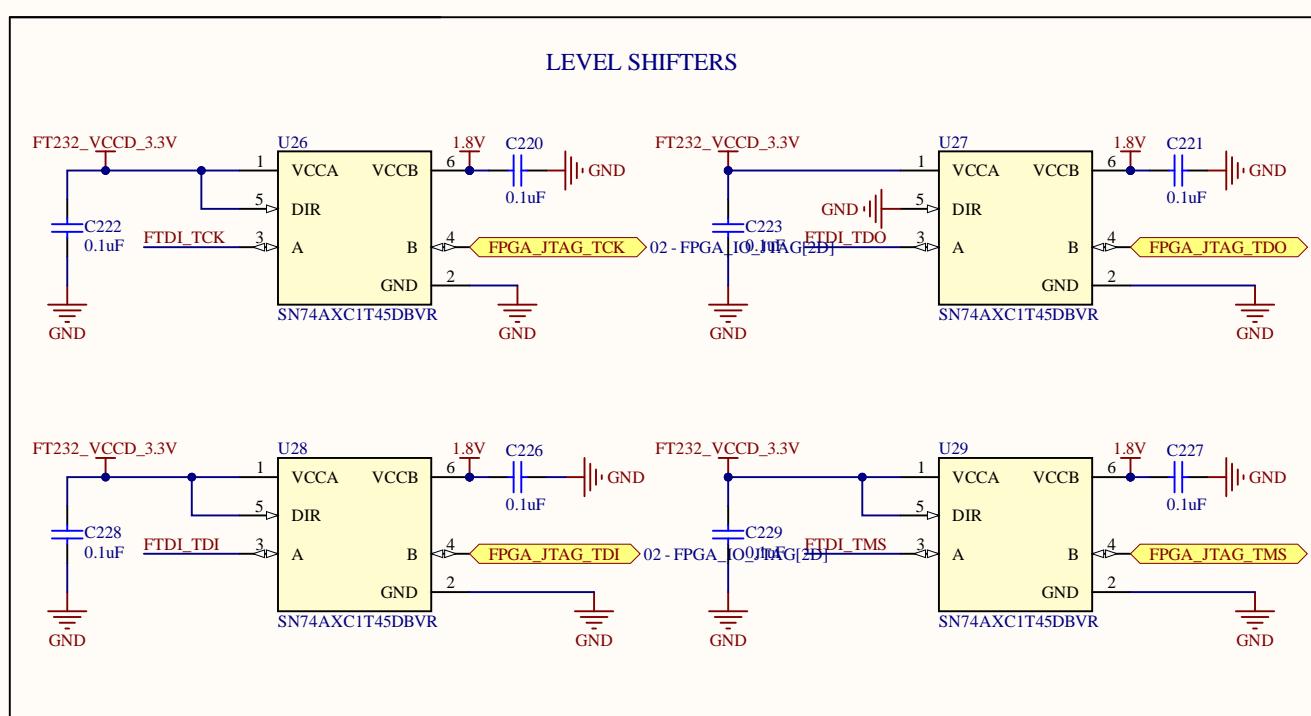
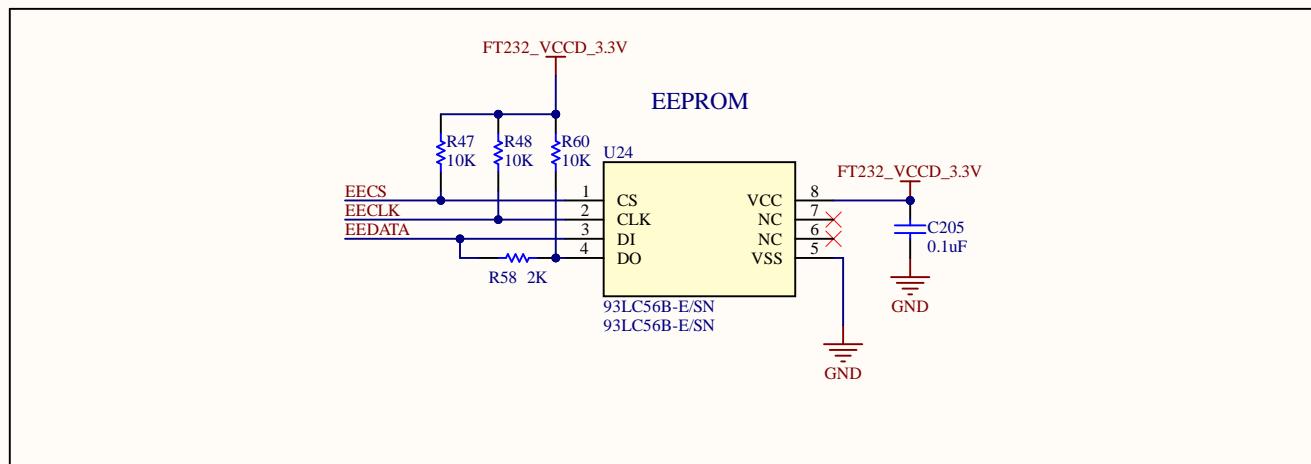
Size: A4



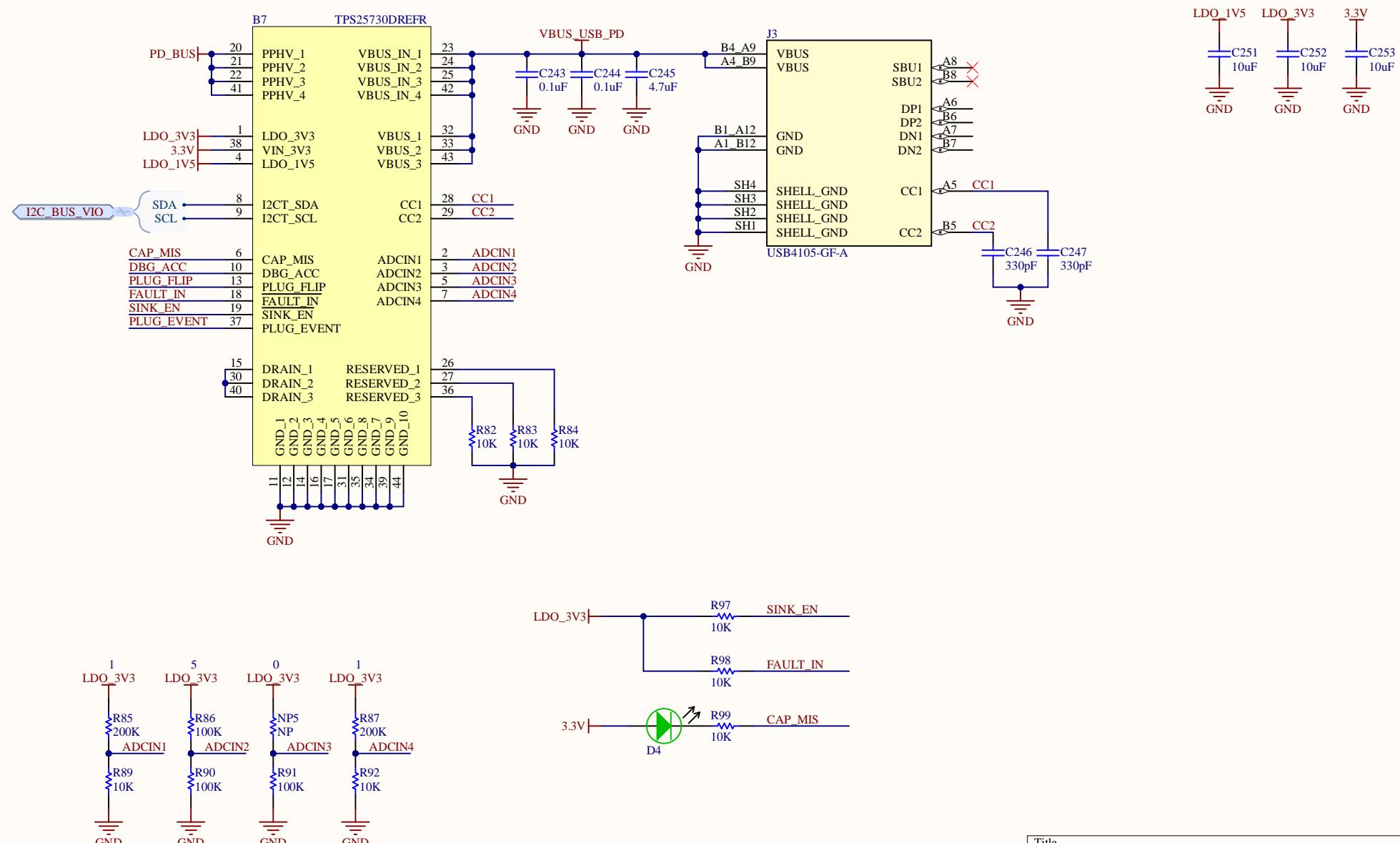
Title		
Size	Number	Revision
A4		
Date:	11/17/2025	Sheet of
File:	C:\Users\...\IV8 STEP_DOWN.SchDoc	Drawn By:



Title		
Size	Number	Revision
A3		
Date: 11/17/2025	Sheet of	
File: C:\Users\...\MCU.SchDoc		Drawn By:

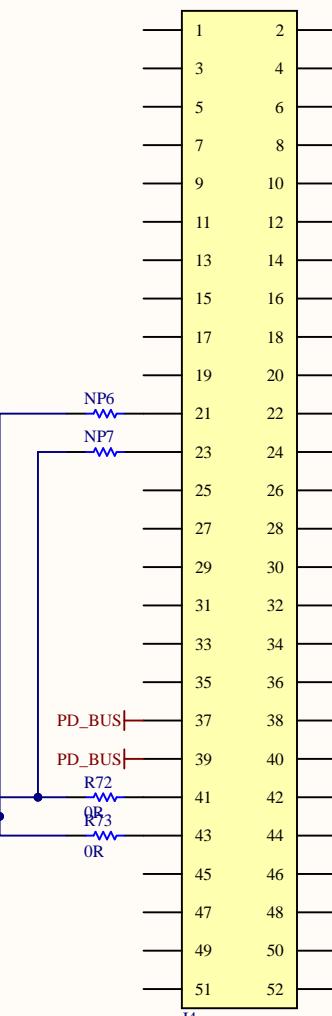


Title		
Size	Number	Revision
A3		
Date: 11/17/2025	Sheet of	
File: C:\Users\...\USB_to_Serial.SchDoc	Drawn By:	

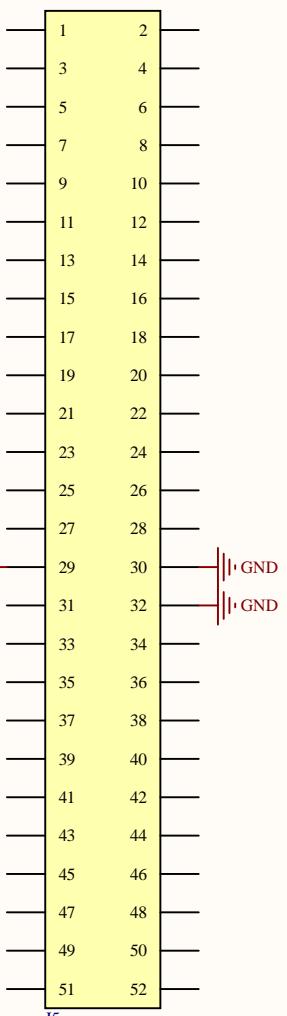


Title		
Size A4	Number	Revision
Date: 11/17/2025		Sheet of
File: C:\Users\...\USB_PD.SchDoc		Drawn By:

A

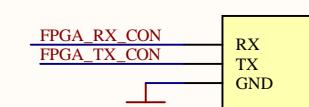
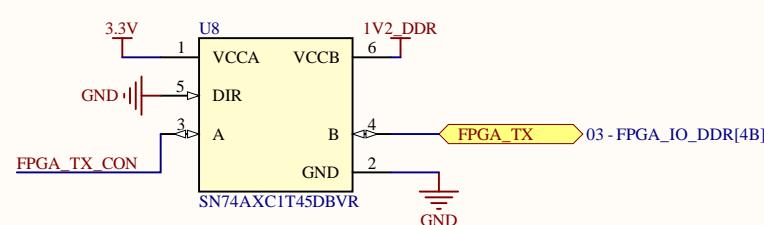
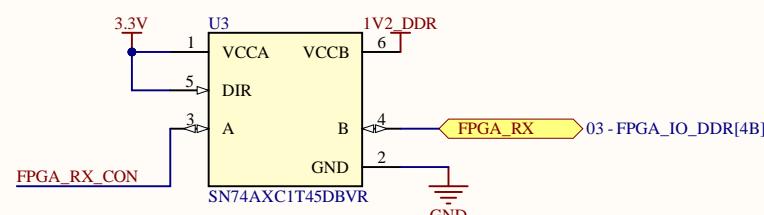
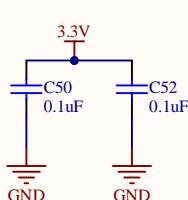


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