

Experiment 1
Biasing of Common-Emitter Amplifiers

Laboratory Report for ENGE 312
Applications of Electronic Devices

George Fox University
Newberg, OR
Jan 29, 2026

Daniel Blue, Ethan Searls, Levi Interian-Uc

I. PROJECT DESCRIPTION

The gain and bias stability of a common-emitter amplifier circuit was investigated in this laboratory experience. The gain of the amplifier was measured and compared between β values. Max Voltage Swing ($V_{o,p-p}$) was also measured and compared between β values.

II. THEORETICAL BACKGROUND

Consider the circuit shown in Fig. 1. It is a bjt amplifier in the common-emitter configuration. It consists of a NPN Bipolar Junction Transistor (BJT), some resistors, a power source, and some DC filtering capacitors. A BJT has three operating regions. They are the active, saturation, and cutoff regions. In order to amplify an input signal with minimal distortion, the most linear region must be used. Crossing into a nonlinear region adds distortion to the output signal. The linear region for a BJT is the active region.

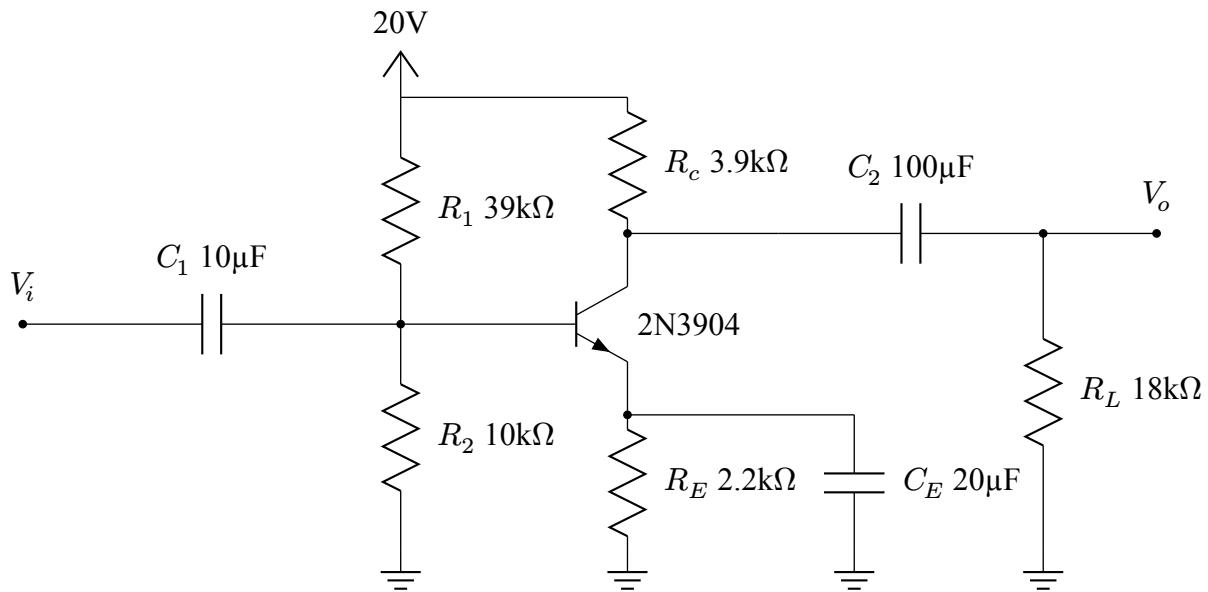


Fig. 1. BJT Amplifier in the Common-Emitter Configuration

Due to the physical construction of the BJT, when there is a small current through the base (I_B), a larger current goes through the collector (I_C). The relationship is shown in Equation 1, where β is the DC current gain.

$$I_C = \beta I_B \quad (1)$$

Most amplifier designs are voltage amplifiers, but this amplifies current. Voltage can be amplified by placing a load resistor (R_L) at the collector node, going to ground.

To ensure complete operation in the active region, V_B can be biased using a simple voltage divider from a voltage source. Equation 2 and Equation 3 show how get a Thevenin equivalent from the voltage divider to set our DC bias.

$$R_B = R_1 \parallel R_2 \quad (2)$$

$$V_{BB} = \left(\frac{R_2}{R_1 + R_2} \right) (V_{CC}) \quad (3)$$

The formulas for the quiescent current and voltage, which account for the effect of the emitter resistor R_E on stability, are given by Equation 4 and Equation 5.

$$I_{CQ} = \frac{V_{BB} - V_{BE}}{\left(\frac{R_E}{\alpha} \right) + \left(\frac{R_B}{\beta} \right)} \quad (4)$$

$$V_{CEQ} = V_{CC} - \left(R_{CC} + \frac{R_E}{\alpha} \right) I_{CQ} \quad (5)$$

β and α are related using Equation 6. This means that $\alpha < 1$

$$\alpha = \frac{\beta}{\beta + 1} \quad (6)$$

Due to the fact that the β of a transistor can vary dramatically between individual units (even amongst those within the same model), some manner of bias stability must be ensured, so that a design can be implemented with less restrictive component tolerances. This is at the sacrifice of some amplifier performance. Generally, to be considered stable the design must satisfy two conditions, that $V_{BB} \gg V_{BE}$ and $R_E \gg \frac{R_B}{\beta+1}$. Without ensured bias stability, the Q point of the amplifier could swing drastically depending on the β of the transistor used, causing amplification to enter the cutoff or saturation regions, which would lead to clipping and harmonic distortion.

An amplifier also doesn't have the same performance over the entire frequency spectrum, the bandwidth can be calculated using Equation 7, where f_{upper} and f_{lower} are 3dB down from the max gain.

$$f_{midband} = \sqrt{f_{lower} * f_{upper}} \quad (7)$$

III. METHODS AND MATERIALS

A. Equipment

Table 1. Bench laboratory equipment used in this procedure.

Manufacturer	Serial Number	Function
Tektronix	CPS250	Power Supply
Tektronix	TDS2024C	Oscilloscope
Fluke	45	Digital Multimeter
VOLTEQ	SFG-1010	Function Generator

B. Experimental Procedure

The circuit in Fig. 1 was constructed as shown, save for the R_E resistor, which was changed to $2k\Omega$ due to insufficient resistor values in the lab. V_i was connected to the function generator. V_{CC} was connected to the benchtop power supply. All Q-point node voltages were recorded and verified, as well as verifying that $V_{BE} = +0.7V$. The DC blocking of the capacitors was also verified. From the data, I_{CQ} and V_{CE} were calculated. These were then compared to the prelab results. β was calculated using the measured and calculated voltages, and then compared to the measured β from the multimeters hfe measurement mode.

The function generator was then turned on and set to 50 kHz. Using the oscilloscope, the v_i and v_o were measured, and the amplitude of the waveform from the function generator was adjusted until the v_o waveform appeared to be a pure sine wave (with the exception of some noise). The max output peak-to-peak voltage was measured by adjusting the input voltage until just before it started clipping. To verify the voltage swing was measured with a waveform that had minimal harmonic distortion or clipping, an FFT was taken of the output signal. The peak-to-peak values of v_i and v_o .

Similar steps were then repeated with a different BJT transistor to verify the effects of a change in β , and how effective the bias stability provided by R_E is.

Bandwidth measurements were taken by using the function generator to scan through the frequency spectrum to observe if the amplifiers gain increased substantially. High and low drop off frequencies were recorded, these became f_{upper} and f_{lower} respectively. These are the points where the output has dropped by a factor of 0.707. The midband frequency f_{mid} was calculated using the geometric mean.

Laboratory analysis included comparing theoretical and experimental Q values, gain results, as well as differences between the two transistors used based on their differing β values. Bias stability conditions were also checked.

IV. RESULTS

Table 2. Comparison of theoretical and measured DC biasing results for the first transistor (Beta ≈ 168)

Parameter	Theoretical	Measured	% Diff
Beta (hFE)	168.0	168.0	0.0%
V_BE	0.7 V	0.67 V	4.38%
V_BQ	4.08 V	4.0 V	1.96%
V_EQ	3.38 V	3.33 V	1.48%
V_CQ	13.1 V	11.7 V	10.69%
I_CQ	1.77 mA	1.9 mA	7.06%
V_CEQ	9.15 V	8.37 V	8.56%

Table 3. DC biasing results for the lower-gain second transistor (Beta ≈ 58.7)

Parameter	Theoretical	Measured	% Diff
Beta (hFE)	58.7	58.7	0.0%
V_BE	0.7 V	0.673 V	4.0%
V_BQ	4.08 V	3.9 V	4.41%
V_EQ	3.38 V	3.31 V	2.07%
V_CQ	13.41 V	11.6 V	13.5%
I_CQ	1.69 mA	1.01 mA	34.0%
V_CEQ	9.62 V	13.8 V	43.45%

Table 4. Experimental DC results comparing both transistors for bias stability evaluation

Parameter	First Transistor	Second Transistor	% Diff
Beta	168.0	58.7	96.43%
V_BQ	4.0 V	3.9 V	2.53%
V_EQ	3.33 V	3.31 V	0.60%

Parameter	First Transistor	Second Transistor	% Diff
V_CQ	11.7 V	11.6 V	0.85%
I_CQ	1.9 mA	1.01 mA	61.17%
V_CEQ	8.37 V	13.8 V	49.07%

Table 5. Comparison of theoretical calculations and experimental midband gain for the first transistor

Parameter	Theoretical	Measured	% Diff
Input Voltage (V _{p-p})	0.080 V	0.0792 V	1.00%
Output Voltage (V _{p-p})	1.47 V	1.44 V	2.04%
Voltage Gain (Av)	18.4	18.18	1.20%

Table 6. Measured midband voltage gain and output characteristics comparison between transistors

Metric	Transistor 1	Transistor 2
% Diff		
12.2 V	7.4 V	Max Negative Swing (V _{o min})
-1.6 V	N/A	Max Undistorted P-P (V _{p-p})
1.44 V	7.4 V	Input Voltage (V _{in})
0.0792 V	0.44 V	Midband Voltage Gain (Av)
18.18	16.81	

Table 7. Numerical verification of DC bias stability design constraints (10x Factor)

Condition	Target Ratio	Actual Ratio	Status
V_BB / V_BE (T1)	> 10	6.09	Not Met (Partial)
V_BB / V_BE (T2)	> 10	5.79	Not Met (Partial)
R_E / [R_B / (B1+1)]	> 10	46.7	Met
R_E / [R_B / (B2+1)]	> 10	16.5	Met

Table 8. Measured frequency characteristics and bandwidth of the amplifier circuit

Parameter	Measured Frequency
Lower Cutoff Frequency (f_{lower})	150 Hz
Upper Cutoff Frequency (f_{upper})	2.4 MHz
Calculated Midband Frequency (f_{mid})	18.97 kHz
Measured Bandwidth	2.399 MHz

A. Sample Calculations

$$V_{BB} = V_{CC} \cdot \frac{R_2}{R_1 + R_2} = 20 \text{ V} \cdot \frac{10 \text{ k}\Omega}{39 \text{ k}\Omega + 10 \text{ k}\Omega} \approx 4.08 \text{ V}$$

$$R_B = R_1 \parallel R_2 = \frac{R_1 \cdot R_2}{R_1 + R_2} = \frac{39 \text{ k}\Omega \cdot 10 \text{ k}\Omega}{39 \text{ k}\Omega + 10 \text{ k}\Omega} \approx 7.96 \text{ k}\Omega$$

$$V_{CQ} = V_{CC} - I_{CQ} \cdot R_C = 20 \text{ V} - (1.50 \text{ mA} \cdot 3900\Omega) \approx 14.15 \text{ V}$$

$$V_{EQ} = I_E \cdot R_E = 1.50 \text{ mA} \cdot 2200\Omega \approx 3.31 \text{ V}$$

Biasing

$$I_{CQ} \approx I_E = \frac{V_{BB} - V_{BE}}{R_E + \frac{R_B}{168+1}} = \frac{4.08 \text{ V} - 0.7 \text{ V}}{2200\Omega + \frac{7959\Omega}{168+1}} \approx 1.50 \text{ mA}$$

$$V_{CEQ} = V_{CQ} - V_{EQ} = 14.15 \text{ V} - 3.31 \text{ V} = 10.84 \text{ V}$$

Voltage Gain

$$A_v = \frac{v_o}{v_i} = \frac{1.44V_{p-p}}{0.0792V_{p-p}} \approx 18.18$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{1.50 \text{ mA}}{25 \text{ mV}} = 0.06 \text{ S}$$

$$r_e = \frac{1}{g_m} \approx 16.7\Omega$$

$$A_v \approx -\frac{R_C \parallel R_L}{r_e + R_{E1}}$$

Bias Stability

$$V_{BB} \gg V_{BE} \rightarrow 4.08 \text{ V} \gg 0.7 \text{ V} \quad (\checkmark)$$

$$R_E \gg \frac{R_B}{168+1} \rightarrow 2200\Omega \gg \frac{7959\Omega}{169} \approx 47.1\Omega \quad (\checkmark)$$

Bandwidth and Percent Difference

$$f_{mid} = \sqrt{f_{lower} \cdot f_{upper}} = \sqrt{150 \text{ Hz} \cdot 2.4 \text{ MHz}} \approx 19.0 \text{ kHz}$$

$$\text{Diff \%} = \left| \frac{\text{Theoretical} - \text{Measured}}{\text{Theoretical}} \right| \cdot 100\%$$

$$\text{Diff \%} = \left| \frac{1.50 \text{ mA} - 1.90 \text{ mA}}{1.50 \text{ mA}} \right| \cdot 100\% \approx 26.7\%$$

V. DISCUSSION

With the initial transistor value ($168 = 168$) it looks as though the calculated and measured values are fairly similar as far as node voltages go. With the second transistor ($B = 58.7$), there seemed to be a higher percent difference overall between calculated and measured in regards to the Q point calculations, this is probably in part because of the fact the R_E got changed to $2k\Omega$ instead of $2.2k\Omega$ due to equipment constraints. Again, when comparing the two resistors the Q points did move a good amount, but that's mostly due to that resistor change, which affected the bias stability. Both transistors had similar amounts of gain, so it seems like the Q point shift didn't affect it too much. The first transistor's frequency gain band was measured, and it seemed fairly wide, covering most of the auditory frequency spectrum (save for the f_{lower} at 150Hz) and well up past 2MHz.

VI. CONCLUSIONS

The objectives of the experiment were to verify the voltage gain and DC bias stability of a common-emitter amplifier circuit. Overall the theoretical design matched the measured outcomes, and while the Q point did shift when changing transistors, similar gain capabilities were consistent from transistor to transistor. The changed resistor value likely contributed to this.