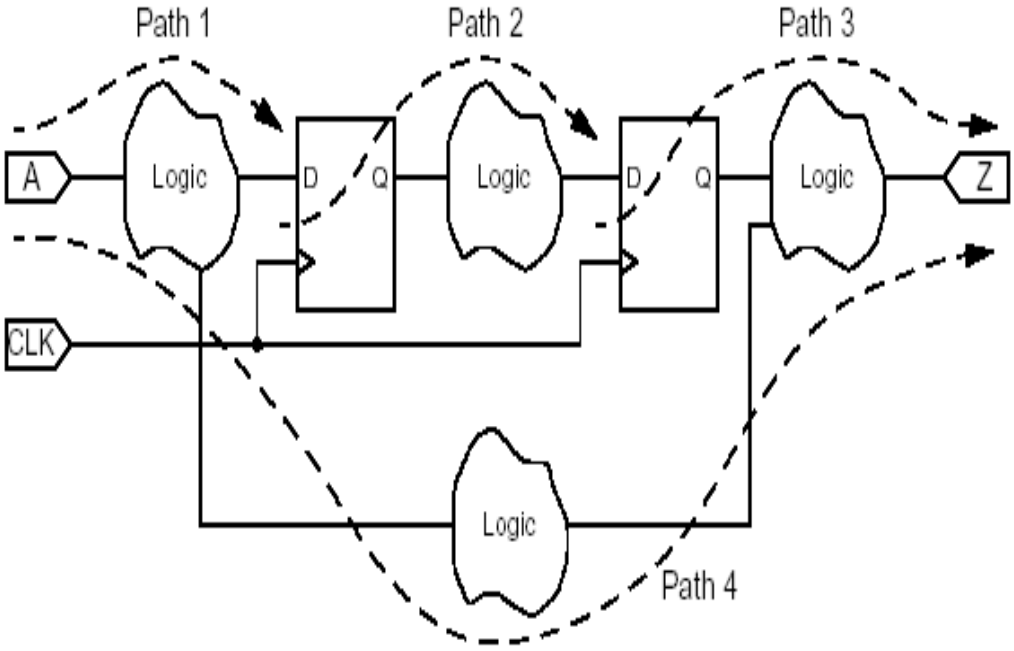
Timing Paths:

1.PrimeTime breaks the design down into a set of timing paths, calculates the signal propagation delay along each path, and checks for violations of timing constraints inside the design and at the input/output interface.

2.Each path has a startpoint and an endpoint.

3.The startpoint is a place in the design where data is launched by a clock edge.

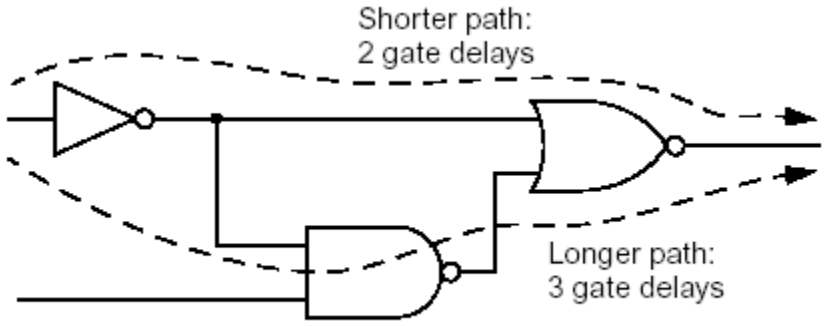
4.The data is propagated through combinational logic in the path and then captured at the endpoint by another clock edge.



1. Timing Paths

Combinatorial logic may have multiple paths

PrimeTime uses the longest path to calculate a maximum delay or the shortest path to calculate a minimum delay.



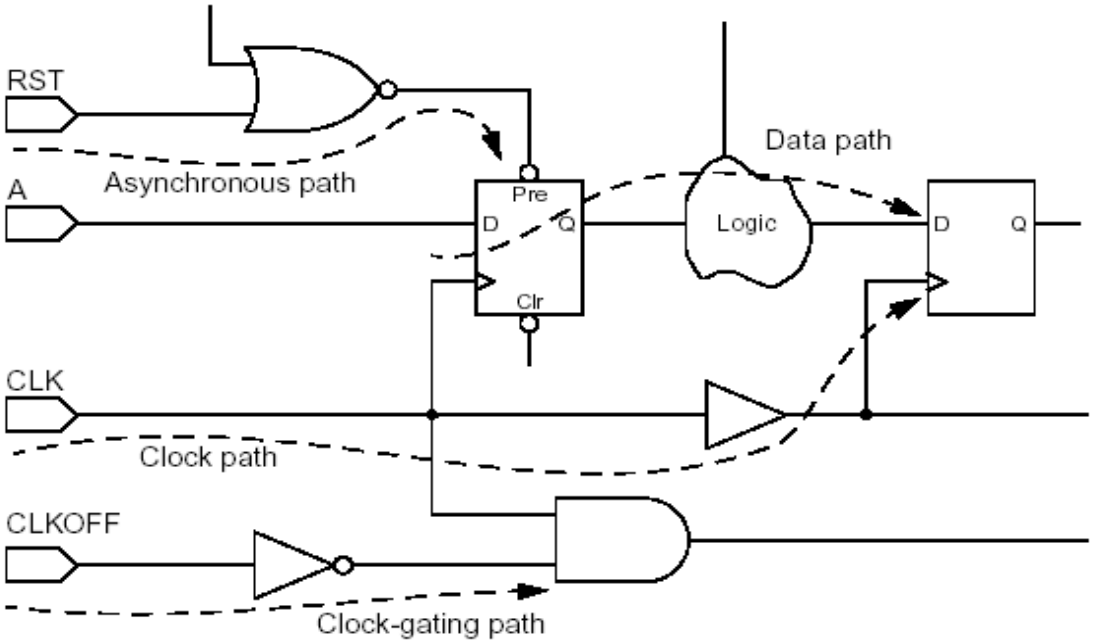
2.Delay Calculation

Other types of Timing paths

Clock path (a path from a clock input port or cell pin, through one or more buffers or inverters, to the clock pin of a sequential element) for data setup and hold checks

Clock-gating path (a path from an input port to a clock-gating element) for clock-gating setup and hold checks

Asynchronous path (a path from an input port to an asynchronous set or clear pin of a sequential element) for recovery and removal checks

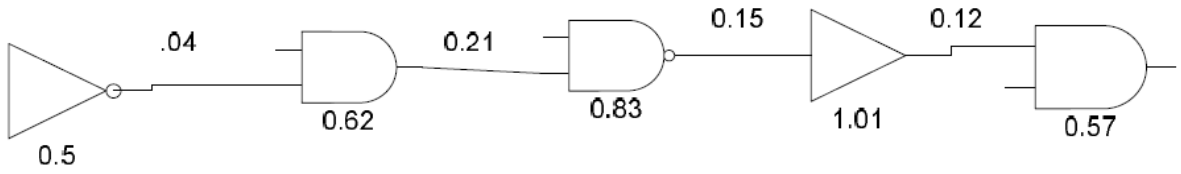


3. Types of Path

Delay Calculation of each timing path:

Once the paths are identifies, PT, calculates the delays. The total delay of a path is the sum of all cell and net delays in the path.

Calculating Tcombinational logic is very simple. The delay though the cell is added to the time thought the net. For given path below figure,



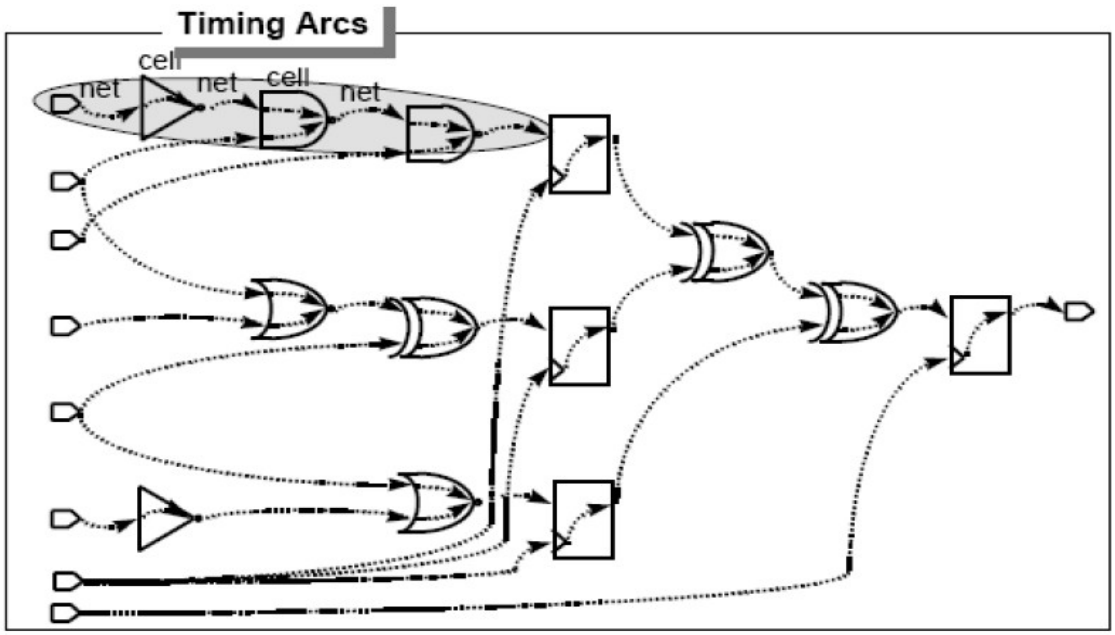
4. Delay Calculation

Tcombinational logic

= (0.5 + 0.04 + 0.62 + 0.21 + 0.83 + 0.15 + 1.01 + 0.12 + 0.57) = 4.05 ns.

STA calculates the delay along each timing path by determining the Gate delay and Net delay.

Gate Delay: Amount of delay from the input to the output of a logic gate. It is calculated based on 2 parameters a. Input Transition Time b. Output Load Capacitance



5. Timing Arcs

1. The total path delay is the addition of all the net and cell delay.

2. When PrimeTime analyzes a path, it must keep track of edge sensitivity or unateness.

3. If PrimeTime used the only largest or smallest delay when calculating the path delay, the results would be overly pessimistic resulting in false setup and hold violations. This is why PrimeTime must know if the input and output of the cell is rising/falling for each path. Also, since PrimeTime does not use test vectors, each path is analyzed twice, once with a rising input and once with a falling input.

Net Delay: Amount of delay from the output of a gate to the input of the next gate in a timing path. It depends on the following parameters

a. Parasitic Capacitance

b. Resistance of net

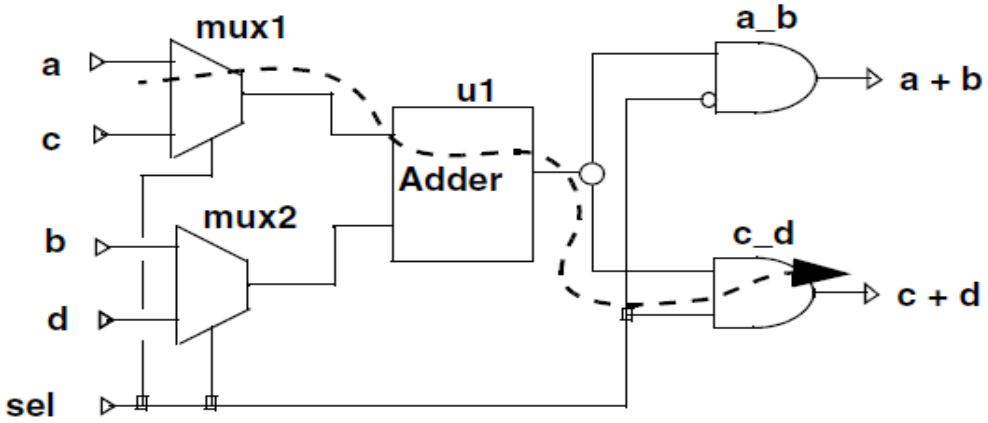
Setting or Declaring false Paths in Primetime:

There are paths in a design were a designer would not want the timing arcs to be calculated . These paths are either not relevant to functional operation of the circuit or paths which are impossible to exercise. Another case where a false path is needed is when data is launched off of a clock and captured on a different asynchronous clock domain.

True and False Path Detection By PrimeTime

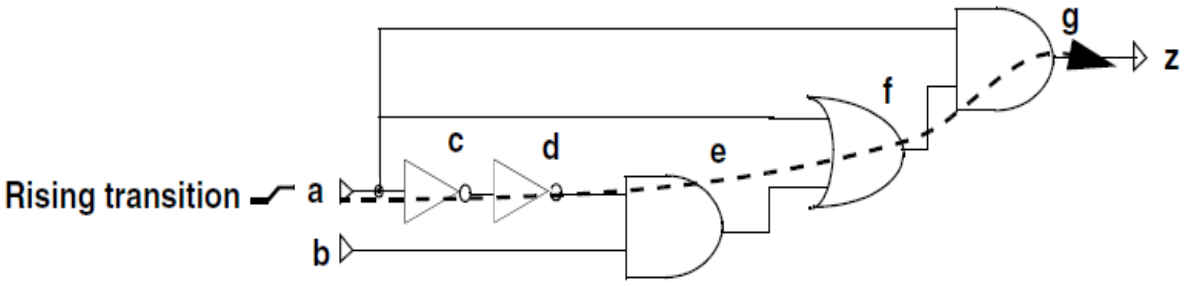
An advanced feature of PrimeTime is the ability to determine whether a specified path is a true path or false path. PrimeTime can also find the most critical true path in the design.

PrimeTime categorizes false paths into two main types: functional and delay-dependent.



6. Functional False Path Due to Resource Sharing

Figure 6 shows an example of a functional false path that results from resource sharing. When mux1 is selected, the path through AND gate c_d is blocked.



7. Delay-Dependent False Path in Carry-Lookahead Logic

Figure 7 shows an example of a delay-dependent false path in carry-lookahead logic. The highlighted path (from a to g) is false for a rising transition at input a. The shorter directpath (from a, through f, to g) determines the longest true path.