ECE 524 - Synthesis and Verifi of Digital Circuits - Spring 2015
Lab 2 - Static Timing Analysis
Due Date: 5-7-2015

1 Objective

The objective of this lab is to **introduce the Static Timing Analysis tool Synopsys PrimeTime and perform static timing analysis with simple constraints**.

2 Exercises

1. Use the **Synopsys Design Compiler** for the file **s27.v with s27.tcl** to produce synthesized file name as **s27_syn.v**. In **s27.tcl**, you need declare your own clock period value with 50 percent duty cycle, all other values in **s27.tcl** are kept same.
2. Read the tutorials **PrimeTime** and **TimingPath** carefully and understand the definitions and concepts explained in the tutorial. **TA will ask questions from these two tutorials during verification**.
3. Use the file **s27_syn.v** and the tutorial **PrimeTime** to perform static timing analysis. **Declare your own value for clock period value (same value as used in s27.tcl), load and tran value and follow the tutorial step by step. Except these three values, all other values and settings are same as mentioned in tutorial**. The objective of this exercise is to obtain **smallest clock period, highest load and highest intran value without any timing violations**.

3 Submission

1. For Exercise 1, final mapped schematic and synthesized verilog code (**s27_syn.v**) and all the reports generated by s27.tcl.
2. For Exercise 3, all the reports generated by Prime.script. **Exercise 3 focus on optimization, points are awarded on relative grading basis**.