Breaking Out of the Die-Box
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Abstract – **Space: the final frontier. These are the voyages of the KT Enterprise. Its five-year mission: to explore strange new devices; to seek out new innovations and new technologies; to boldly go where no competitor has gone before.** This whimsical adaptation of the cult classic is very apropos to the state of the wafer inspection world today. Historically, finding yield killer defects on patterned wafer inspection has been mostly limited to a die-to-neighboring-die comparison paradigm. Our primary focus is rapidly migrating from hardware and image processing solutions to reduce system noise and improve defect signal, to addressing wafer pattern noise, but these efforts alone are falling short. This paper advocates breaking out of the die-to-die box as the next paradigm shift. It identifies major system, hardware and software difficulties that must be overcome to enable this breakout, proposes some architectural approaches, and explores possibilities in this new inspection frontier.

I. Introduction

Imagine combining Google Earth with medical imaging technology to image the outer layer of the earth's crust over time. After an earthquake, reprocessing critical areas may identify signatures enabling prediction capabilities days in advance.

Unlike this difficult example to collect layered image data, we can image semiconductor device layers after each manufacturing step. Access to design data provides the means to construct a multi-dimensional model of what each device actually looks like. This would unlock a whole new realm of possibilities. However, there are many interesting and challenging problems to tackle to make this dream a reality.

To dominate in the future we will have to metaphorically take a page out of Google's book. We need to be able to store the entire history of the wafer stack. [1]

A. Multi-dimensional Inspection Possibilities

NanoPoint is a suite of software and image processing solutions that leverages chip design data to target critical inspection areas with high precision. It has been a game changer in minimizing wafer pattern noise in yield critical areas and thus extending our tool's defect discovery capabilities. However, it is still fundamentally limited to die-to-die comparisons paradigm.

Adding dimensions of focus, spectrums, optical modes and wafer layers, a multi-dimensional view of each semiconductor device is constructed. This coupled with the design model enables possibilities to inspect device to model, device to any other same device on any wafer, and common design structures within the device and even across different devices. [2]

II. Solutions for this new Paradigm

The solution requires a new architecture **BRISSC**; **B**idirectional, **R**emote-able, **I**nfrastructure for **S**harable, **S**torage and **C**ompute. Bidirectional is to save and play back image

data for later re-processing. Remote-able and sharable allows for a centralized system that supports multiple tools and the possibility of moving the system outside the cleanroom to lower costs.

A. Data Storage

This new inspection paradigm will require petabytes of data storage to allow image processing across layers and wafers. A single layer of a 300mm wafer imaged with a 25nm pixel size generates 150 terabytes of data; 7 layers require one petabyte of storage. Table 1 shows a hypothetical analysis of the data storage needed for a FAB with a 60,000 wafers per month capacity.[1] [3]

Wafer Data Analysis Items	
Wafer Starts Per Month	60000
Wafer Lead Time Days	14
Wafer Sampling Percent	8%
Wafers Sampled Per Month	4800
Layers Per Wafer	32
Layers Sampled Per Wafer	5
Layers Sampled Per Month	24000
Layers Sampled in Lead Time	11200
Average Layers Per Hour	2
Hours Per Month	720
Tools Needed	17
Average Data Bandwidth GB/sec	32
Data Storage Needs (PB)	**615**

Table 1: Theoretical FAB Data Storage

This is over 80x the amount of data that Facebook stored per month in 2013 and on par with the total storage they manage. [4] This is a serious amount of data, so compression techniques are necessary to reduce the cost of the system.

B. High Bandwidth

To meet current bandwidth requirements — Broad Band Plasma, BBP, tools generate data at ~40GB/sec — we must solve two issues: getting the data off the tool without sacrificing throughput and onto disk drives.

InfiniBand FDR 4x, or IB, can meet a 5 GB/sec read/write speed.[2] [5] IB links will transfer data from tool to disk storage systems where it is buffered in memory then written to disk. Current disk speed in a RAID6[3] configuration can meet a 5 GB/sec read/write speed.

8 disk storage nodes in parallel will meet the storage bandwidth requirement. Stored data from a previous layer, or even a different wafer, can be sent back to the tool at the same b/w.

Multiple tools and disk storage systems will be connected together so any tool to any storage system can achieve full bandwidth. If tools need to share a storage system which exceeds this bandwidth, the tools will just gracefully degrade, i.e. slow down but not fail.

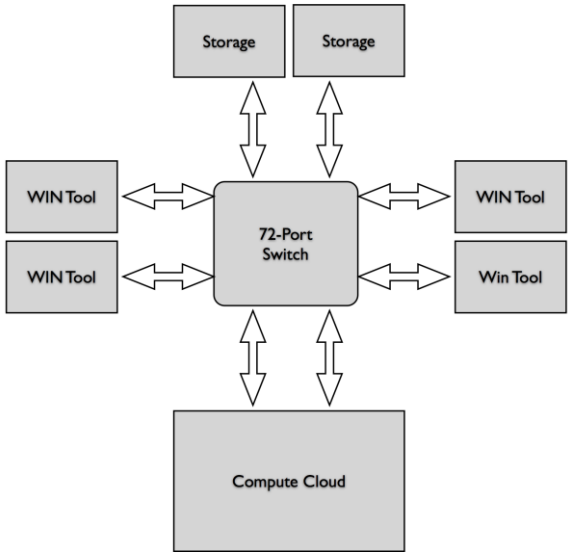

Figure 1: BRISSC Architecture

C. Compression Techniques

Any compression method must be reduced to a streaming problem because random access from disk kills throughput.

One method is only store image patches of interest that exceed a threshold lower than used for defect detection. Storing these in a SQLite database file will enable efficient transfer and later lookup of selected patches to reduce bandwidth needs.

D. Parallel Computing

Obviously a compute cloud will be critical. [6] The WIN tools have a ton of compute resources, but this must be reserved for maintaining WPH

[1] Global Foundries has Fabs with capacity of 50,000 to 80,000 wafers.

[2] IB is a switched fabric topology, FDR 4x configuration data rate is 54.54 Gbit/sec

[3] RAID6 configuration of 36 drives, 3 x 12

throughput for such a costly resource.

Compute resources will be added to the IB network for overflow and offline computing. Compute intensive algorithms that exceed the inspector's compute resources need overflow compute. Applications not on critical path can take advantage of lag time, a scheduling concept, for offline compute. For example, inspector results not needed until the wafer arrives at the eDR tool provides minutes of lag time for offline processing.

A homogenous set of compute resources is desirable for resource allocation, cost, scalability, and maintenance. Not all applications will run on a cluster of inexpensive compute nodes, so a pragmatic compromise is to plan for a small assortment of types, probably two. A main low cost resource[4] and a high end resource[5].

E. Scalability

As it is unlikely that storage and compute requirements will increase proportionally, this architecture supports independent scaling of these two resource types.

For initial deployment in the field a lower cost configuration with less flexible scaling will be a combined storage and compute system.

F. Software Architecture

The software architecture will provide some basic resource management capabilities to build and run applications on. A low level get/put type interface will provide data transfer between tools, the compute, and storage systems on the IB network.

"To provide "burst" compute capacity, we want a generally usable compute cloud much like the Amazon AWS cloud or Microsoft's Azure." [7] The physical machines in the cloud will be accessed as virtual machines" [7] so each application can run in its "native" supported language and OS, i.e. no porting required.

G. Applications, Algorithms and AI

Applications built on this architecture can provide value in 3 areas; higher quality results, faster time to results, and reduced parts cost.

Higher quality results are achieved when new information is known about the device after the wafer is no longer available to inspect but the wafer image data is available. This is analogous to forensic science where DNA samples from the past can be used with current technology to solve old cases. For example, knowing precisely where the chip failed can focus the search for a signature that would indict the process or step that originated this failure and help define a template to identify the killer defect when it reoccurs.

III. Further Work Needed/Challenges

A. New Inspection Methods

Volume inspection in Z is the next frontier to conquer. [1] Inspecting each layer to identify when the first signature of a defect can be detected and correlated to final test failure will enable customers to fix process systematic issues faster.

Fusing data and capabilities between KT tools will enable faster defect discovery. eDR provides high resolution but at very low throughput and BBP provides high throughput at much lower resolution. eDR images provide resolution to optimize BBP recipes and algorithm parameters, and BBP results direct eDR to sample critical areas, significantly improving throughput.

Inspections can compare any area within a die to any other area(s) within the same die, other die or even other wafers that were or will be scanned in the future. Space and time no longer constrain the inspection methods employed.

B. Visualization

Something conceptually similar to Google maps will provide ease of use in viewing image data for a particular location and compare this across layers, wafers, and devices. Fast access to this data and a rich suite of image processing tools will enable data visualization as an effective strategy in recipe tuning and algorithm learning.

C. Rapid Algorithm Prototyping

This architecture should support future rapid algorithm prototyping without code recompilation. Algorithms will be implemented

[4] likely configuration: 2 sockets x 12 cores with 256GB+ memory

[5] likely configuration: 4 sockets x 15 cores with 384GB+ memory

like plug and play blocks that can be linked together to rapidly evaluate new methods.

D. Common Mode Errors

Current inspection methods often disregard common mode errors because they are mostly eliminated when comparing die to die within a single scan across the wafer. Some examples of these errors are optical field dependent aberrations: distortion, uniformity, field tilt, polarization effects, and illumination angle, sensor pixel response, stage thermal drift, and air wiggle.

Aliasing for under sampled pixels sizes which rely on common mode image shift, and improved interpolation scheme to handle 0.5 pixel shift with minimal interpolation error for non-aliased pixel will also need consideration. [8]

E. Position, Position, Position

Current generation tools cannot position accurately enough during image data collection, so image alignment methods are employed for common mode inspections. These alignment solutions are still done too coarsely — at best on 512x512 pixel regions — to align to within a few pixels.

Future inspection modes will require much finer resolution and accuracy, sub-pixel alignment of each pixel. Near neighborhood die-to-die alignment will be replaced with global alignment within die and across layers, wafers, devices, and tools.

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