

## DM5490/DM7490A, DM7493A Decade and Binary Counters

### General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 90A and divide-by-eight for the 93A.

All of these counters have a gated zero reset and the 90A also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade or four-bit binary), the B input is connected to the  $Q_A$  output. The input count pulses are applied to input A and the outputs are as

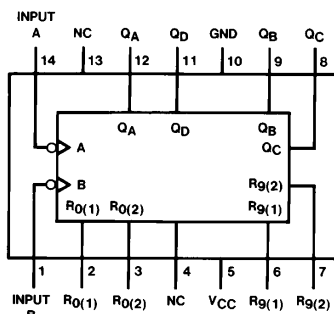
described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 90A counters by connecting the  $Q_D$  output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output  $Q_A$ .

### Features

- Typical power dissipation
  - 90A 145 mW
  - 93A 130 mW
- Count frequency 42 MHz

### Connection Diagrams

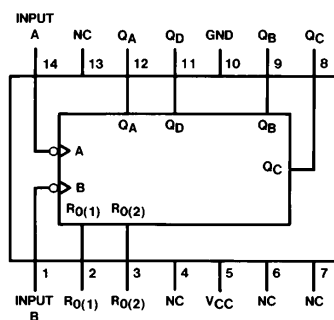
Dual-In-Line Package



TL/F/6533-1

Order Number DM5490J, DM5490W or DM7490AN  
See NS Package Number J14A, N14A or W14B

Dual-In-Line Package



TL/F/6533-2

Order Number DM7493AN  
See NS Package Number N14A

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter		DM5490			DM7490A			Units
			Min	Nom	Max	Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage		2			2			V
V <sub>IL</sub>	Low Level Input Voltage				0.8			0.8	V
I <sub>OH</sub>	High Level Output Current				−0.8			−0.8	mA
I <sub>OL</sub>	Low Level Output Current				16			16	mA
f <sub>CLK</sub>	Clock Frequency (Note 5)	A	0		32	0		32	MHz
		B	0		16	0		16	
t <sub>W</sub>	Pulse Width (Note 5)	A	15			15			ns
		B	30			30			
		Reset	15			15			
t <sub>REL</sub>	Reset Release Time (Note 5)		25			25			ns
T <sub>A</sub>	Free Air Operating Temperature		−55		125	0		70	°C

## '90A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = −12 mA			−1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	2.4	3.4		V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IH</sub> = Min, V <sub>IL</sub> = Max (Note 4)		0.2	0.4	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V			1	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max V <sub>I</sub> = 2.7V	A		80	μA
			Reset		40	
			B		120	
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max V <sub>I</sub> = 0.4V	A		−3.2	mA
			Reset		−1.6	
			B		−4.8	
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 2)	DM54	−20	−57	mA
			DM74	−18	−57	
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max (Note 3)		29	42	mA

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I<sub>CC</sub> is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

Note 4: Q<sub>A</sub> outputs are tested at I<sub>OL</sub> = Max plus the limit value of I<sub>IL</sub> for the B input. This permits driving the B input while maintaining full fan-out capability.

Note 5: T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

## '90A Switching Characteristics

at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$  (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$ $C_L = 15 pF$		Units
			Min	Max	
$f_{MAX}$	Maximum Clock Frequency	A to $Q_A$	32		MHz
		B to $Q_B$	16		
$t_{PLH}$	Propagation Delay Time Low to High Level Output	A to $Q_A$		16	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	A to $Q_A$		18	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	A to $Q_D$		48	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	A to $Q_D$		50	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	B to $Q_B$		16	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	B to $Q_B$		21	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	B to $Q_C$		32	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	B to $Q_C$		35	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	B to $Q_D$		32	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	B to $Q_D$		35	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	SET-9 to $Q_A, Q_D$		30	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	SET-9 to $Q_B, Q_C$		40	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	SET-0 Any Q		40	ns

## Recommended Operating Conditions

Symbol	Parameter		DM7493A			Units
			Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage		4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage		2			V
V <sub>IL</sub>	Low Level Input Voltage				0.8	V
I <sub>OH</sub>	High Level Output Current				−0.8	mA
I <sub>OL</sub>	Low Level Output Current				16	mA
f <sub>CLK</sub>	Clock Frequency (Note 5)	A	0		32	MHz
		B	0		16	
t <sub>w</sub>	Pulse Width (Note 5)	A	15			ns
		B	30			
		Reset	15			
t <sub>REL</sub>	Reset Release Time (Note 5)		25			ns
T <sub>A</sub>	Free Air Operating Temperature		0		70	°C

## '93A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = −12 mA			−1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	2.4	3.4		V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IH</sub> = Min, V <sub>IL</sub> = Max (Note 4)		0.2	0.4	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V			1	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max V <sub>I</sub> = 2.4V	Reset		40	μA
			A		80	
			B		80	
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max V <sub>I</sub> = 0.4V	Reset		−1.6	mA
			A		−3.2	
			B		−3.2	
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 2)		−18	−57	mA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max (Note 3)		26	39	mA

**Note 1:** All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

**Note 2:** Not more than one output should be shorted at a time.

**Note 3:** I<sub>CC</sub> is measured with all outputs open, both R0 inputs grounded following momentary connection to 4.5V and all other inputs grounded.

**Note 4:** Q<sub>A</sub> outputs are tested at I<sub>OL</sub> = Max plus the limit value of I<sub>IL</sub> for the B input. This permits driving the B input while maintaining full fan-out capability.

**Note 5:** T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

## '93A Switching Characteristics

at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$  (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$ $C_L = 15 pF$		Units
			Min	Max	
$f_{MAX}$	Maximum Clock Frequency	A to $Q_A$	32		MHz
		B to $Q_B$	16		
$t_{PLH}$	Propagation Delay Time Low to High Level Output	A to $Q_A$		16	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	A to $Q_A$		18	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	A to $Q_D$		70	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	A to $Q_D$		70	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	B to $Q_B$		16	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	B to $Q_B$		21	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	B to $Q_C$		32	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	B to $Q_C$		35	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	B to $Q_D$		51	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	B to $Q_D$		51	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40	ns

## Function Tables (Note D)

**90A**  
BCD Count Sequence  
(See Note A)

Count	Outputs			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

**90A**  
BCD Bi-Quinary (5-2)  
(See Note B)

Count	Outputs			
	Q <sub>A</sub>	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

**93A**  
Count Sequence  
(See Note C)

Count	Outputs			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

**90A**  
Reset/Count Function Table

Reset Inputs				Outputs			
R0(1)	R0(2)	R9(1)	R9(2)	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L		COUNT		
L	X	L	X		COUNT		
L	X	X	L		COUNT		
X	L	L	X		COUNT		

**93A**  
Reset/Count Function Table

Reset Inputs		Outputs			
R0(1)	R0(2)	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
H	H	L	L	L	L
L	X		COUNT		
X	L		COUNT		

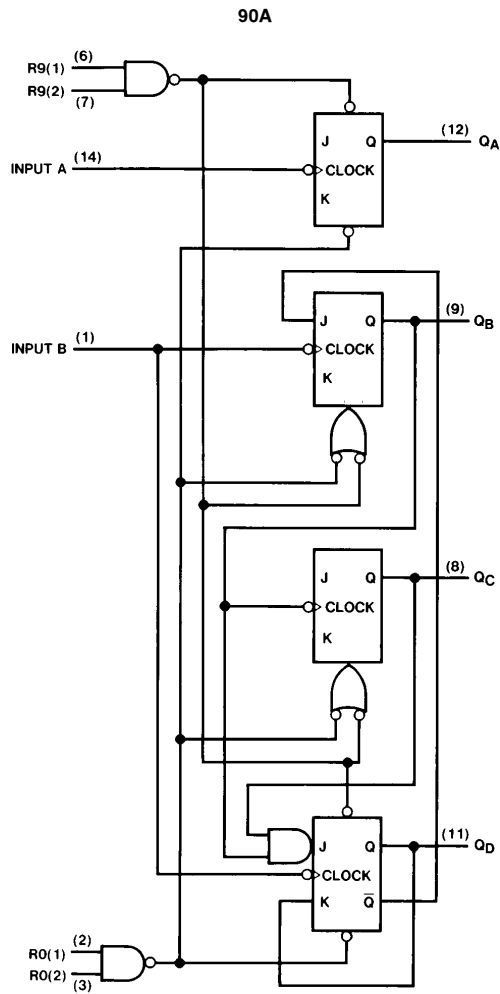
**Note A:** Output Q<sub>A</sub> is connected to input B for BCD count.

**Note B:** Output Q<sub>D</sub> is connected to input A for bi-quinary count.

**Note C:** Output Q<sub>A</sub> is connected to input B.

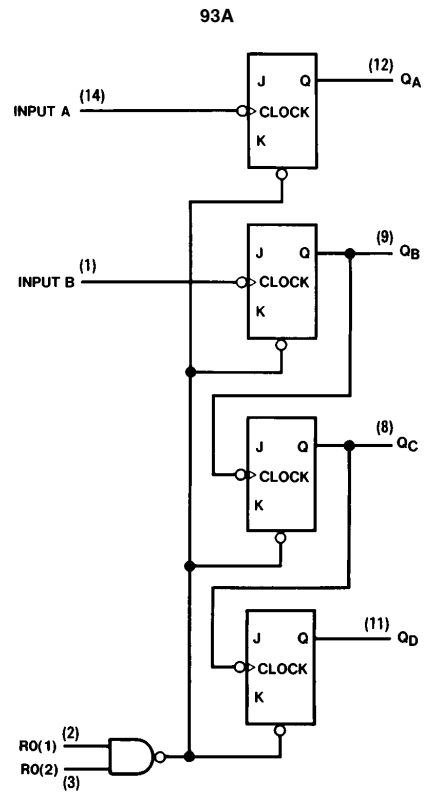
**Note D:** H = High Level, L = Low Level, X = Don't Care.

## Logic Diagrams

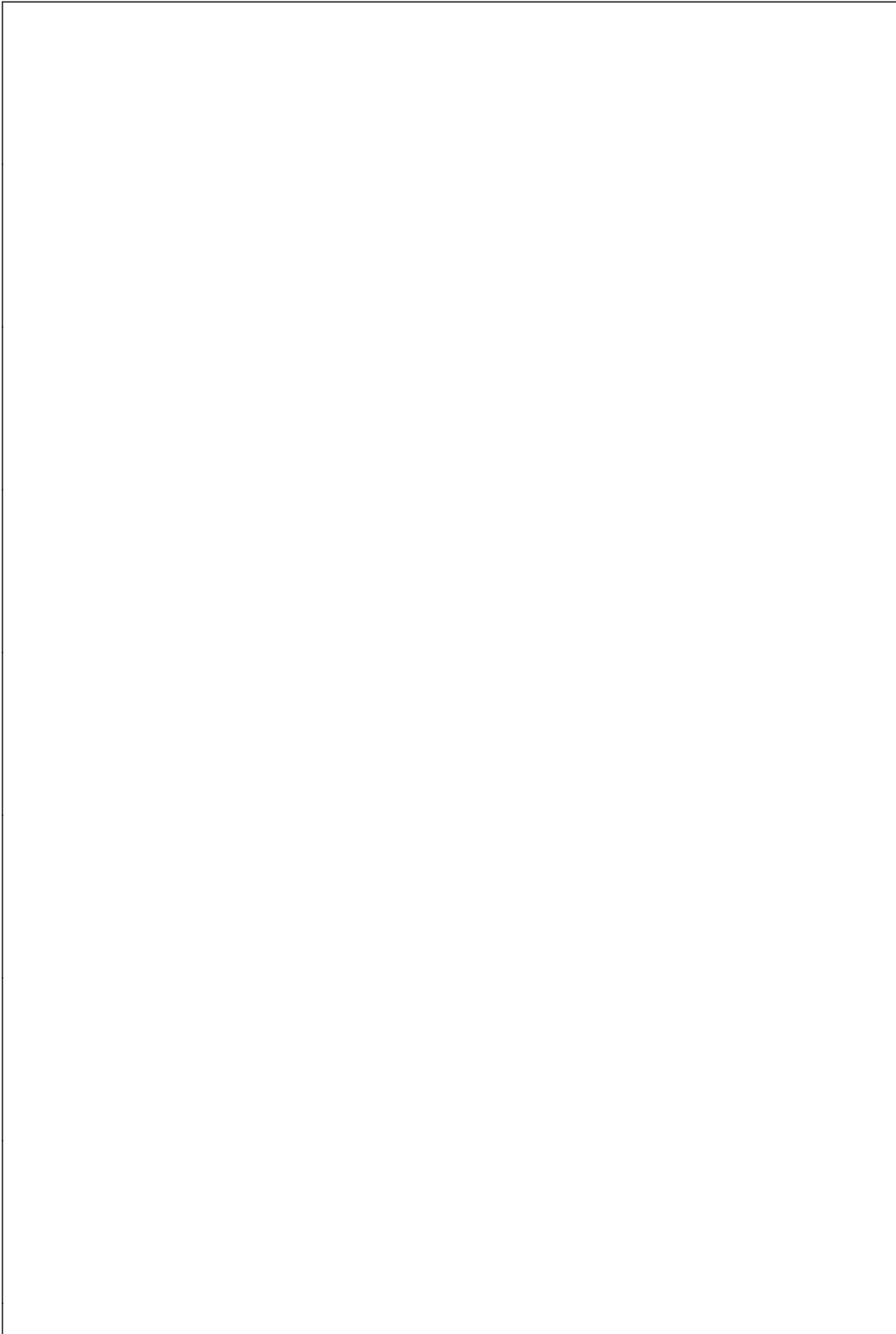


TL/F/6533-3

The J and K inputs shown without connection are for reference only and are functionally at a high level.

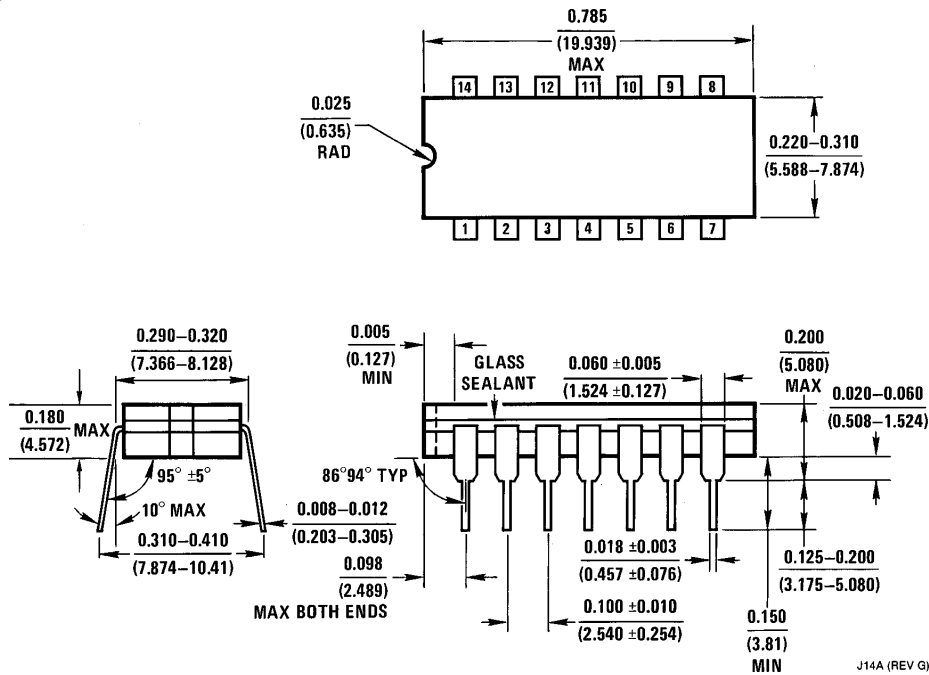


TL/F/6533-4

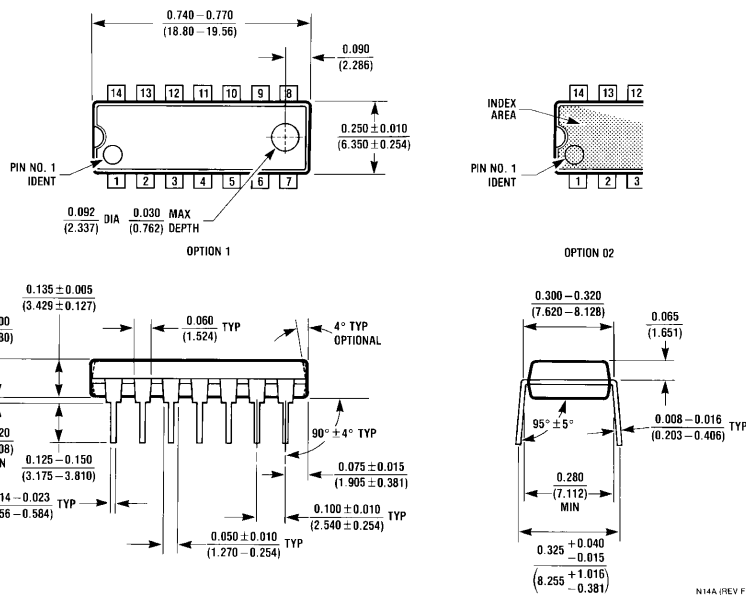




# Physical Dimensions inches (millimeters)



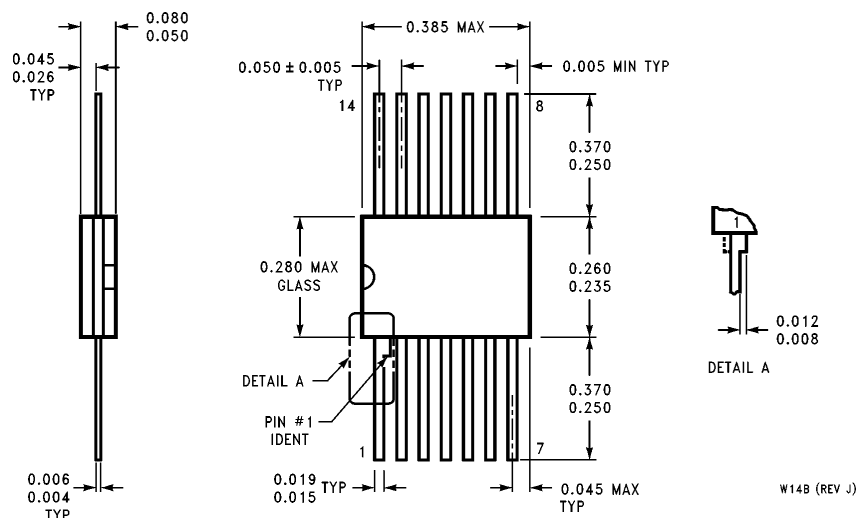
**14-Lead Ceramic Dual-In-Line Package (J)**  
Order Number DM5490J  
NS Package Number J14A



**14-Lead Molded Dual-In-Line Package (N)**  
Order Number DM7490AN or DM7493AN  
NS Package Number N14A

# DM5490/DM7490A, DM7493A Decade and Binary Counters

## Physical Dimensions inches (millimeters) (Continued)



**14-Lead Ceramic Flat Package (W)**  
**Order Number DM5490W**  
**NS Package Number W14B**

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**National Semiconductor Corporation**  
1111 West Bardin Road  
Arlington, TX 76017  
Tel: 1(800) 272-9959  
Fax: 1(800) 737-7018

**National Semiconductor Europe**  
Fax: (+49) 0-180-530 85 86  
Email: [cnjwge@tevm2.nsc.com](mailto:cnjwge@tevm2.nsc.com)  
Deutsch Tel: (+49) 0-180-530 85 85  
English Tel: (+49) 0-180-532 78 32  
Français Tel: (+49) 0-180-532 93 58  
Italiano Tel: (+49) 0-180-534 16 80

**National Semiconductor Hong Kong Ltd.**  
13th Floor, Straight Block,  
Ocean Centre, 5 Canton Rd.  
Tsimshatsui, Kowloon  
Hong Kong  
Tel: (852) 2737-1600  
Fax: (852) 2736-9960

**National Semiconductor Japan Ltd.**  
Tel: 81-043-299-2309  
Fax: 81-043-299-2408

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