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| EXPERIMENT: Conditional Subtractor |

References

1. *Digital Design Using Digilent FPGA Boards ─ VHDL Edition* 
   1. *Quad 2-to-1 Multiplexer*
   2. *N-bit Comparator*
   3. *N-bit Subtractor*
2. Nexys-4 Reference Manual: *nexys4\_rm.pdf* (available on Moodle)

**LAB**

**Part 1**

1. In this lab, we want to create a circuit that performs the design specification shown in pseudo-code below:

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| **int submax(x, y)**  **if (x < y)**  **z = y - x;**  **else**  **z = x - y;**  **end if**  **return z;** |

There are several ways in which we could design this circuit. According to the pseudo-code, the component that we need to make must subtract *y* from *x* whenever *x* is less than *y*, otherwise it must subtract *x* from *y*. The output will always be positive since we are subtracting the smaller number (either *x* or *y*) from the larger number in either case. We are going to design the circuit using a multiplexer to select between the two operations, a comparator to compare *x* with *y* that will control the multiplexer to select the correct operation, and two subtractors to perform the operations. The components necessary are shown in Figure 1. We will use a 4-bit bus, that is, both *x* and *y* will be 4-bits.

**Note:** if you have a Nexys-4 board feel free to use an 8-bit bus instead, since it has enough switches that we can input two 8-bit numbers at once.

Design the circuit by connecting the components in Figure 1 so that the component *SubMax* behaves as described in the design description given by the pseudo-code above. Be sure to label all signals and include the bus size indicators on all lines where appropriate.

1. Create a VHDL file called *submax.vhd* and implement your design by port mapping the multiplexer (Listing 5.9), N-bit comparator (Listing 5.32), and two N-bit subtractors (Listing 6.6) from your book according to your design. Modify the N-bit comparator by removing the *gt* and *eq* outputs since we do not need them.
2. Create a testbench called *submax\_tb.vhd.* Use it to simulate *SubMax* showing that it works correctly when *x* < *y* and when *y* ≤ *x*. Use at least one set of inputs for each of these two cases.



Figure 1: *SubMax*

**Deliverables:** submax.vhd, submax\_tb.vhd, modified N-bit comparator, functional simulation of submax.vhd

**Part 2**

1. Another way that we could implement the design specification from Part 1 would be to use VHDL behavioral statements that describes the behavior of the circuit and let the Xilinx synthesis tools design the digital logic. Write a VHDL program called *submax2.vhd* using only behavioral statements in VHDL that will implement the design specification from Part 1. Hint: Your entity will be the same as in Part 1 and the architecture will be very similar to the pseudo-code. Don't forget to place your behavioral statements inside of a process with a sensitivity list.
2. Create a testbench called *submax2\_tb.vhd* and simulate *SubMax2* showing that it works correctly when *x* < *y* and when *y* ≤ *x*. Use at least one set of inputs for each of these two cases.

**Deliverables:** submax2.vhd, submax2\_tb.vhd, functional simulation of submax2.vhd

**Part 3**

1. In order to test our digital circuit on the Nexys board, create a top-level for our design to make use of the inputs and outputs (I/O) on the board. Use the switches to control the inputs *x* and *y*. This will work well since both *x* and *y* are 4-bit buses and we have at least 8 switches on the board. For the output, *z*, use 4 LEDs. Create this top-level, shown in Figure 2, and port map either *SubMax* or *SubMax2* into the top level. You can choose which one since they are functionally the same.



Figure 2

1. Demonstrate the operation of your synthesized program on the Nexys board to your lab instructor.
2. Answer the following questions. Use as inputs *x*=15 and *y*=9.
   1. What answer do you get?
   2. Change the greater of the two inputs with the answer from question a. What is the output of the circuit? So x = (answer from part a), y=9.
   3. Continue replacing the greater of the two inputs with the output until the two inputs are the same and therefore the output is zero. What is the value of the two inputs when they are the same?
   4. Is there a relationship between this output and the original inputs of 15 and 9? Hint: Think of dividing the original *x* and *y* by the final answer. What is the relationship?

You can use this circuit to iteratively compute the \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ of two numbers.

**Deliverables:** VHDL files *submax2\_tb.vhd, submax2.vhd,* and *submax\_top.vhd* and the answers to section 3 as a Word file (you can submit just the questions/answer section.)