**Lab 2: A Special Purpose Processor (SPP) for Computing Euclid’s GCD**

**Part 1 Deliverables:**

1. Design Schematic

Diagram, schematic

Description automatically generated

Figure : Euclid's GCD Schematic

1. See attached source files:
   1. RegAndMuxControl.vhd
   2. EuclidsGCD.vhd
   3. EuclidsGCD\_tb.vhd
2. Functional Simulation of EuclidsGCD.vhd:

Graphical user interface

Description automatically generated

Figure : Functional Simulation of EuclidGCD.vhd with x = 15 (0x0F) and y = 6 (0x06)

A screenshot of a computer

Description automatically generated with medium confidence

Figure : Functional Simulation of EuclidGCD.vhd with x = 4 (0x04) and y = 14 (0x0E)

Both simulations show the correct answer is obtained and persists provided input variables remain constant despite continuing clock cycles. The simulations require asserting the clear bit for a brief period to put the registers into a known state, hence the “00” value for GCD at the beginning of the simulation.

**Part 2 Deliverables:**

1. See attached source file:
   1. EuclidsGCD\_top.vhd

**Part 3 Deliverables:**

1. See attached source file:
   1. EuclidsGCD\_top2.vhd