**Fall 2022**

To: SECS Faculty and ECE/CSI 4710 & ECE/CSI 5710/008 students

From: Darrin M. Hanna, Ph.D., CFII, Professor of Engineering

Subject: ECE 4710/5710 – Digital Logic and Microprocessor Design

CSI 3710/5008 – Computer Hardware Design in 202B ODH

##### Prerequisites

###### ECE 2700 (ECE 278) and either major standing or instructor approval

**Text and Materials (Required)**

*Digital Design Using Digilent FPGA Boards - VHDL/Vivado Edition*, by Richard E. Haskell and Darrin M. Hanna, LBE Books, 2018.

*Advanced VHDL Graphics Using Digilent FPGA Boards*, by Richard E. Haskell and Darrin M. Hanna, LBE Books, 2014.

**Digital Logic Design Board with FPGA:** Nexys-A7 FPGA trainer board available to purchase from [www.digilentinc.com](http://www.digilentinc.com); each student must purchase a board.

**Class and Lab Time**

Classes will be held on Tuesday and Thursday from 5:30 to 7:17 p.m. in room 202B of O’Dowd Hall. The labs will be held in Room 562 of the Engineering Center. Labs will start on Monday, September 12, 2022.

**Course Objectives**

By the end of this course a successful student will be able to (ABET 1-7 mapping shown in parentheses):

* Design combinational and sequential components using VHDL (1)
* Describe how combinational and sequential components can be used to design a datapath and control unit for performing logic operations (1)
* Design custom architectures to interact with external peripherals (1)
* Design dedicated special-purpose processors using VHDL and synthesize them to an FPGA (1)
* Build a testbench for a digital system (1, 6)
* Perform a functional and timing simulation of a digital circuit described in VHDL (1, 6)
* Work in a team environment to design a digital system and communicate the results in a written report and an oral presentation (2, 5, 7)

**Laboratory**

This class has an important, hands-on laboratory component. Students must complete each lab assignment individually unless otherwise specified in the lab instructions. We will use Xilinx design tools and simulator, and the Digilent Nexys-A7 prototyping board to design, implement, simulate, and test our hardware. The Xilinx design tools and simulator can be downloaded for free online. Lab assistants will be available during the lab times and outside of class, by appointment, to help with the labs. Students must turn in lab assignments, demonstrate the hardware that they implemented to a lab assistant, and successfully answer the questions asked by the lab assistant to receive credit.

**List of Topics**

* Digital Logic Circuits
* Combinational Logic Circuits
* Timing
* Implementation Technologies
* Latches and Flip-Flops
* Sequential Logic Circuits
* Standard Sequential Components and RAM
* Datapaths
* Control Units
* Dedicated Microprocessors
* Interfacing with Peripherals
* Test Benches
* Digital Debugging

In addition to the lectures, the class will include a hands-on laboratory in which students will design digital circuits using VHDL and synthesize them to Xilinx FPGAs. Each of the labs will involve a digital design using VHDL.

**Design Project**

In addition to the assigned labs each student will participate in a group project and demonstrate an original VHDL design by means of a PowerPoint presentation given to the class, a video, and a project report.

**Exams**

There will be two exams during the semester.

**Grading**

Grading will be based on the following:

Labs/HW 20 %

Exam 1 25 %

Exam 2 25 %

Design Project

Tuesday, December 13th 7p – 11p

30 %

100 %

A student who does not earn a passing grade (60% or more) in the laboratory and on the Design Project will receive a 0.0 (F) in the course.

**Academic Conduct** Students are expected to conduct themselves according to the student handbook. Any student found responsible for cheating by the Academic Conduct Committee will receive a 0.0 (F) in this course.

**Office Hours**

**Darrin M. Hanna, Ph.D., CFII**

By appointment, email me

Email: [dmhanna@oakland.edu](mailto:dmhanna@oakland.edu)

Office: 436 Engineering Center (EC)

248.370.2170

Web page: <http://www.cse.secs.oakland.edu/hanna>