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**School of Electrical and Computer Engineering**

**Embedded Systems Design - ECE 5721 - Fall 2022**

**Homework 1**

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**September 22, 2022**

1. Design at the block diagram level an Electric Wheelchair or Scooter. Show the inputs, outputs, microcontroller, motor, controls, etc.

Diagram

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Figure : Block diagram of an electric scooter

1. Under what conditions is Register 13 switched between holding the Main Stack Pointer (MAP) and the Process Stack Pointer (PSP)?

“Simple applications typically use the only MSP, although a kernel or operating system may use both” ( [1], 85). When the CPU is in handler mode, the stack pointer refers to the MSP. However, when the CPU is in Thread mode, the SP can refer to either the MSP or the PSP. A special CPU register named “CONTROL” has a flag field called “SPSEL” that selects which stack pointer to use. In systems with a kernel or operating system, threads will use the PSP and the OS, and exception handlers will use the MSP. ( [1], 99).

1. What is the content of register 14 after a Peripheral Interrupt Occurs?

“Register 14 is called the Link Register, and it holds the return address when a Branch and Link instruction is used” ( [1], 85). This means the when the processor receives an interrupt it needs to service, the processor stores the address of the currently executing process in the link register so that it can return there after the interrupt is handled.

1. What are the valid input voltage ranges for Logic 1 and 0 for a KL25Z128VLK4 – 80 with VDD = 3V?

The voltage levels for logic 1 and logic 0 on a KL25Z128VLK4-80 with a VDD equal to 3V are 2.1-3.0V and 0-1.0V, respectively ( [1], 27).

1. Refer to the Cortex M0+ based KL25Z128VLK4 – 80 LQFP details: How many GPIO pins are there for:
   1. Port A

15 (14 + 1 alternate (pin 42, default = RESET\_b, ALT1 = PTA20)

* 1. Port B

12

* 1. Port C

16

* 1. Port D

8

* 1. Port E

15

1. Which Digital Outputs (Ports & Pins) on KL25Z support high drive capability?

Port B, pins 0 and 1

Port D, pints 6 and 7

1. Calculate the resistor values to limit the current through the Blue and Red LEDs of Figure 2.3 to 18mA each. Assume VDD = 3V.

Assuming a VDD of 3.0V, a forward voltage 1.8V for the red LED and a forward voltage of 2.7V for the blue LED, and a desired current of 18mA for each LED, the resistances, *R\_red* and *R\_blue,* are calculated to be:

1. Convert the Program Listing 2.4 of Chapter 2 – Dean to use Fast GPIO access rather than regular GPIO.
2. while(1) {
3. if (FPTA->PDIR & MASK(SW1\_SHIFT)) {
4. // switch is not pressed, so light only LED 2
5. FGPIO\_PSOR\_REG(FPTA) = MASK(LED2\_SHIFT)
6. FGPIO\_PCOR\_REG(FPTA) = MASK(LED1\_SHIFT)
7. } else {
8. // switch is pressed, so light only LED 1
9. FGPIO\_PSOR\_REG(FPTA) = MASK(LED1\_SHIFT)
10. FGPIO\_PCOR\_REG(FPTA) = MASK(LED2\_SHIFT)
11. }
12. }
13. What is the purpose of the following register?
    1. EPSR

The Execution Program Status “Register”, or EPSR, is a single bit field within the more generic Program Status Register (PSR). This bit field contains the Thumb status bit, which indicates the current state of the processor with regards to which instruction set it is currently executing. That is, if EPSR is set to 1, the processor is in Thumb mode, which means it is executing a set of 16-bit instructions which are a subset of the larger 32-bit ARM instruction set architecture.

* 1. MSP

The Main Stack Pointer, or MSP, contains the address of the top of the stack in memory. That is, the address where new entries to memory will be added, or the address from which memory will be retrieved.

1. Describe the response of the KL25Z Nested Vector Interrupt Controller when it experiences the late arrival of a second interrupt (I2) after the initial interrupt (I1) has caused the processor to begin a context switch to service the interrupt. Interrupt I2 has the same priority as I1. Provide an example of the sequence of steps that a processor may experience when this occurs:

When the late arrival of a second interrupt (I2) occurs during the context switched caused by a previous interrupt (I1) that has the same priority as I2, the processor will continue its context switch, proceed with servicing I1 while I2 is held in a **pending** **state**. After servicing I1, the previous priority level is restored, and the new exception (I2) is handled if priority level allows. This is (roughly) illustrated in Figure 2.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Int. 1 | | Int. 2 | Int 2 (Pending) | | Interrupt 2 Handler | | |  |  |
|  |  |  |  |  |
|  |  | Interrupt 1 Handler | | |  | | |  |  |
|  |  |  |  |  |  |  |
| Main Process | |  |  |  |  |  |  | Main Process | |
|  |  |  |  |  |  |

Figure :Program control flow following second interrupt with same priority as first occurring during context switch caused by first interrupt

# **References**

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| --- | --- |
| [1] | A. Dean, Embedded Systems Fundamentals with Arm Cortex-M based Microcontrollers, Cambridge: Arm Education Media, 2017. |