

**School of Electrical and Computer Engineering**

**Embedded System Design - ECE 5721 - Fall 2022**

**Final Project Proposal**

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# Introduction

Fatigued driving is a serious problem that results in thousands of crashes, injuries, and deaths every year. These crashes impose monumental physical, emotional, and financial hardships for the individuals affected by the crash, as well as economic and logistical complications for trucking companies, insurance firms, and state and local governments.

Research has shown the Electroencephalography (EEG) is one of the most reliable tools for detecting sleep onset while driving [1]. It is possible that a device that detects the onset of driver fatigue and implements some form of corrective action could help mitigate the risk of driver drowsiness and thereby reduce the likeliness of crashes.

For this project, we propose to design and prototype an EEG data acquisition and feature extraction device to detect drowsiness in drivers. The project will consist of three main parts: a surrogate “brain” to produce test signals to feed into the system, an analog filter stage for initial signal conditioning, and a digital filter, feature detection, and output stage. The relationship between these three blocks is depicted graphically in Figure 1.

Diagram

Description automatically generated

Figure : Block diagram of drowsiness detection unit

The left-most block, representing the surrogate brain, will consist of a FRDM-KL25Z development board whose sole purpose will be to produce simulation waveforms to be collected for analysis by the fatigue detection system. The surrogate brain will produce a series of complex waveforms comprised of pure sine waves of varying frequencies and amplitudes mixed with random, high-frequency noise to simulate real EEG. These signals will be generated by the device’s onboard digital-to-analog converter peripheral.

The middle stage consists of some simple analog signal conditioning. This includes input buffers, amplifiers, and analog filters. Normal human EEG activity typically falls within a frequency range of 1-30Hz, so a bandpass filter will be developed and implemented to attenuate high frequency noise before passing the signals to the digital filter stage.

The final block depicted in Figure 1 is the Digital Filter/Feature Detection/Output stage. This block will also consist of a FRDM-KL25Z development board. We will utilize the four differential channels of the device’s analog-to-digital converter (ADC) to digitize the signals as they exit the analog filter stage. We will then implement some software filters to further reduce high frequency noise before performing a Fourier transform on the input signals.

The results of the Fourier transform will be analyzed to detect frequency shifts in the input signals’ power distributions. We will assert that a shift from >12 Hz (alpha and beta waves) to <8Hz (delta and theta waves) will indicate impending drowsiness. Upon detection of such a state will drive a loud noise through a speaker and blink lights in an attempt to rouse the driver.

Some stretch goals for this project would be to implement wireless communication to broadcast the alertness of a driver to a central dispatch location. GPS could also be included to relay this information in tandem to the dispatcher for use in the event of an accident.

# References

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