Logic Report

T2_3

Abd-Allah Ahmad Aref Al-Dessoukey	1210252
Danah Rafik Reyad Aly Hassan	1210221
Hamza Ayman MohyEldeen Elghonemy	1210218
Youssef Ayman MohamedReda	1210334

Work Distribution

IDs	Name	Part done
1210252	Abd-Allah Ahmad Aref Al-Dessoukey	Addition and Subtraction
1210221	Danah Rafik Reyad Aly Hassan	Remainder
1210218	Hamza Ayman MohyEldeen Elghonemy	Binary to BCD and BCD to seven segments
1210334	Youssef Ayman MohamedReda	Multiplication

All the following tests for each part (every operation) have been made on the main ALU circuit, for all cases where the Output is equal to 0000000, the Zero Flag turns on successfully, and for all cases where the Output is signed -ve, the Sign Flag turns on successfully. Whenever The Div by Zero Flag turns on is indicated in the remainder table.

Table 1: Addition

First Operand	Second Operand	SW Actual Output	Expected Output	Status
0000	**0000**	0000000	0000000	Succeeded
1000	**0000**	0000000	0000000	Succeeded
0000	**1000**	0000000	0000000	Succeeded
1000	**1000**	0000000	0000000	Succeeded
0000	**0110**	0000110	0000110	Succeeded
0000	**1110**	1000110	1000110	Succeeded
0111	**0000**	0000111	0000111	Succeeded
1101	**0000**	1000101	1000101	Succeeded
0110	**0101**	0001011	0001011	Succeeded
0111	**0111**	0001110	0001110	Succeeded
0010	**0111**	0001001	0001001	Succeeded
1100	**0010**	1000010	1000010	Succeeded
1110	**0110**	0000000	0000000	Succeeded
1010	**0101**	0000011	0000011	Succeeded
0110	**1010**	0000100	0000100	Succeeded
0111	**1111**	0000000	0000000	Succeeded
0101	**1111**	1000010	1000010	Succeeded
1011	**1010**	1000101	1000101	Succeeded
1100	**1100**	1001000	1001000	Succeeded
1100	**1111**	1001011	1001011	Succeeded

Table 2: Subtraction

First Operand	Second Operand	SW Actual Output	Expected Output	Status
0000	**0000**	0000000	0000000	Succeeded
1000	**0000**	0000000	0000000	Succeeded
0000	**1000**	0000000	0000000	Succeeded
1000	**1000**	0000000	0000000	Succeeded
0000	**0110**	1000110	1000110	Succeeded
0000	**1110**	0000110	0000110	Succeeded
0111	**0000**	0000111	0000111	Succeeded
1101	**0000**	1000101	1000101	Succeeded
0110	**0101**	0000001	0000001	Succeeded
0111	**0111**	0000000	0000000	Succeeded
0010	**0111**	1000101	1000101	Succeeded
1100	**0010**	1000110	1000110	Succeeded
1110	**0110**	1001100	1001100	Succeeded
1010	**0101**	1000111	1000111	Succeeded
0110	**1010**	0001000	0001000	Succeeded
0111	**1111**	0001110	0001110	Succeeded
0101	**1111**	0001100	0001100	Succeeded
1011	**1010**	1000001	1000001	Succeeded
1100	**1100**	0000000	0000000	Succeeded
1100	**1111**	0000011	0000011	Succeeded

Table 3: Multiplication

First Operand	Second Operand	SW Actual Output	Expected Output	Status
0000	**0000**	0000000	0000000	Succeeded
1000	**0000**	0000000	0000000	Succeeded
0000	**1000**	0000000	0000000	Succeeded
1000	**1000**	0000000	0000000	Succeeded
0000	**0110**	0000000	0000000	Succeeded
0000	**1110**	0000000	0000000	Succeeded
0111	**0000**	0000000	0000000	Succeeded
1101	**0000**	0000000	0000000	Succeeded
0011	**0110**	0010010	0010010	Succeeded
0100	**0111**	0011100	0011100	Succeeded
1100	**0111**	1011100	1011100	Succeeded
1001	**0101**	1000101	1000101	Succeeded
0110	**1001**	1000110	1000110	Succeeded
0101	**1111**	1100011	1100011	Succeeded
1010	**1100**	0001000	0001000	Succeeded
1110	**1011**	0010010	0010010	Succeeded

Table 4: Remainder

First Operand	Second Operand	SW Actual Output	Expected Output	Status
0000	**0000**	0000000 Div by Zero flag	0000000 Div by Zero flag	Succeeded
1000	**0000**	0000000 Div by Zero flag	0000000 Div by Zero flag	Succeeded
0000	**1000**	0000000 Div by Zero flag	0000000 Div by Zero flag	Succeeded
1000	**1000**	0000000 Div by Zero flag	0000000 Div by Zero flag	Succeeded
0110	**0000**	0000000 Div by Zero flag	0000000 Div by Zero flag	Succeeded
1110	**0000**	0000000 Div by Zero flag	0000000 Div by Zero flag	Succeeded
0000	**0110**	0000000	0000000	Succeeded
0000	**1110**	0000000	0000000	Succeeded
0101	**0010**	0000001	0000001	Succeeded
0110	**0011**	0000000	0000000	Succeeded
0101	**1010**	0000001	0000001	Succeeded
0110	**1011**	0000000	0000000	Succeeded
1110	**0100**	1000010	1000010	Succeeded
1110	**0010**	0000000	0000000	Succeeded
1111	**1010**	1000001	1000001	Succeeded
1110	**1011**	0000000	0000000	Succeeded