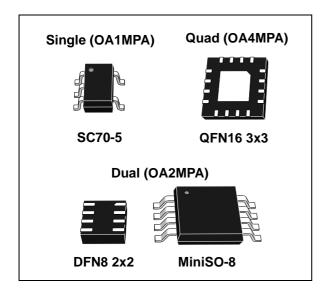


# OA1MPA, OA2MPA, OA4MPA

# High precision low-power CMOS op amp

**Datasheet - production data** 



#### **Features**

Low offset voltage: 200 µV max.

Low power consumption: 10 μA at 5 V

Low supply voltage: 1.5 V to 5.5 V

Gain bandwidth product: 150 kHz typ.

Low input bias current: 1 pA typ.

• Rail-to-rail input and output

EMI hardened operational amplifiers

High tolerance to ESD: 4 kV HBM

Extended temperature range: -40 to +125 °C

### **Benefits**

High precision without calibration

- Energy saving
- Guaranteed operation on low-voltage battery

### **Applications**

- Wearable
- Fitness and healthcare
- Medical instrumentation

### **Description**

The OA1MPA, OA2MPA, OA4MPA series of single, dual, and quad operational amplifiers offer low-voltage operation, rail-to-rail input and output, and excellent precision ( $V_{io}$  lower than 200  $\mu V$  at 25 °C).

These low power op amps benefit from STMicroelectronics 5 V CMOS technology and offer an excellent speed/power consumption ratio (150 kHz typical gain bandwidth) while consuming less than 14  $\mu A$  at 5 V. The OA1MPA, OA2MPA, OA4MPA series also feature an ultra-low input bias current.

The OA1MPA, OA2MPA, OA4MPA are respectively the single, dual and quad operational amplifier versions and are housed in the smallest industrial package.

The OA1MPA, OA2MPA, OA4MPA family is the ideal choice for wearable, fitness and healthcare applications.

**Table 1. Device summary** 

Order code	Temperature range	Package	Packaging	Marking
OA1MPA22C		SC70-5		K1W
OA2MPA22Q	40° C to 1425° C	DFN8 2x2	Tana and real	K1W
OA2MPA34S	-40° C to +125° C	MiniSO8	Tape and reel	V712
OA4MPA33Q		QFN16 3x3		K1W

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### 1 Pin connections

**Single** 5 VCC+ VCC- 2 4 OUT IN- 3 **SC70-5 (OA1MPA)** Dual 0 VCC+ VCC+ OUT1 OUT1 OUT2 OUT2 IN1-IN1+ IN2-IN1+ IN2-VCC-IN2+ VCC-IN2+ DFN8 2x2 (OA2MPA) MiniSO-8 (OA2MPA) Quad 15 14 IN1+ IN4+ 12 VCC-VCC+ 2 NC<sup>(1)</sup> 3 10 NC NC IN2+ IN3+ IN3-QFN16 3x3 (OA4MPA)

Figure 1. Pin connections (top view)

1. The exposed pads of the QFN16 3x3 can be connected to VCC- or left floating.

# 2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply voltage <sup>(1)</sup>	6	
V <sub>id</sub>	Differential input voltage <sup>(2)</sup>	±V <sub>CC</sub>	V
V <sub>in</sub>	Input voltage <sup>(3)</sup>	V <sub>CC-</sub> - 0.2 to V <sub>CC+</sub> + 0.2	
I <sub>in</sub>	Input current <sup>(4)</sup>	10	mA
T <sub>stg</sub>	Storage temperature	-65 to +150	°C
R <sub>thja</sub>	Thermal resistance junction-to-ambient <sup>(5)(6)</sup> SC70-5 DFN8 2x2 MiniSO8 QFN16 3x3	205 120 190 45	°C/W
R <sub>thjc</sub>	Thermal resistance junction-to-case DFN8 2x2	33	
Tj	Maximum junction temperature	150	°C
	HBM: human body model <sup>(7)</sup>	4	kV
	MM: machine model for OA1MPA <sup>(8)</sup>	150	
ESD	MM: machine model for OA2MPA <sup>(8)</sup>	200	V
ESD	MM: machine model for OA4MPA <sup>(8)</sup>	300	
	CDM: charged device model except MiniSO8 <sup>(9)</sup>	1.5	kV
	CDM: charged device model for MiniSO8 <sup>(9)</sup>	1.3	KV
	Latch-up immunity	200	mA

- 1. All voltage values, except the differential voltage are with respect to the network ground terminal.
- The differential voltage is a non-inverting input terminal with respect to the inverting input terminal. The OA2MPA and OA4MPA devices include an internal differential voltage limiter that clamps internal differential voltage at 0.5 V.
- 3.  $V_{CC}$   $V_{in}$  must not exceed 6 V,  $V_{in}$  must not exceed 6 V.
- 4. Input current must be limited by a resistor in series with the inputs.
- 5. Short-circuits can cause excessive heating and destructive dissipation.
- 6. R<sub>th</sub> are typical values.
- 7. Human body model: 100 pF discharged through a 1.5 k $\Omega$  resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
- Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two
  pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin
  combinations with other pins floating.</li>
- Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to ground.

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**Table 3. Operating conditions** 

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply voltage	1.5 to 5.5	V
V <sub>icm</sub>	Common mode input voltage range	$V_{CC-}$ - 0.1 to $V_{CC+}$ + 0.1	V
T <sub>oper</sub>	Operating free air temperature range	-40 to +125	°C



# 3 Electrical characteristics

 $V_{CC+}$  = 1.8 V with  $V_{CC-}$  = 0 V,  $V_{icm}$  =  $V_{CC}/2,$  T = 25 °C, and  $R_L$  = 10  $k\Omega$  connected to  $V_{CC}/2$  (unless otherwise specified)

**Table 4. Electrical characteristics** 

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
DC perfori	mance					
		T = 25 °C			200	
$V_{io}$	Input offset voltage (V <sub>icm</sub> = 0 V)	-40 °C < T< 85 °C			850	μV
	(Vicm - O V)	-40 °C < T< 125 °C			1200	
ΔV <sub>io</sub> /ΔΤ	Input offset voltage drift	-40 °C < T< 125 °C <sup>(1)</sup>			10	μV/°C
1	Input offset current	T = 25 °C		1	10 <sup>(2)</sup>	
l <sub>io</sub>	$(V_{out} = V_{CC}/2)$	-40 °C < T< 125 °C		1	300 <sup>(2)</sup>	- ^
ı	Innut his surrent ()/ // /2)	T = 25 °C		1	10 <sup>(2)</sup>	рA
l <sub>ib</sub>	Input bias current (V <sub>out</sub> = V <sub>CC</sub> /2)	-40 °C < T< 125 °C		1	300 <sup>(2)</sup>	
	Common mode rejection ratio	T = 25 °C	69	88		
CMR	$ \begin{aligned} &20 \log \left(\Delta V_{icm}/\Delta V_{io}\right) \\ &V_{icm} = 0 \text{ V to } V_{CC}, \\ &V_{out} = V_{CC}/2, \text{ R}_L > 1 \text{ M}\Omega \end{aligned} $	-40 °C < T< 125 °C	61			dB
Δ.	Large signal voltage gain $V_{out} = 0.5 \text{ V}$ to $(V_{CC} - 0.5 \text{ V})$ $T = 25 \text{ °C}$ $-40 \text{ °C} < T < 125 \text{ °C}$	T = 25 °C	95			
$A_{vd}$		-40 °C < T< 125 °C	85			
V	High level output voltage	T = 25 °C			75	
$V_{OH}$	$(V_{OH} = V_{CC} - V_{out})$	-40 °C < T< 125 °C			80	mV
V.	Lave lavel autout valtage	T = 25 °C			40	1111
$V_{OL}$	Low level output voltage	-40 °C < T< 125 °C			60	
	1	T = 25 °C	6	12		
	$I_{\text{sink}} (V_{\text{out}} = V_{\text{CC}})$	-40 °C < T< 125 °C	4			mA
l <sub>out</sub>	1	T = 25 °C	5	7		IIIA
	I <sub>source (</sub> V <sub>out</sub> = 0 V)	-40 °C < T< 125 °C	3			
1	Supply current (per channel,	T = 25 °C		9	14	
I <sub>CC</sub>	$V_{out} = V_{CC}/2$ , $R_L > 1 M\Omega$	-40 °C < T< 125 °C			16	μA
AC perfori	mance					
GBP	Gain bandwidth product		100	120		1.11=
Fu	Unity gain frequency	- 1010 C 100 F		100		kHz
$F_{m}$	Phase margin	$R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF}$		45		Degrees
G <sub>m</sub>	Gain margin			19		dB

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
SR	Slew rate <sup>(3)</sup>	$R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF},$ $V_{out} = 0.5 \text{ V to V}_{CC} - 0.5 \text{ V}$		0.04		V/µs
	Equivalent input noise voltage	f = 1 kHz		100		nV
e <sub>n</sub>		f = 10 kHz		96		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
t <sub>init</sub>	Initialization time <sup>(4)</sup>	T = 25 °C			5	ms
		-40 °C < T< 125 °C			60	ms

- 1. See Section 4.4: Input offset voltage drift over temperature.
- 2. Guaranteed by characterization.
- 3. Slew rate value is calculated as the average between positive and negative slew rates.
- Initialization time is defined as the delay after power-up to guarantee operation within specified performances. Guaranteed by design. See Section 4.6: Initialization time.



 $V_{CC+}$  = 3.3 V with  $V_{CC-}$  = 0 V,  $V_{icm}$  =  $V_{CC}/2,$  T = 25 °C, and  $R_L$  = 10  $k\Omega$  connected to  $V_{CC}/2$  (unless otherwise specified)

**Table 5. Electrical characteristics** 

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
DC perfor	mance					
		T = 25 °C			200	
$V_{io}$	Input offset voltage	-40 °C < T< 85 °C			850	μV
		-40 °C < T< 125 °C			1200	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 125 °C <sup>(1)</sup>			10	μV/°C
$\Delta V_{io}$	Long-term input offset voltage drift	T = 25 °C <sup>(2)</sup>		0.3		$\frac{\mu V}{\sqrt{month}}$
1	Input offset current	T = 25 °C		1	10 <sup>(3)</sup>	
l <sub>io</sub>	$(V_{out} = V_{CC}/2)$	-40 °C < T< 125 °C		1	300 <sup>(3)</sup>	nΛ
1	Input bias current (V <sub>out</sub> = V <sub>CC</sub> /2)	T = 25 °C		1	10 <sup>(3)</sup>	рA
I <sub>ib</sub>	Imput bias current (vout – vCC/2)	-40 °C < T< 125 °C		1	300 <sup>(3)</sup>	
	Common mode rejection ratio	T = 25 °C	80	100		
CMR	$ \begin{aligned} &20 \text{ log } (\Delta V_{\text{icm}}/\Delta V_{\text{io}}) \\ &V_{\text{icm}} = 0 \text{ V to } V_{\text{CC}}, V_{\text{out}} = V_{\text{CC}}/2, \\ &R_{\text{L}} > 1 \text{ M}\Omega \end{aligned} $	-40 °C < T< 125 °C	69			dB
۸	Large signal voltage gain	T = 25 °C	95			
$A_{vd}$	$V_{out} = 0.5 \text{ V to } (V_{CC} - 0.5 \text{ V})$	-40 °C < T< 125 °C	85			
V <sub>OH</sub>	High level output voltage	T = 25 °C			75	
▼OH	$(V_{OH} = V_{CC} - V_{out})$	-40 °C < T< 125 °C			80	mV
$V_{OL}$	Low level output voltage	T = 25 °C			40	111 V
VOL.	20W 10V01 Odiput Voltago	-40 °C < T< 125 °C			60	
	$I_{\text{sink}}(V_{\text{out}} = V_{\text{CC}})$	T = 25 °C	20	34		
l <sub>out</sub>	-Sirik ( Fout FGC)	-40 °C < T< 125 °C	15			mA
·out	I <sub>source (</sub> V <sub>out</sub> = 0 V)	T = 25 °C	20	26		1117 (
	Source (Four 9 F)	-40 °C < T< 125 °C	15			
I <sub>cc</sub>	Supply current (per channel,	T = 25 °C		9	14	μA
	$V_{\text{out}} = V_{\text{CC}}/2, R_{\text{L}} > 1 \text{ M}\Omega$	-40 °C < T< 125 °C			16	μ, ,
AC perfor	mance					
GBP	Gain bandwidth product		100	120		kHz
F <sub>u</sub>	Unity gain frequency	$R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF}$		100		NI IZ
F <sub>m</sub>	Phase margin			45		Degrees
G <sub>m</sub>	Gain margin			19		dB
SR	Slew rate <sup>(4)</sup>	$R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF},$ $V_{\text{out}} = 0.5 \text{ V to } V_{\text{CC}} - 0.5 \text{ V}$		0.05		V/μs

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
e <sub>n</sub>	Equivalent input noise voltage	f = 1 kHz		100		nV
	Equivalent input noise voltage	f = 10 kHz		96		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
t <sub>init</sub>	Initialization time <sup>(5)</sup>	T = 25 °C			5	ma
	initialization time.	-40 °C < T< 125 °C			50	ms

- 1. See Section 4.4: Input offset voltage drift over temperature.
- 2. Typical value is based on the V<sub>io</sub> drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration. See Section 4.5: Long-term input offset voltage drift.
- 3. Guaranteed by characterization.
- 4. Slew rate value is calculated as the average between positive and negative slew rates.
- Initialization time is defined as the delay after power-up which guarantees operation within specified performances. Guaranteed by design. See Section 4.6: Initialization time.



 $V_{CC+}$  = 5 V with  $V_{CC-}$  = 0 V,  $V_{icm}$  =  $V_{CC}/2,$  T = 25 °C, and  $R_L$  = 10  $k\Omega$  connected to  $V_{CC}/2$  (unless otherwise specified)

**Table 6. Electrical characteristics** 

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit	
DC perfori	mance						
		T = 25 °C					
$V_{io}$	Input offset voltage	-40 °C < T< 85 °C			850	μV	
		-40 °C < T< 125 °C			1200		
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 125 °C <sup>(1)</sup>			10	μV/°C	
$\Delta V_{io}$	Long-term input offset voltage drift	T = 25 °C <sup>(2)</sup>		0.7		$\frac{\mu V}{\sqrt{month}}$	
	Input offset current	T = 25 °C		1	10 <sup>(3)</sup>		
l <sub>io</sub>	$(V_{out} = V_{CC}/2)$	-40 °C < T< 125 °C		1	300 <sup>(3)</sup>	1	
	Input bias current	T = 25 °C		1	10 <sup>(3)</sup>	- pA	
I <sub>ib</sub>	$(V_{out} = V_{CC}/2)$	-40 °C < T< 125 °C		1	300 <sup>(3)</sup>		
	Common mode rejection ratio	T = 25 °C	74	94			
CMR	$ \begin{aligned} &20 \text{ log } (\Delta V_{\text{icm}}/\Delta V_{\text{io}}) \\ &V_{\text{icm}} = 0 \text{ V to } V_{\text{CC}}, \\ &V_{\text{out}} = V_{\text{CC}}/2, \text{ R}_{\text{L}} > 1 \text{ M}\Omega \end{aligned} $	-40 °C < T< 125 °C	73				
	Supply voltage rejection ratio	T = 25 °C	71	90			
SVR	$ \begin{aligned} &20 \log \left(\Delta V_{CC}/\Delta V_{io}\right) \\ &V_{CC} = 1.5 \text{ to } 5.5 \text{ V},  V_{ic} = 0 \text{ V}, \\ &R_L > 1  M\Omega \end{aligned} $	-40 °C < T< 125 °C	71			dB	
^	Large signal voltage gain	T = 25 °C	95			, ab	
$A_{vd}$	$V_{out} = 0.5 \text{ V to } (V_{CC} - 0.5 \text{ V})$	-40 °C < T< 125 °C	85				
		V <sub>RF = 100 mVRFpeak</sub> , f = 400 MHz		38 <sup>(4)</sup>			
EMIRR	EMI rejection ratio	V <sub>RF = 100 mVRFpeak</sub> , f = 900 MHz		50 <sup>(4)</sup>			
LIVIIKK	EMIRR = 20 log $(V_{RFpeak}/\Delta V_{io})$	V <sub>RF = 100 mVRFpeak</sub> , f = 1800 MHz		60 <sup>(4)</sup>			
	p.s	V <sub>RF = 100 mVRFpeak</sub> , f = 2400 MHz		63 <sup>(4)</sup>			
$V_{OH}$	High level output voltage	T = 25 °C			75		
VОН	$(V_{OH} = V_{CC} - V_{out})$	-40 °C < T< 125 °C			80	mV	
V <sub>a</sub> .	Low level output voltage	T = 25 °C			40	liiv	
V <sub>OL</sub>	Low level output voltage	-40 °C < T< 125 °C			60		
	$I_{sink} (V_{out} = V_{CC})$	T = 25 °C	35	56			
1	'SINK ( VOUT VCC)	-40 °C < T< 125 °C	20			mA	
l <sub>out</sub>	J	T = 25 °C	35	45		111/4	
	I <sub>source (</sub> V <sub>out</sub> = 0 V)	-40 °C < T< 125 °C	20				



Table 6. Electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit	
ı	Supply current (per channel,	T = 25 °C		10	14		
I <sub>CC</sub>	$V_{\text{out}} = V_{\text{CC}}/2, R_{\text{L}} > 1 \text{ M}\Omega$	-40 °C < T< 125 °C			16	μΑ	
AC perfori	mance						
GBP	Gain bandwidth product		110	150		kHz	
F <sub>u</sub>	Unity gain frequency	$R_1 = 10 \text{ k}Ω, C_1 = 100 \text{ pF}$		120		KHZ	
F <sub>m</sub>	Phase margin	$ K_L  = 10 \text{ ks2, GL} = 100 \text{ pr}$		45		Degrees	
G <sub>m</sub>	Gain margin			19		dB	
SR	Slew rate <sup>(5)</sup>	$R_L = 10 \text{ k}\Omega$ , $C_L = 100 \text{ pF}$ , $V_{out} = 0.5 \text{ V to V}_{CC} - 0.5 \text{ V}$		0.06		V/μs	
∫e <sub>n</sub>	Low-frequency peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		10		μV <sub>pp</sub>	
e <sub>n</sub>	Equivalent input noise voltage	f = 1 kHz		100		nV	
on	Equivalent input noise voltage	f = 10 kHz		96		<u>nV</u> √Hz	
THD+N	Total harmonic distortion + noise	$\begin{split} f_{in} &= 1 \text{ kHz, A}_{CL} = 1, \\ R_{L} &= 100 \text{ k}\Omega, \text{ V}_{icm} = (\text{V}_{CC} \text{ - 1 V})/2, \\ \text{BW} &= 22 \text{ kHz, V}_{out} = 0.5 \text{ V}_{pp} \end{split}$		0.008		%	
+	Initialization time <sup>(6)</sup>	T = 25 °C			5	me	
t <sub>init</sub>	milianzation time.	-40 °C < T< 125 °C			50	- ms	

<sup>1.</sup> See Section 4.4: Input offset voltage drift over temperature.

Typical value is based on the V<sub>io</sub> drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration. See Section 4.5: Long-term input offset voltage drift.

<sup>3.</sup> Guaranteed by characterization.

<sup>4.</sup> Tested on SC70-5 package.

<sup>5.</sup> Slew rate value is calculated as the average between positive and negative slew rates.

<sup>6.</sup> Initialization time is defined as the delay after power-up to guarantee operation within specified performances. Guaranteed by design. See Section 4.6: Initialization time.

Figure 2. Supply current vs. supply voltage at  $V_{icm} = V_{CC}/2$ 

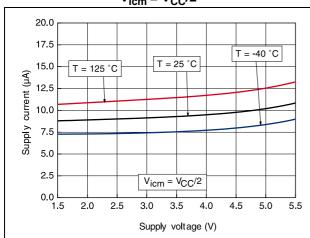


Figure 3. Input offset voltage distribution at  $V_{CC} = 5 \text{ V}, V_{icm} = V_{CC}/2$ 

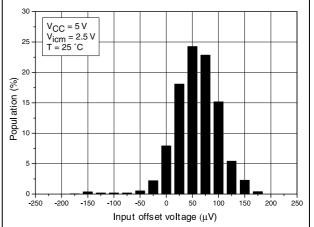


Figure 4. Input offset voltage distribution at  $V_{CC}$  = 3.3 V,  $V_{icm}$  =  $V_{CC}/2$ 

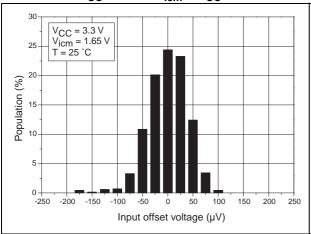


Figure 5. Input offset voltage temperature coefficient distribution

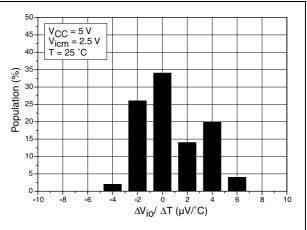
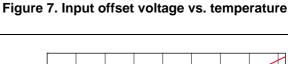
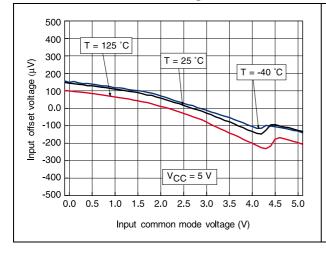
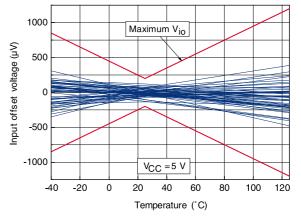


Figure 6. Input offset voltage vs. input common mode voltage



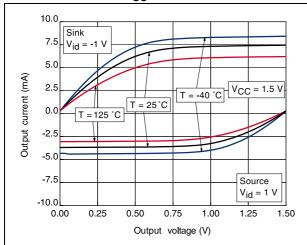




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Figure 8. Output current vs. output voltage at  $V_{CC} = 1.5 \text{ V}$ 

Figure 9. Output current vs. output voltage at  $V_{CC} = 5 \text{ V}$ 



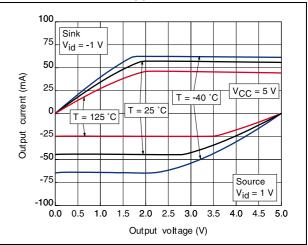
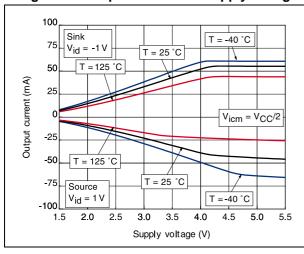


Figure 10. Output current vs. supply voltage

Figure 11. Bode diagram at  $V_{CC} = 1.5 \text{ V}$ 



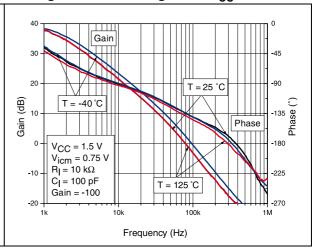
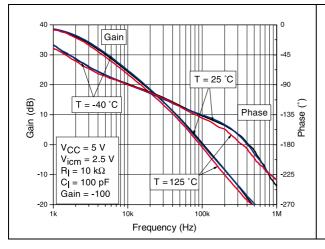


Figure 12. Bode diagram at  $V_{CC} = 5 \text{ V}$ 

Figure 13. Closed-loop gain diagram vs. capacitive load



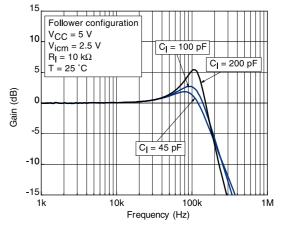




Figure 14. Positive slew rate

2.5 2.0 1.5 1.0 Output voltage (V) T = 125 °C 0.5 0.0 T = 25 °C -0.5 -1.0 V<sub>CC</sub> = 5 V V<sub>icm</sub> = V<sub>CC</sub>/2 C<sub>I</sub> = 100 pF  $T = -40 \,^{\circ}C$ -1.5 -2.0  $R_I = 10 \text{ k}\Omega$ -2.5 75 125 25 50 100 150 Time (µs)

Figure 15. Negative slew rate

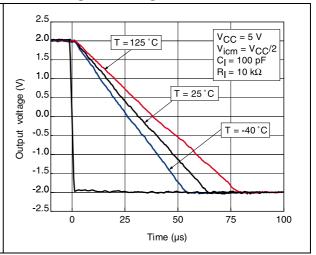


Figure 16. Slew rate vs. supply voltage

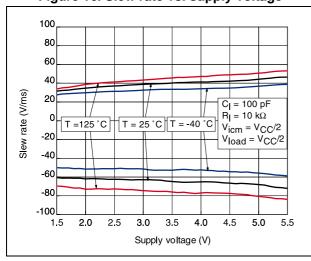


Figure 17. Noise vs. frequency

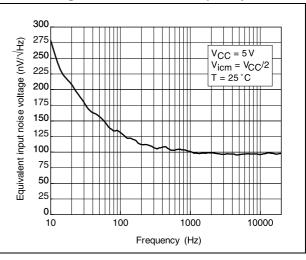


Figure 18. 0.1 Hz to 10 Hz noise

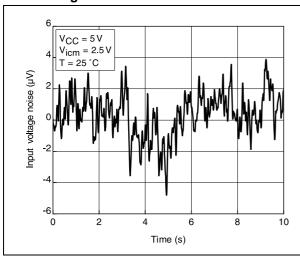
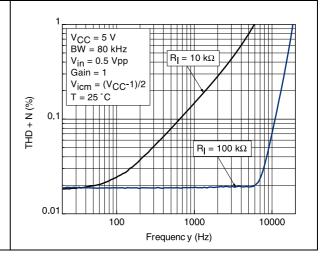


Figure 19. THD+N vs. frequency

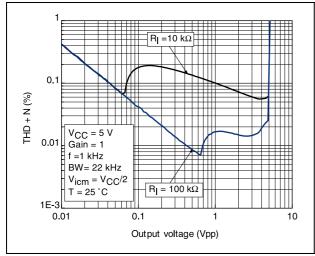


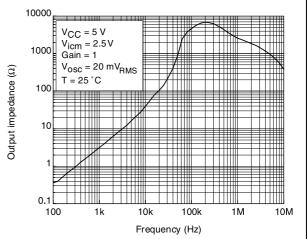
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Figure 20. THD+N vs. output voltage

Figure 21. Output impedance vs. frequency in closed-loop configuration







## 4 Application information

### 4.1 Operating voltages

The OA1MPA, OA2MPA, and OA4MPA series of devices can operate from 1.5 V to 5.5 V. The parameters are fully specified for 1.8 V, 3.3 V, and 5 V power supplies. However, they are very stable in the full  $V_{CC}$  range and several characterization curves show OA1MPA, OA2MPA, and OA4MPA device characteristics at 1.5 V. In addition, the main specifications are guaranteed in the extended temperature range from -40 °C to +125 °C.

### 4.2 Rail-to-rail input

The OA1MPA, OA2MPA, and OA4MPA devices have a rail-to-rail input, and the input common mode range is extended from  $V_{CC-}$ - 0.1 V to  $V_{CC+}$  + 0.1 V.

### 4.3 Rail-to-rail output

The output levels of the OA1MPA, OA2MPA, and OA4MPA operational amplifiers can go close to the rails: to a maximum of 40 mV below the upper rail and to a maximum of 75 mV above the lower rail when a 10 k $\Omega$  resistive load is connected to  $V_{CC}/2$ .

### 4.4 Input offset voltage drift over temperature

The maximum input voltage drift over the temperature variation is defined as the offset variation related to offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift over temperature is computed using *Equation 1*.

#### **Equation 1**

$$\frac{\Delta V_{io}}{\Delta T} = \text{max} \left| \frac{V_{io}(T) - V_{io}(25^{\circ}C)}{T - 25^{\circ}C} \right|$$

with T = -40 °C and 125 °C.

The datasheet maximum value is guaranteed by a measurement on a representative sample size ensuring a  $C_{\rm pk}$  (process capability index) greater than 1.33.

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### 4.5 Long-term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using *Equation 2*.

#### **Equation 2**

$$A_{FV} \, = \, e^{\beta \cdot (V_S - V_U)}$$

#### Where:

A<sub>FV</sub> is the voltage acceleration factor

 $\beta$  is the voltage acceleration constant in 1/V, constant technology parameter ( $\beta$  = 1)

V<sub>S</sub> is the stress voltage used for the accelerated test

V<sub>II</sub> is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in Equation 3.

#### **Equation 3**

$$A_{FT} \, = \, e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S}\right)}$$

#### Where:

A<sub>FT</sub> is the temperature acceleration factor

Ea is the activation energy of the technology based on the failure rate

k is the Boltzmann constant (8.6173 x 10<sup>-5</sup> eV.K<sup>-1</sup>)

 $T_{IJ}$  is the temperature of the die when  $V_{IJ}$  is used (K)

T<sub>S</sub> is the temperature of the die under temperature stress (K)

The final acceleration factor,  $A_F$ , is the multiplication of the voltage acceleration factor and the temperature acceleration factor (*Equation 4*).

#### **Equation 4**

$$A_F = A_{FT} \times A_{FV}$$

 $A_F$  is calculated using the temperature and voltage defined in the mission profile of the product. The  $A_F$  value can then be used in *Equation 5* to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

#### **Equation 5**

 $Months = A_F \times 1000 \ h \times 12 \ months / (24 \ h \times 365.25 \ days)$ 

To evaluate the op amp reliability, a follower stress condition is used where  $V_{CC}$  is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules).

The  $V_{io}$  drift (in  $\mu V$ ) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see *Equation 6*).

#### **Equation 6**

$$V_{CC} = maxV_{op} \text{ with } V_{icm} = V_{CC}/2$$

The long term drift parameter ( $\Delta V_{io}$ ), estimating the reliability performance of the product, is obtained using the ratio of the  $V_{io}$  (input offset voltage value) drift over the square root of the calculated number of months (*Equation 7*).

#### **Equation 7**

$$\Delta V_{io} = \frac{V_{io} drift}{\sqrt{(months)}}$$

where  $V_{io}$  drift is the measured drift value in the specified test conditions after 1000 h stress duration.

### 4.6 Initialization time

The OA1MPA, OA2MPA, and OA4MPA series of devices use a proprietary trimming topology that is initiated at each device power-up and allows excellent  $V_{io}$  performance to be achieved. The initialization time is defined as the delay after power-up which guarantees operation within specified performances. During this period, the current consumption ( $I_{CC}$ ) and the input offset voltage ( $V_{io}$ ) can be different to the typical ones.

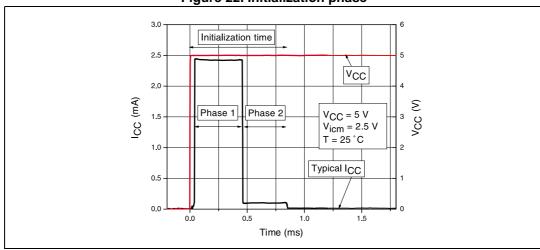


Figure 22. Initialization phase

The initialization time is  $V_{CC}$  and temperature dependent. *Table 7* sums up the measurement results for different supply voltages and for temperatures varying from -40 °C to 125 °C.

V (V)	Temperature: -40 °C		Temperature: 25 °C		Temperature: 125 °C		
V <sub>CC</sub> (V)	T <sub>init</sub> (ms)	I <sub>CC</sub> phase 1 (mA)	T <sub>init</sub> (ms)	I <sub>CC</sub> phase 1 (mA)	T <sub>init</sub> (ms)	I <sub>CC</sub> phase 1 (mA)	
1.8	37	0.33	3.2	0.40	0.35	0.46	
3.3	2.9	1.4	0.95	1.3	0.34	1.2	
5	2.4	3.2	0.85	2.4	0.31	2.9	

Table 7. Initialization time measurement results

# 4.7 PCB layouts

For correct operation, it is advised to add a 10 nF decoupling capacitors as close as possible to the power supply pins.

### 4.8 Macromodel

Accurate macromodels of the OA1MPA, OA2MPA, and OA4MPA devices are available on the STMicroelectronics' website at <a href="https://www.st.com">www.st.com</a>. These model are a trade-off between accuracy and complexity (that is, time simulation) of the OA1MPA, OA2MPA, and OA4MPA op amp. They emulate the nominal performance of a typical device within the specified operating conditions mentioned in the datasheet. They also help to validate a design approach and to select the right op amp, but they do not replace on-board measurements.

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# 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: <a href="https://www.st.com">www.st.com</a>. ECOPACK<sup>®</sup> is an ST trademark.



# 5.1 SC70-5 package information

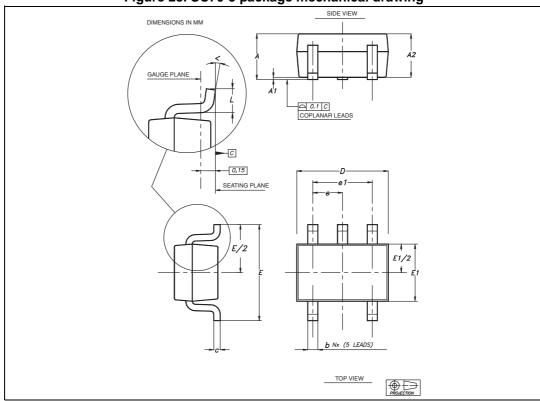


Figure 23. SC70-5 package mechanical drawing

Table 8. SC70-5 package mechanical data

		Dimensions								
Symbol	Millimeters			Inches						
	Min.	Тур.	Max.	Min.	Тур.	Max.				
Α	0.80		1.10	0.032		0.043				
A1	0		0.10			0.004				
A2	0.80	0.90	1.00	0.032	0.035	0.039				
b	0.15		0.30	0.006		0.012				
С	0.10		0.22	0.004		0.009				
D	1.80	2.00	2.20	0.071	0.079	0.087				
E	1.80	2.10	2.40	0.071	0.083	0.094				
E1	1.15	1.25	1.35	0.045	0.049	0.053				
е		0.65			0.025					
e1		1.30			0.051					
L	0.26	0.36	0.46	0.010	0.014	0.018				
<	0°		8°	0°		8°				

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# 5.2 DFN8 2x2 package information

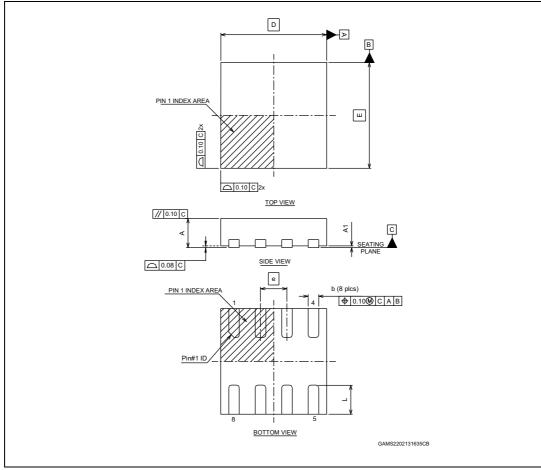


Figure 24. DFN8 2x2 package mechanical drawing

Table 9. DFN8 2x2 package mechanical data

	Dimensions						
Ref.	Millimeters			Inches			
	Min.	Тур.	Max.	Min.	Тур.	Max.	
А	0.70	0.75	0.80	0.028	0.030	0.031	
A1	0.00	0.02	0.05	0.000	0.001	0.002	
b	0.15	0.20	0.25	0.006	0.008	0.010	
D		2.00			0.079		
E		2.00			0.079		
е		0.50			0.020		
L	0.045	0.55	0.65	0.018	0.022	0.026	
N	8			8			

# 5.3 MiniSO-8 package information

Figure 25. MiniSO-8 package mechanical drawing

Table 10. MiniSO-8 package mechanical data

	Dimensions						
Ref.	Millimeters			Inches			
	Min.	Тур.	Max.	Min.	Тур.	Max.	
Α			1.1			0.043	
A1	0		0.15	0		0.006	
A2	0.75	0.85	0.95	0.030	0.033	0.037	
b	0.22		0.40	0.009		0.016	
С	0.08		0.23	0.003		0.009	
D	2.80	3.00	3.20	0.11	0.118	0.126	
E	4.65	4.90	5.15	0.183	0.193	0.203	
E1	2.80	3.00	3.10	0.11	0.118	0.122	
е		0.65			0.026		
L	0.40	0.60	0.80	0.016	0.024	0.031	
L1		0.95			0.037		
L2		0.25			0.010		
k	0°		8°	0 °		8°	
ccc			0.10			0.004	

# 5.4 QFN16 3x3 package information

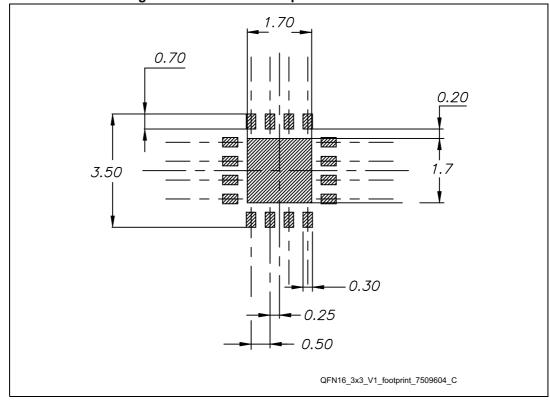
BOTTOM VIEW R (OPTIONAL) EXPOSED PAD PIN 1 -**L** 16x **b** 16x (4 LEADS PER SIDE) // 0.1 C -*A3* SEATING PLANE Ċ O.08 C LEADS COPLANARITY TOP VIEW QFN16\_3x3\_V1\_7509604\_C

Figure 26. QFN16 3x3 package mechanical drawing

Table 11. QFN16 3x3 mm package mechanical data (pitch 0.5 mm)

	Dimensions						
Ref.	Millimeters			Inches			
	Min.	Тур.	Max.	Min.	Тур.	Max.	
Α	0.80	0.90	1.00	0.031	0.035	0.039	
A1	0		0.05	0		0.002	
A3		0.20			0.008		
b	0.18		0.30	0.007		0.012	
D	2.90	3.00	3.10	0.114	0.118	0.122	
D2	1.50		1.80	0.059		0.071	
Е	2.90	3.00	3.10	0.114	0.118	0.122	
E2	1.50		1.80	0.059		0.071	
е		0.50			0.020		
L	0.30		0.50	0.012		0.020	

Figure 27. QFN16 3x3 footprint recommendation



# 6 Revision history

**Table 12. Document revision history** 

Date	Revision	Changes
28-Feb-2014	1	Initial release

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