```
-- Altera Memory Initialization File (MIF)

DEPTH = 1024;
WIDTH = 16;

ADDRESS_RADIX = HEX;
DATA_RADIX = HEX;

CONTENT
  BEGIN
    [000..3FF] : 0000;  -- Default to NOP

            000 : 0411;  -- Start:  LOAD    B
;Load value stored in B
            001 : 0C12;  --          ADD     C
;Add value stored in C
            002 : 0C13;  --          ADD     D
;Add value stored in D
            003 : 0810;  --          STORE   A
;Store value in A
            004 : 1404;  -- Here:    JUMP    Here
;Loop here forever
            010 : 0000;  -- A:       DW      &H0000
            011 : 0004;  -- B:       DW      &H0004
            012 : 0003;  -- C:       DW      &H0003
            013 : 0005;  -- D:       DW      &H0005
  END;
```

Figure 1. Machine code stored in source file *EXAMPLE.MIF* created using the Simple Computer assembler. These instructions are executed on the *SCOMP* and are used to compute $A = (B + C) + D$.

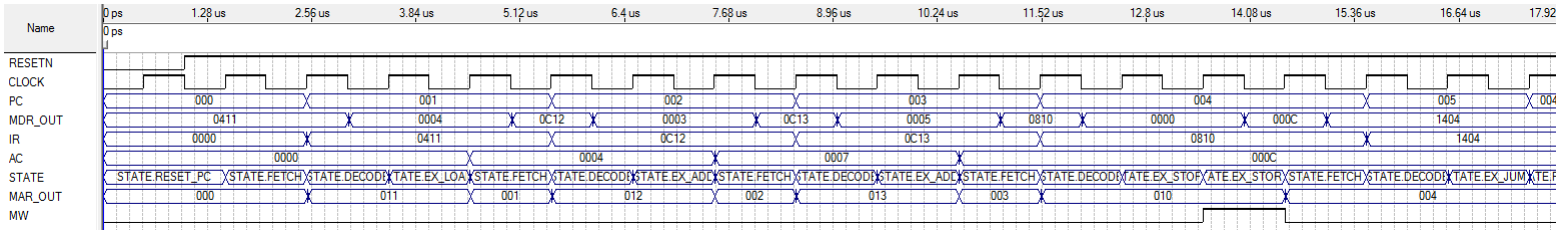

Figure 2. Timing simulation waveform of instructions stored in *EXAMPLE.MIF* being executed on *SCOMP*. A 1 us period is used, and *RESETN* is initially held *LOW* to reset the computer. Once the reset signal is pulled *HIGH*, a *FETCH* and *DECODE* cycle is performed to load the next instruction, *EX_LOAD*.

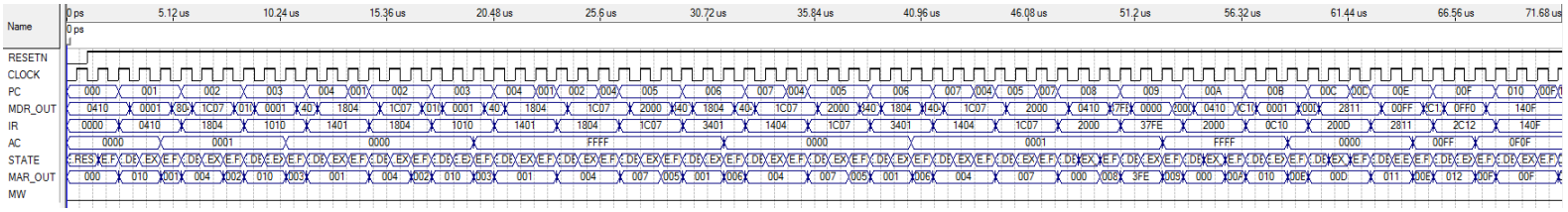

Figure 3. Timing simulation waveform of *SCOMP*, now with an extended number of instruction states, executing instructions stored in *TEST_CODE.MIF*. The clock frequency is set to 1 us, and the *RESETN* line is initially held *LOW* to reset the computer. The *AC* register ultimately retains the value 0x0F0F.

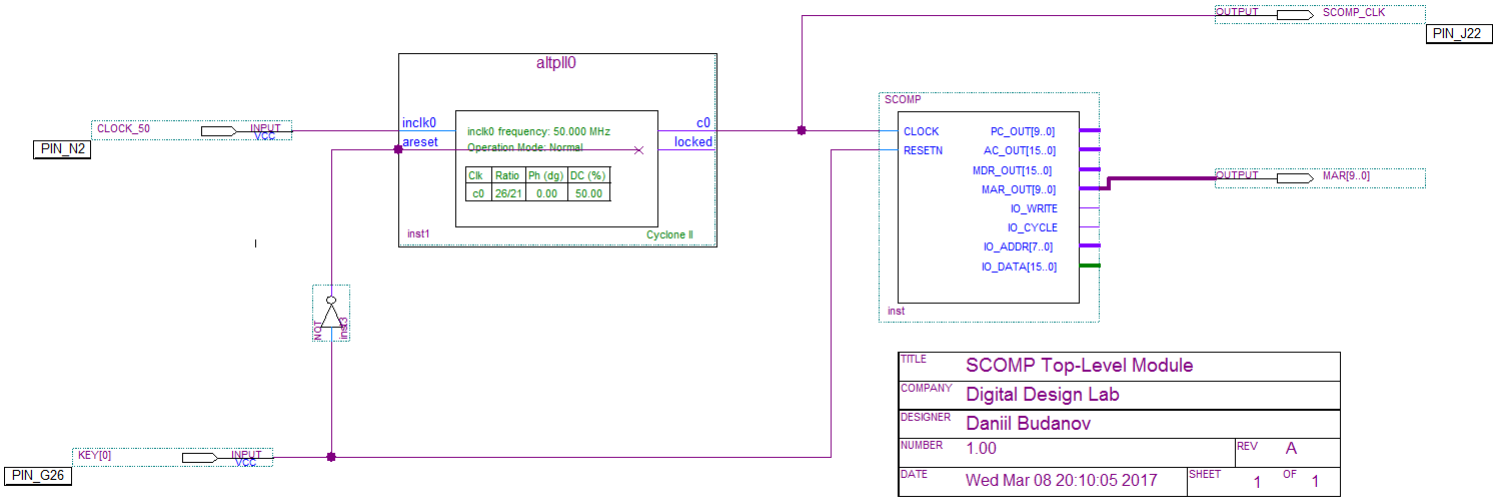

Figure 4. Schematic of Simple Computer with a PLL being input a 50 MHz clock from the *DE*2 board and supplying a clock signal at 61.90 MHZ. This clock output frequency is within 5 MHz of the 65.03 MHz operating maximum of *SCOMP*, as given by the Timing Summary. *KEY*[0] is used to reset both the PLL and the *SCOMP*, and the PLL output is routed to a physical pin *J*22 on the FPGA.

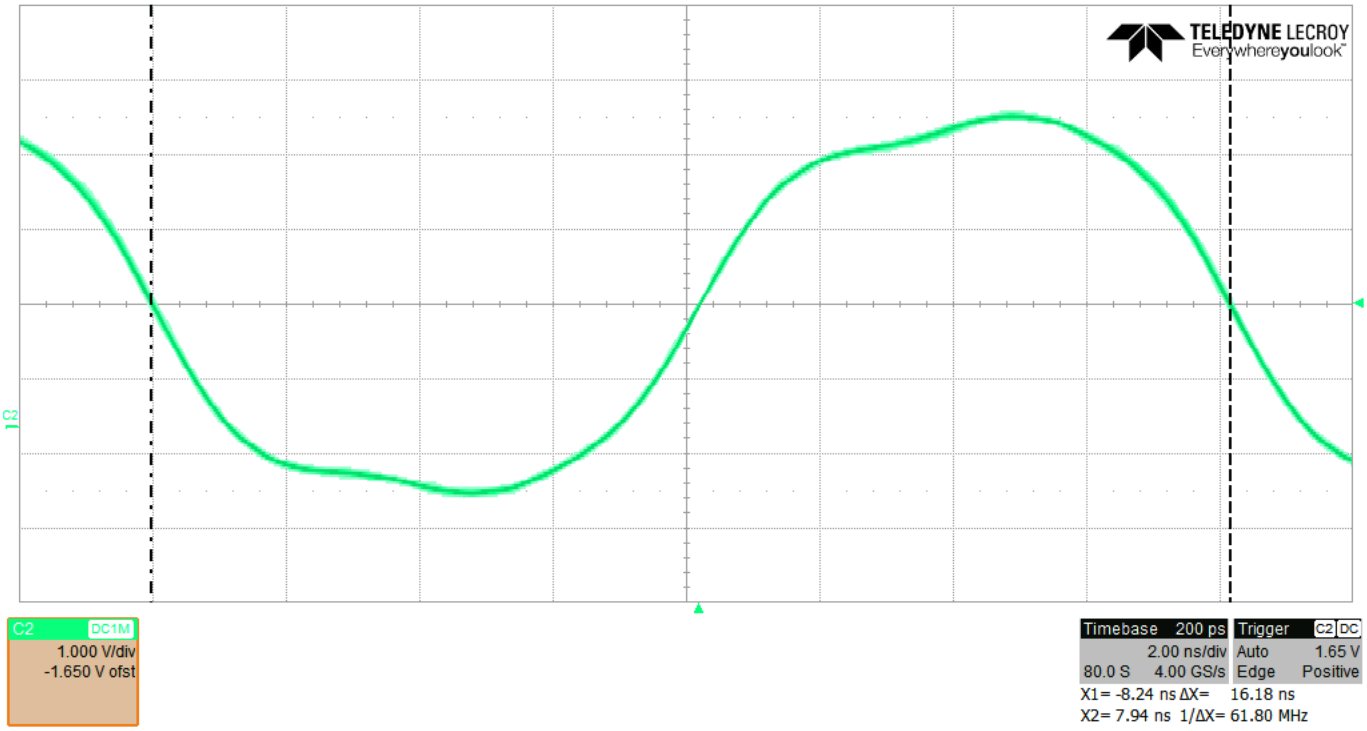

Figure 5. Oscilloscope waveform of the clock signal being output by the PLL into the *SCOMP*. A 16.18 ns clock period is measured.