Daniil Budanov

github.com/danbudanov dbudanov3@gatech.edu
linkedin.com/in/danbudanov *(404) 457 2051 (cell)*

Skills

- Experience with SystemVerilog, C, C++, Python, Java, MATLAB, C++, EagleCAD
- Utilized FreeRTOS, MRAA/UPM, mbed, OpenCV, Theano, GNU Radio, and Altera tools
- Fluent in Russian and English
- Technical research and presentation skills
- Experienced with laboratory test equipment and LTSpice circuit simulation

Employment History

Tesla / Test Engineering Intern
January 2018 - Present, Fremont, CA

Contributes to design of testers for remanufacturing team by analyzing vehicle firmware, streamlining communication between tester and vehicle, and diagnosing tester failures. Documents firmware for systems under test, and develops scripts to facilitate device debugging and data post-processing for remanufacturing purposes.

LF Lab at Georgia Tech / Undergraduate Researcher
August 2017 - December 2017, Atlanta, GA

Created Verilog IP and architecture for the Mini AWESOME ELF/VLF Receiver SDR based on an Intel SoC.

Intel Corporation / Software Engineering Intern
June 2017 - August 2017, Hillsboro, OR

Supported Intel's MRAA and UPM low-level I/O and sensor libraries. Developed soft IP and hardware abstraction libraries to ease software developer use of Intel SoC and FPGA platforms. Built demo to showcase benefits of SoCs in industrial hardware/software development.

May 2016 - August 2016, Hillsboro, OR

Built computer vision applications on Intel's IoT hardware for security applications in connected cities and created demo and workshop content to engage computer vision developers in IoT.

Georgia Tech Research Institute / Engineering Co-op
August 2016 -December 2016, Atlanta, GA

Worked in the **Information and Communications Laboratory;** Deployed software defined radio projects involving filter implementation in Verilog, automatic modulation recognition using machine learning techniques, and testbed construction for modeling radio infrastructures.

Education

Georgia Institute of Technology / B.Sc. in Computer Engineering
August 2015 - Present, Atlanta, GA | Expected Graduation Fall 2019
GPA: 3.60 / 4.0

Technical Activities

HyperJackets / Electrical Team Member, Constitutional Advisor, Former Team Lead
October 2017 - Present
Develops electrical development roadmaps and system specifications, designs and reviews electronic circuits, designs firmware based on FreeRTOS for pod ECUs for SpaceX's Hyperloop competition.

RoboJackets / Vice President
September 2015 - December 2017, Atlanta, GA
Performs administrative duties for Georgia Tech's collegiate competitive robotics organization.

Intelligent Ground Vehicle Competition / Electrical Subteam Lead
September 2015 - May 2017
Led team that maintains and deploys power and embedded systems for a 300-lb autonomous vehicle.

Electrical Training / Team Lead
September 2016 - December 2016
Developed curriculum and managed team that guided incoming members through designing, constructing, and programming an electrical system.