YICHEN ZHANG
Matriculation number S2130520
MSc Hons Project Phase 1 Report
<Insert Project Title Here>
Edit previous line with correct
project type
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Mission Statement

Background

Simulation Program with Integrated Circuit Emphasis or SPICE has now been widely used in the IC design and verification. Solving of sparse matrices often takes up most of the SPICE simulation time. Lower–upper (LU) decomposition is the most commonly used method to solve matrices. It factorizes a matrix into two factors – a lower triangular matrix L and an upper triangular matrix U. In this way, we only need to solve triangular systems to get results. However, the sparse-matrix computation is hard to parallelize on regular processors due to the irregular structure of the matrices. Modern FPGAs, however, have the potential to compute these hard-to-parallelise problems more efficiently due to its flexible reconfigurability.

Aim & Tasks

Implement LU Decomposition on FPGAs and accelerate it.

- To implement LU decomposition with C++.
- To implement LU decomposition on FPGA.
- Test the power consumption and efficiency of the algorithm on FPGA.
- Accelerate the LU decomposition by parallelization and make it robust enough for circuit simulation application.
- Produce a parallel FPGA-based Matrix Solver.

Background Knowledge

- C++ is designed with an orientation towards system programming and embedded. It offers a direct hardware mapping and can be synthesized into FPGA. Modern C++ has also provided parallel version of many algorithms.
- Verilog is a hardware description language. It is commonly used in design and verification of digital circuit in register-transfer level and can be physically realized by synthesis software.

Resources

- Xilinx Vitis
  The Vitis unified software platform is a free new tool that combines all aspects of Xilinx software development into one unified environment. It enables accelerated applications on various Xilinx platforms including FPGAs. It is easy to get from Xilinx official website.

- Intel oneAPI
  oneAPI is a cross-industry, open, standards-based unified programming model that delivers a common developer experience across accelerator architectures. It provides optimized compilers, libraries, frameworks and analysis tools for development on CPUs, GPUs and FPGAs. It provides free access through Intel official website.

Abstract

The abstract should be a concise ($\leq$200 words) description of the project.

Declaration of Originality

I declare that this thesis is my
original work except where stated.

.....

Statement of Achievement

This is a brief statement outlining what you yourself (as opposed to your supervisor, technical staff, team members if you were working in a team, etc.) contributed to the project and what you yourself achieved. The statement need not be more than a couple of paragraphs and should certainly not take up more than one side of A4.

Contents

List of Figures

List of Tables

List of Symbols

#	Pound sign; used with the meaning “number of”.
θ	Angle between the radial line and the z-plane.

Glossary

POSIX Some description field.

RAII Resource Acquisition is Initialisation.

Chapter 1

Introduction and Background

1.1 Project overview

1.1.1 Subsection 1

1.1.2 Subsection 2

1.2 Summary

See Figure 1.1 on page 1 for an example of a figure. [1]

(a) Captions go below the figure. Remember to cite sources if needed.

(b) As above.

Figure 1.1: A figure with two subfigures in it.

[1] This is a footnote that incidentally contains a citation [1].

Chapter 2

Background

2.1 titles

$$x + 1 = 5 \tag{2.1}$$

POSIX is listed in the glossary. The second mention of POSIX will not be set in boldface.

2.1.1 more titles

$$dd = 5 \tag{2.2}$$

[2]

2.1.2 sections sections...

[3] [4]

2.2 Hello

$$y + 2 - x = 2 \tag{2.3}$$

Chapter 3

Conclusion

$$\frac{2}{5} \tag{3.1}$$

Acknowledgements

θ

References

[1] N. Kapre and A. DeHon, 'Parallelizing sparse matrix solve for spice circuit simulation using fpgas,' in *2009 International Conference on Field-Programmable Technology*, Dec. 2009, pp. 190–198. DOI: 10.1109/FPT.2009.5377665.

[2] E. P. Natarajan, 'Klu–a high performance sparse linear solver for circuit simulation problems,' Ph.D. dissertation, University of Florida, 2005.

[3] R. Kastner, J. Matai and S. Neuendorffer, 'Parallel Programming for FPGAs,' *arXiv e-prints*, arXiv:1805.03648, arXiv:1805.03648, May 2018. arXiv: 1805.03648 [cs.AR].

[4] L. H. Crockett, R. A. Elliot, M. A. Enderwitz and R. W. Stewart, *The Zynq Book: Embedded Processing with the Arm Cortex-A9 on the Xilinx Zynq-7000 All Programmable Soc.* Glasgow, GBR: Strathclyde Academic Media, 2014, ISBN: 099297870X.

Appendix A

RAII is Awesome

(a) ...

Figure A.1: ...

(b) ....

Figure A.1: each needs its main caption. ideally, it should be the same as above

$$\frac{52}{1x} \tag{A.1}$$

A.1 Hello

Appendix B

Equation example

Header	Header 2
Item 1	9.81
Item 2	42.00
Item 3	3.14

(a) ...caption...

Header	Header 2
Item 1	9.81
Item 2	42.00
Item 3	3.14

(b) ...caption...

Table B.1: Overall idea.

Example of an aligned equation (commented out in the source):