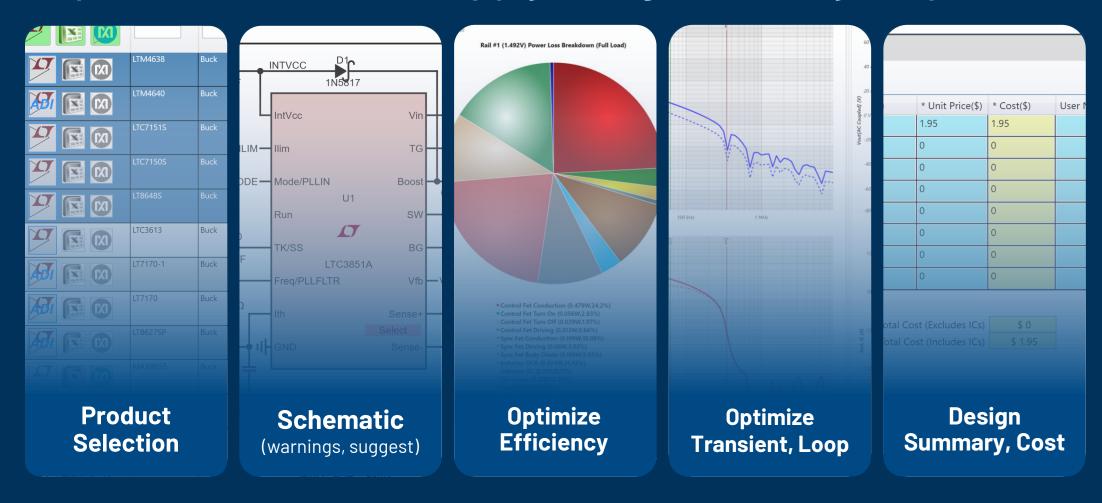




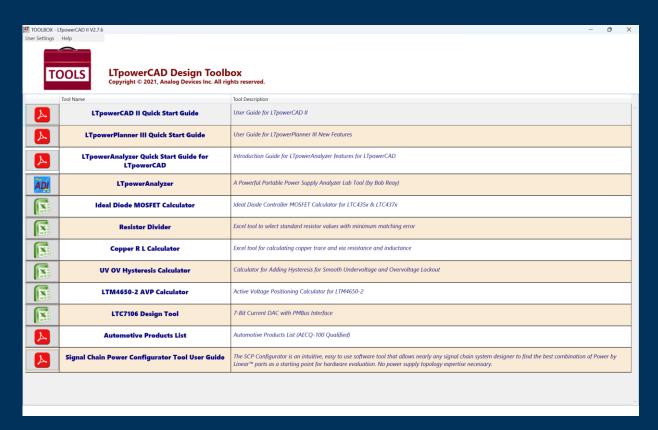
LTpowerCAD: Power Supply Design in 5 Easy Steps



Free download @ www.analog.com/LTpowerCAD



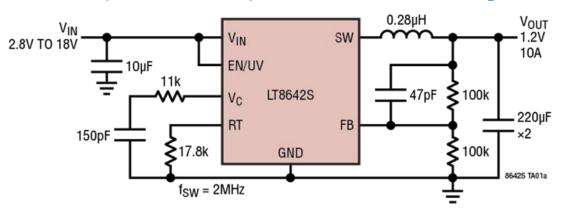
LTpowerCAD: Tools & Advanced Features



- Design Curves: how does the input voltage affect the operating point?
- EMI Filter Design: will your design pass common EMI certifications?
- Component Selection:
 - Browse from component library or add a new component
 - DC Bias derating
 - Effect of T_J in RDSON and DCR
- Auto-compensation
- Export/Print Plots

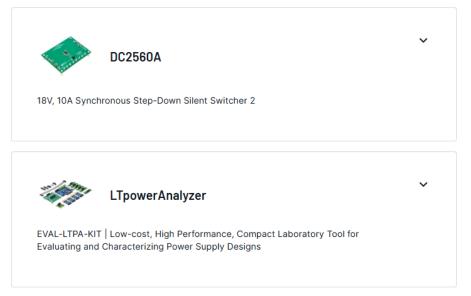


Example: Step-Down Design using LTpowerCAD



<u>DC2560A</u>: 18V, 10A Evaluation Kit featuring the <u>LT8642S</u> Silent Switcher 2 step down regulator

Evaluation Kits



Specification	Value	Units
V _{NOMINAL}	1.2	V
DC Setpoint (% of V_{NOM})	0.5	%
VR Ripple (% of V _{NOM})	1	%
AC Transient (% of V_{NOM})	2.5	%
MAX DC + AC (% of V_{NOM})	3.0	%
Step Load	5	А
Slew Rate	10	A/us

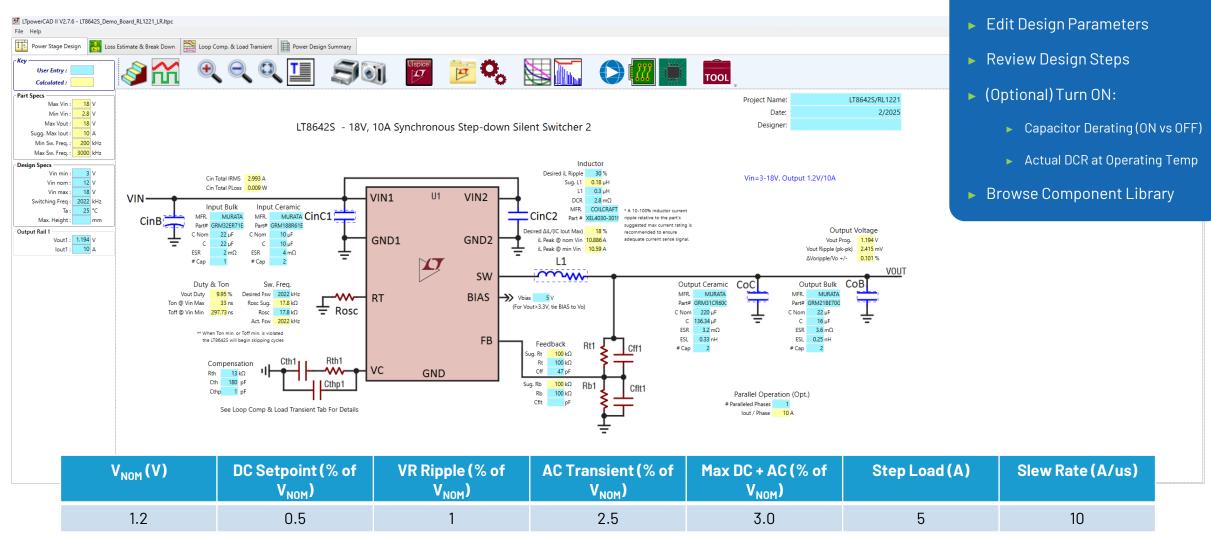


FPGA and Processors Compatible Reference Designs | Analog Devices

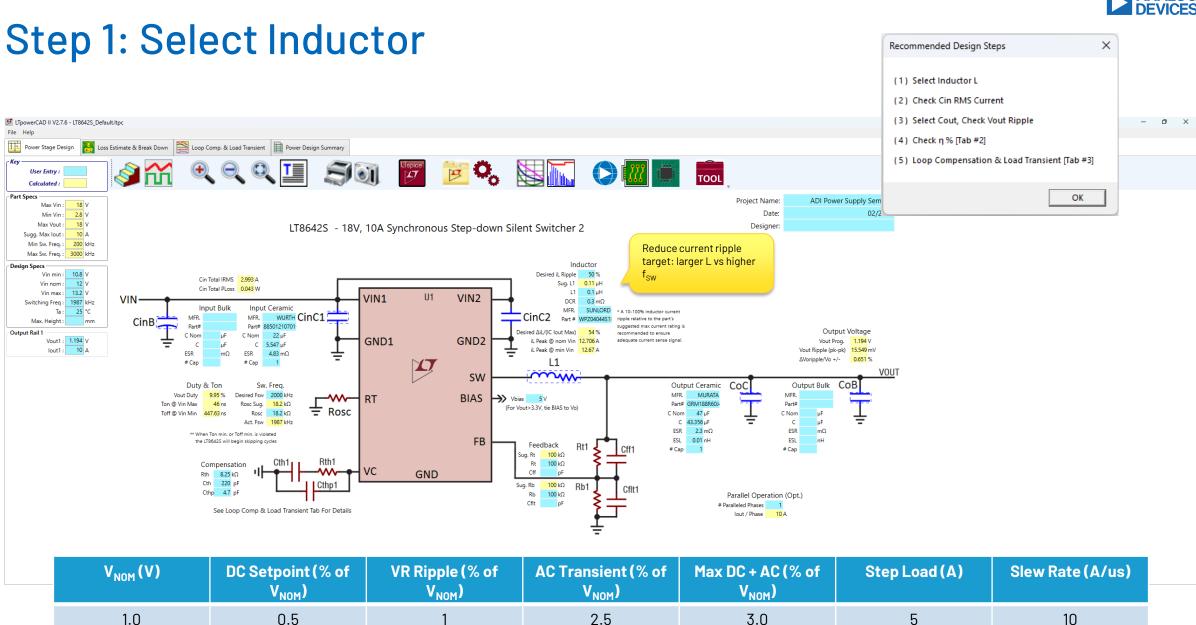


Power Stage Design Tab

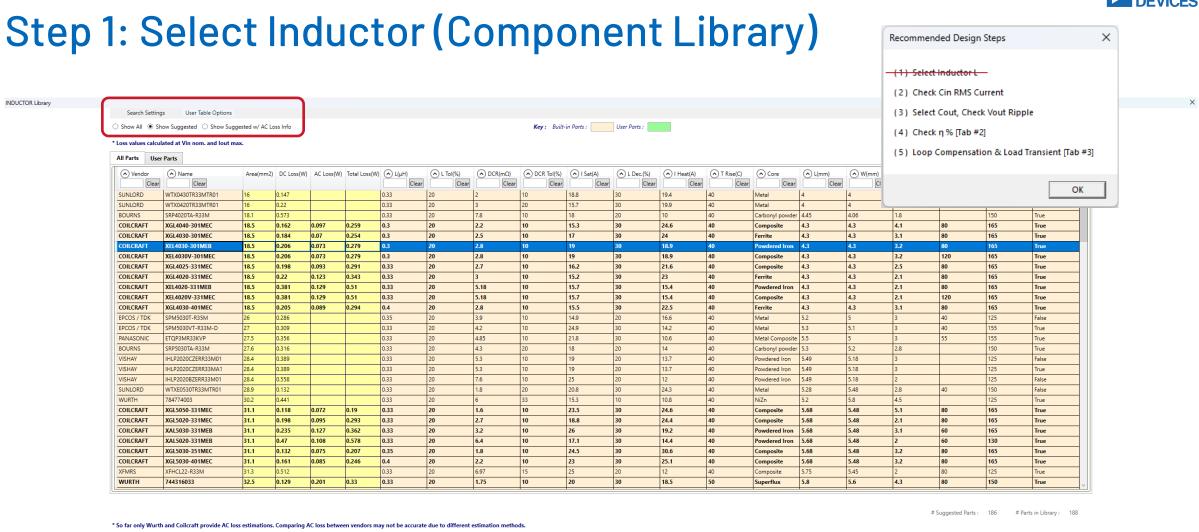
Schematics and Power Stage Design



















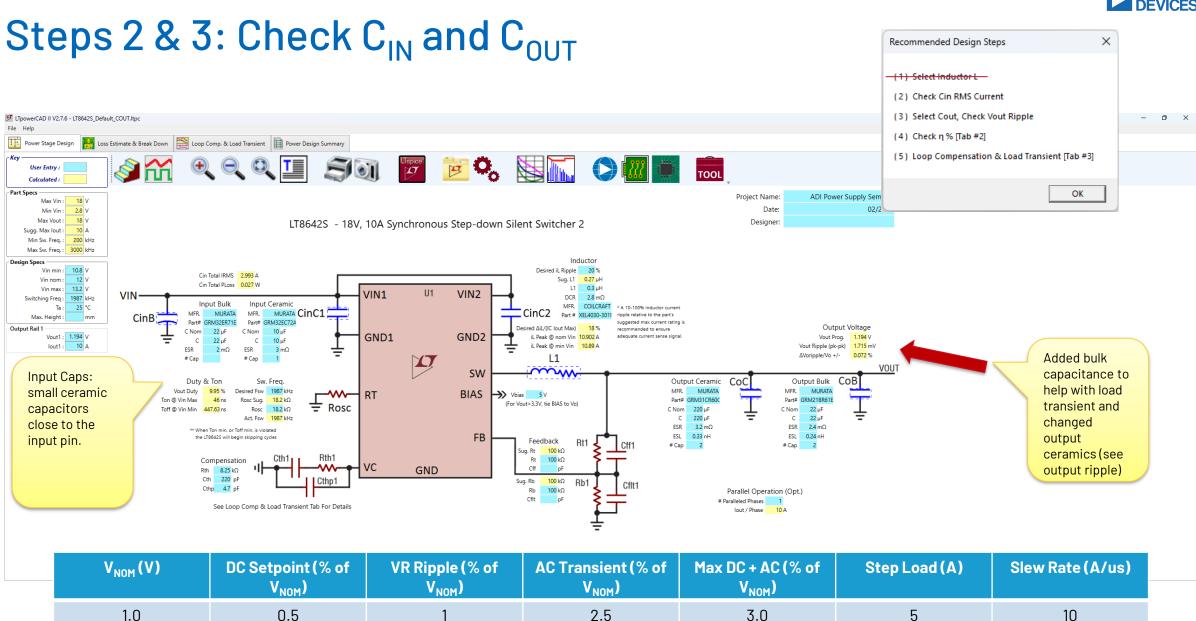






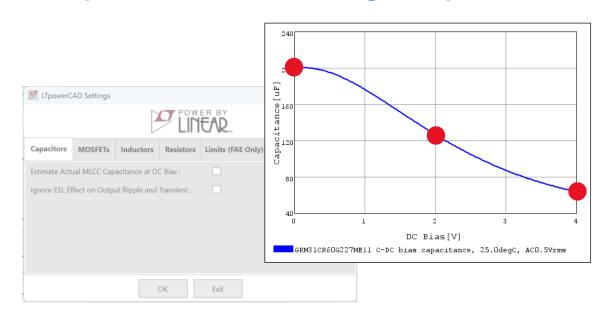








Capacitor Derating: Tips & Tricks

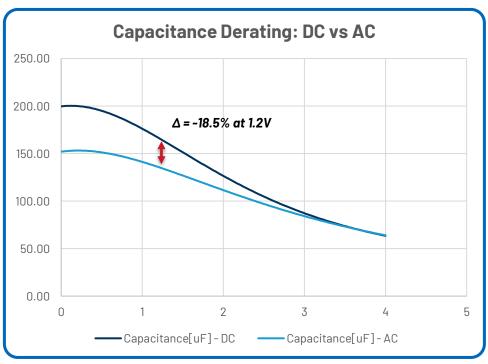


Part Number	C _{NOM} (uF)	LTpowerCAD Derating (uF)	C _{DC-BIAS} (uF)	C _{AC-BIAS} (uF)
GRM31CR60G227ME11	220	177.35	168.51	136.34
GRM21BD70J226ME44	22	21.125	20.65	16.58

^{*}LTpowerCAD uses a 3-point interpolation and does not derate capacitance based on AC voltage or temperature

Additional Information:

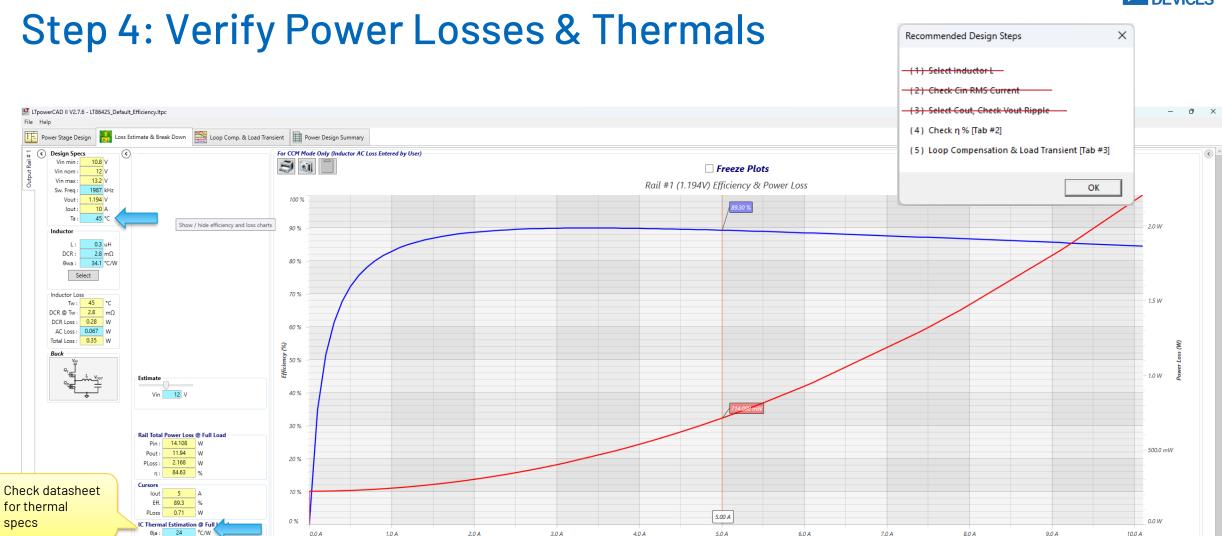
- Murata: The voltage characteristics of electrostatic capacitance | Murata Manufacturing Articles
- Kemet: Here's What Makes MLCC Dielectrics Different



Performance characteristic curves obtained from Murata's Simsurfing Tool.

Homework: compare LTpowerAnalyzer frequency response (or any frequency analyzer) of the LT8642S demo board with different LTpowerCAD derating models.





Load Current (A)

Export Import Clear Imported

(Tj-Ta): 43.051 °C

Tj: 88.051 °C



LT8642S: Design of Compensation Network

► High loop DC Gain (by default).

Target #1) Fast Transient Response. (High BW)

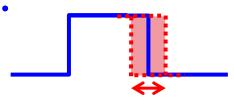
 \rightarrow Loop BW <= 1/5~ 1/10 f_{SW}

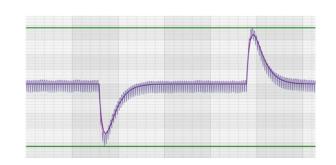
Target #2) Stability. (across operating range)

- → PM ≥45 degree. (≥60 degree preferred.)
- \rightarrow GM \geq 10dB

Target #3) Attenuate switching noises.







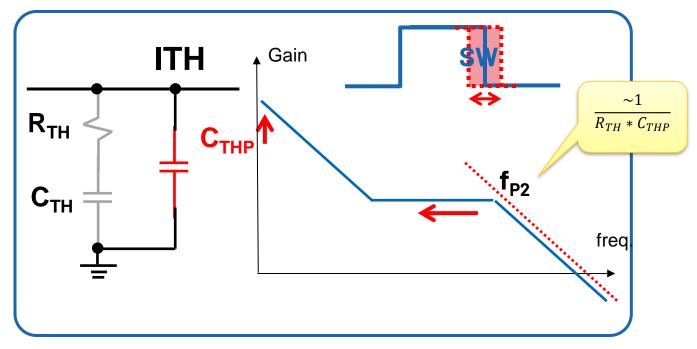
Component	Value	Units
R _{TH}	OPEN	kΩ
C_{TH}		pF
C_THP		pF
C _{FF}		pF

Proposed initial values for LT8642S example



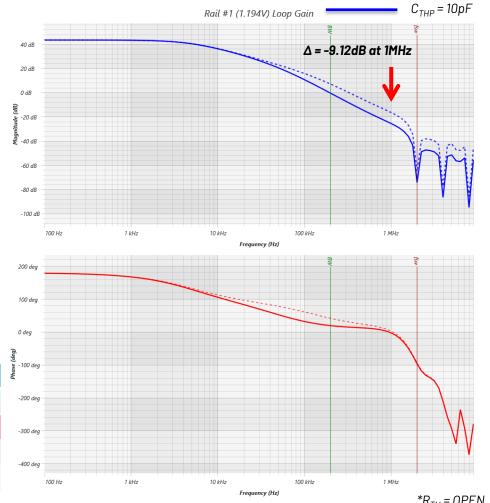
 $C_{THP} = OPEN$

Step 1: HF Gain Attenuation (C_{THP})



- Higher C_{THP} reduces HF gain, improve noise immunity
- f_{P2} moves to a lower frequency and will affect PM
- Slightly increase transient ΔV_{OUT}

Stability Metric	CTHP = OPEN	CTHP = 10pF
Bandwidth (kHz)	316.23	199.53
Phase Margin (Deg)	30.88	18.93
Gain @ fSW/2 (dB)	-16.21	-25.33
Gain Margin (dB)	-18.08	-25.33



 $*R_{TH} = OPEN$



 \square PM > 45°

GM > 10dB

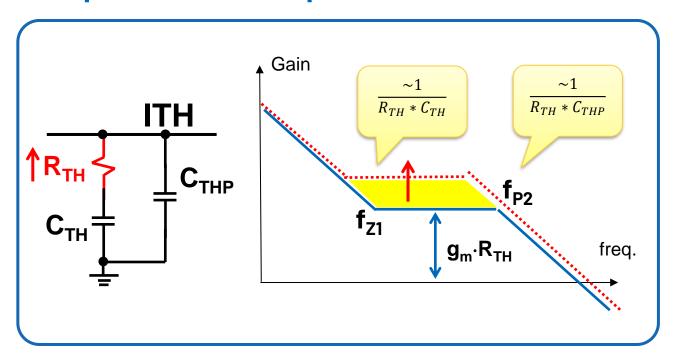
Loop BW: $1/10 \text{ to } 1/5 f_{SW}$

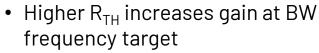


......

 $R_{TH} = 1k\Omega$

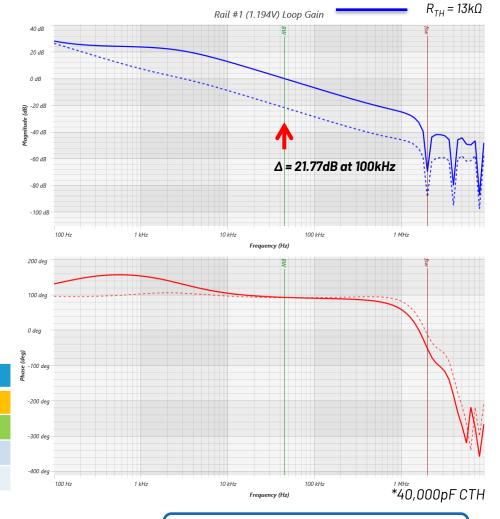
Step 2: Set Loop Gain & Load Transient





- Reduces ΔV_{OUT} during load transients
- Reduces phase margin

Stability Metric	R _{TH} = 1kΩ	R _{TH} = 13kΩ
Bandwidth (kHz)	3.16	44.67
Phase Margin (Deg)	104.84	93.03
Gain @ fSW/2(dB)	-45.71	-24.84
Gain Margin (dB)	-88.56	-39.31





■ GM > 10dB

☐ Loop BW: 1/10 to 1/5 f_{SW}

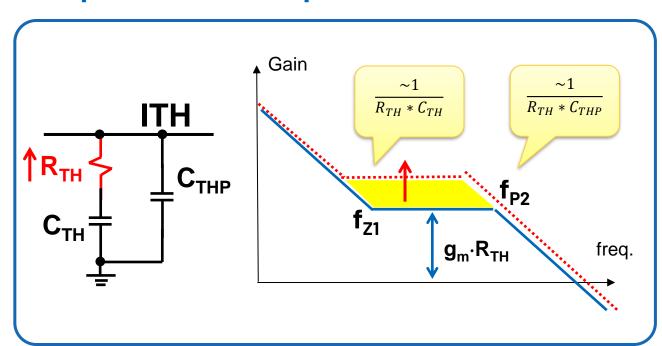
 $[\]Box$ Gain @ f_{SW}/2 < -8dB

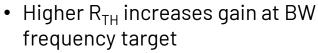


 $R_{TH} = 1k\Omega$

 $R_{TH} = 13k\Omega$

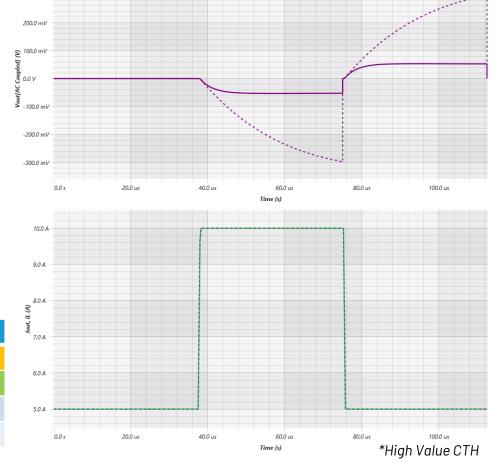
Step 2: Set Loop Gain & Load Transient (Cont.)





- Reduces ΔV_{OUT} during load transients
- Reduces phase margin

Stability Metric	R _{TH} = 1kΩ	R _{TH} = 13kΩ
Bandwidth (kHz)	3.16	44.67
Phase Margin (Deg)	104.84	93.03
Gain @ fSW/2 (dB)	-45.71	-24.84
Gain Margin (dB)	-88.56	-39.31



Rail #1 (1.194V) Load Transien



■ GM > 10dB

300.0 mV

☐ Loop BW: 1/10 to 1/5 f_{SW}

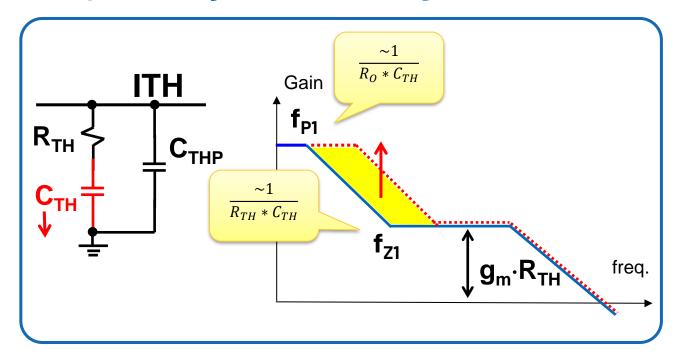
 $[\]Box$ Gain @ f_{SW}/2 < -8dB



 $C_{TH} = 180 pF$

 $C_{TH} = 470 pF$

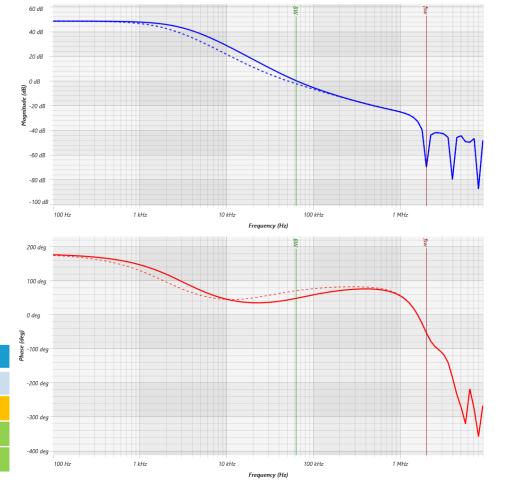
Step 3: Adjust Settling Time





- Make sure PM > 45°
- Keep f_{Z1} < BW

Stability Metric	C _{TH} = 470pF	C _{TH} = 180pF
Bandwidth (kHz)	50.12	63.1
Phase Margin (Deg)	67.09	48.52
Gain @ fSW/2 (dB)	-24.92	-25.03
Gain Margin (dB)	-39.37	-32.78



Rail #1 (1.194V) Loop Gain





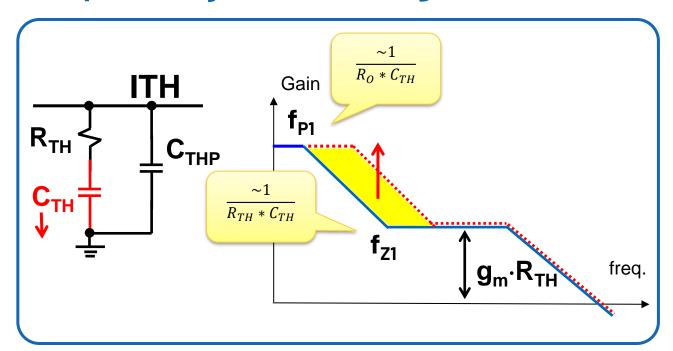
☐ GM > 10dB

■ Loop BW: 1/10 to 1/5 f_{SW}



 $C_{TH} = 470 pF$

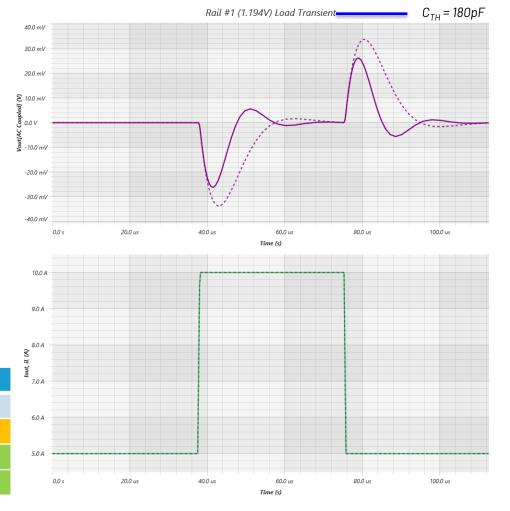
Step 3: Adjust Settling Time (Cont.)





- Make sure PM > 45°
- Keep f_{Z1} < BW

Stability Metric	C _{TH} = 470pF	C _{TH} = 180pF
Bandwidth (kHz)	50.12	63.1
Phase Margin (Deg)	67.09	48.52
Gain @ fSW/2(dB)	-24.92	-25.03
Gain Margin (dB)	-39.37	-32.78





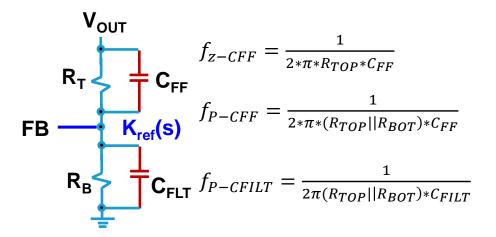


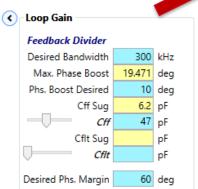
□ GM > 10dB

 \checkmark Loop BW: 1/10 to 1/5 f_{SW}



Step 4 (Opt.): FB Capacitors



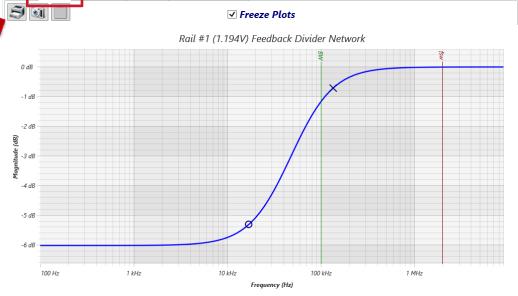


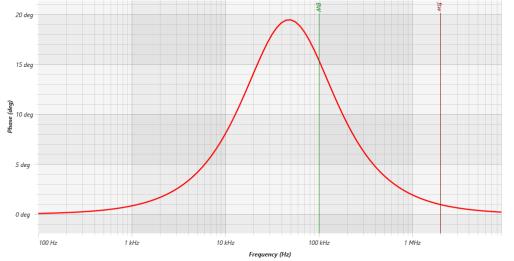
- Only add if necessary to provide additional BW and PM
 - Set phase boost peak f_{BST} around f_{BW}
 - Recommended: leave C_{ff} footprints on PCB

Stability Metric	C _{FF} = OPEN	C _{FF} = 47pF
Bandwidth (kHz)	63.1	100
Phase Margin (Deg)	48.52	74.26
Gain @ fSW/2(dB)	-25.03	-19.03
Gain Margin (dB)	-32.78	-33.45







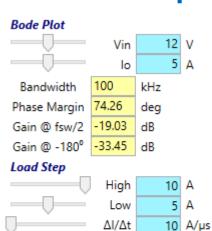








Final Step: Confirm Design Targets



ΔVo Target & Response

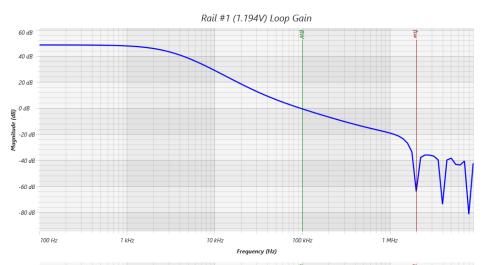
Target Total Δ Vo \pm 3 %

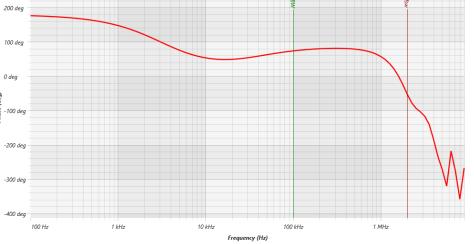
Target Δ VoRipple \pm 1 % Δ VoRipple \pm 0.28 %

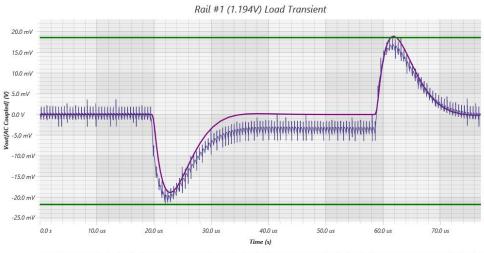
Allowed Δ VoStep \pm 2.72 % Δ VoStep \pm 1.82 %

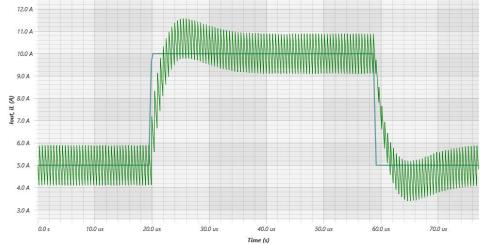
Total Δ Vo \pm 2.1 %

Component	Value	Units
R _{TH}	13	kΩ
C _{TH}	180	pF
C _{THP}	1	pF
C_{FF}	47	pF











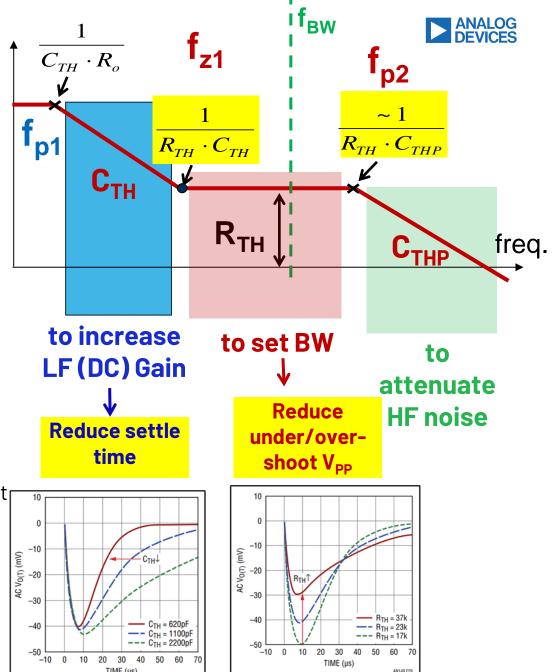




■ Loop BW: 1/10 to 1/5 f_{SW}

Summary of Compensation Design

- 1. Set Bandwidth and Transient Response
 - 1. Adjust RTH (higher RTH increases BW, decreases PM)
 - 2. Check for transient response target
- 2. Set Settling Time
 - Adjust CTH (lower CTH reduces settling time at the expense of PM)
- 3. Check for HF Attenuation
 - Adjust CTHP (higher CTHP improves noise immunity at the expense of BW)
- 4. Optional: Feedforward Capacitor
 - Check if phase boost is needed by looking at the PM and transient response
- 5. Close the loop (pun intended)
 - 1. Confirm design targets

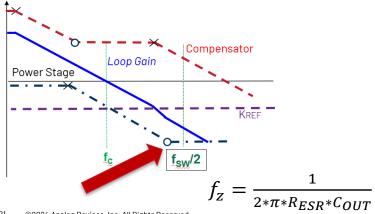




Final Thoughts & Questions

Component / Spec	Tolerance	Min	Normal	Max	Units
Inductor	20%	240	300	360	nH
VOUT Ripple		3.018	2.415	2.012	. mV
Bandwidth			12.20%		%
Phase Margin			4.77%		%
COUT	20%	240	304.68	366	uF
Bandwidth			36.77		%
COUT ESR		±2		mΩ	
Phase Margin		23.52		%	
	LTPowerCAI	D vs LTspice			
Bandwidth		2.02		%	
Phase Margin		7.82		%	
	LTPowerCAD vs L	.TPowerAnalyz	zer		
Bandwidth		6.25		%	
Phase Margin			24.71		%

LTPowerCAD vs LTspice vs LTPowerAnalyzer results comparison



Final Thoughts

- Ideal BW range is lower on high FSW designs
- Simulation model accuracy depends on "precise" passive models
 - Board parasitics play a role on BW & PM
- LTspice and additional simulation capabilities:
 - Second stage filter & split rails
 - Up/downstream converters