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18-240

27 January 2023

Lab 0

1. True. Laptops do not have the software needed, but using ssh, students can remotely use Linux machines that do have the proper software installed.
2. False. When using the Linux machines in the lab, the needed software is installed, and ssh'ing would add unneeded complexity.
3. X11 forwarding allows for graphical output from the remote computer's programs, allowing software dependent on a GUI to be used. SSH allows for accessing the command line.
4. You need to state the default nettype. This prevents VCS from not raising errors when you make a typo and don't name a variable properly.
5. Module instantiation creates a specific module that has been defined, and does not need to be in initial blocks. Function calls can only be used in initial blocks, and have outputs and inputs like a more traditional software language.
6. The logic keyword means that a value will have one of 7 values, most importantly 0 and 1. They are used to instantiate wires.
7. It will run both initial points. If both have a finish, whichever it reaches first will end the simulation.
8. The top module is the module declared that will contain all the other modules. It has no inputs or outputs, since it is the highest module and has nothing else to interact with.

9. It causes the code to not compile. This is because although execution is simultaneous, the declaration of variables is separate from this.
10. The waveform allows visualization of all the changes in inputs, and how they relate to each other. One might use it if they need a more general view of how the circuit is behaving.
11. They are generated in the muxTester module.
12. They are generated by the multiplexer itself.
13. Simulation means using software to predict how a circuit will behave. Synthesis means programming an actual gate array to run the circuit, providing a more concrete test of the system.
14. It is used to connect the pins defined in the systemVerilog code to actual real world connections in the DE2 115.
15. You know you will have successfully imported them if the pin planner shows some pins as red dots. If you don't successfully import pins, there won't be errors, but there will be critical warnings. Quartus will choose random pins to assign, which won't be a great idea.
16. If they don't match, Quartus won't know how to synthesize your code or where to start. It will return an error and won't finish.
17. It will cause errors and won't finish, because the monitor and other features aren't actually gates, and Quartus has no way to properly synthesize this.
18. SystemVerilog_CodingStandards.pdf
19. init_handin240

20. ECE servers are the only computers that have access to the script, and you must be in the same directory as the code.