Hardware Implementation of a Multi-Layer Perceptron Neural Network

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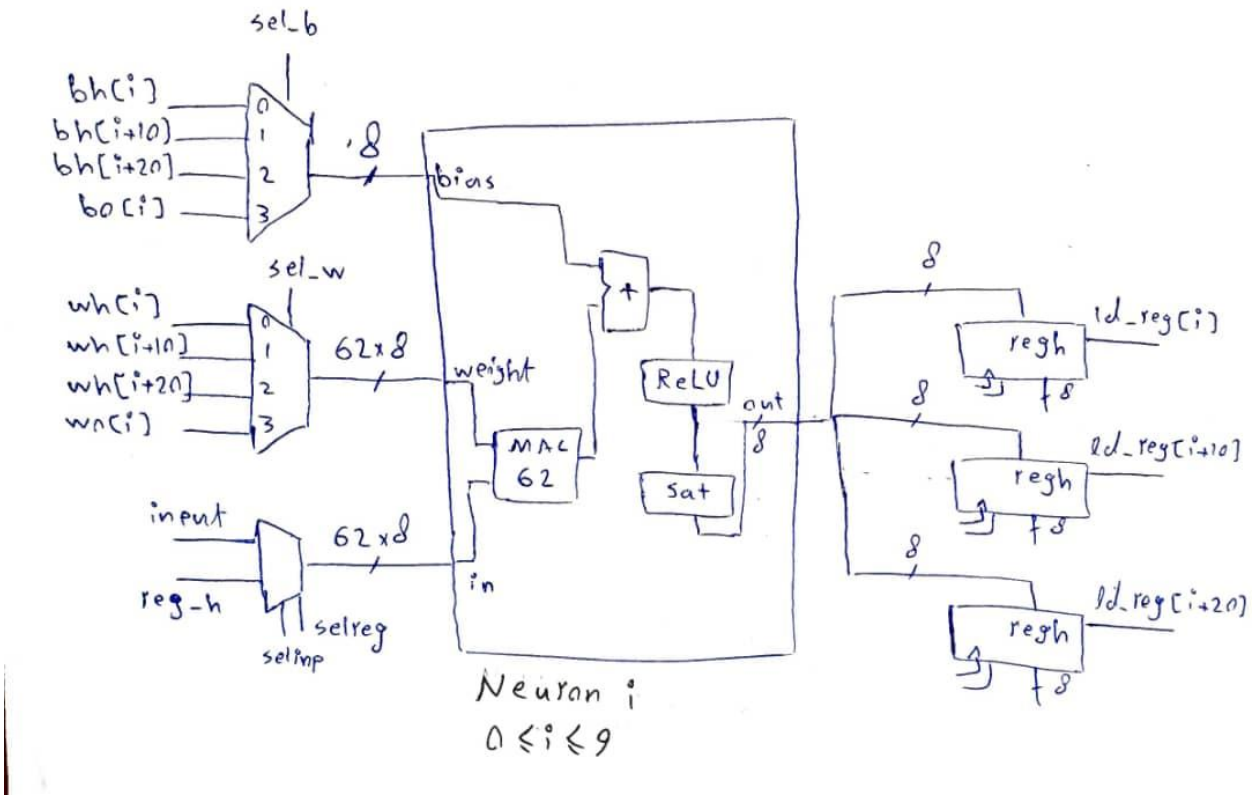
Datapath:



Mulxtiplexers:

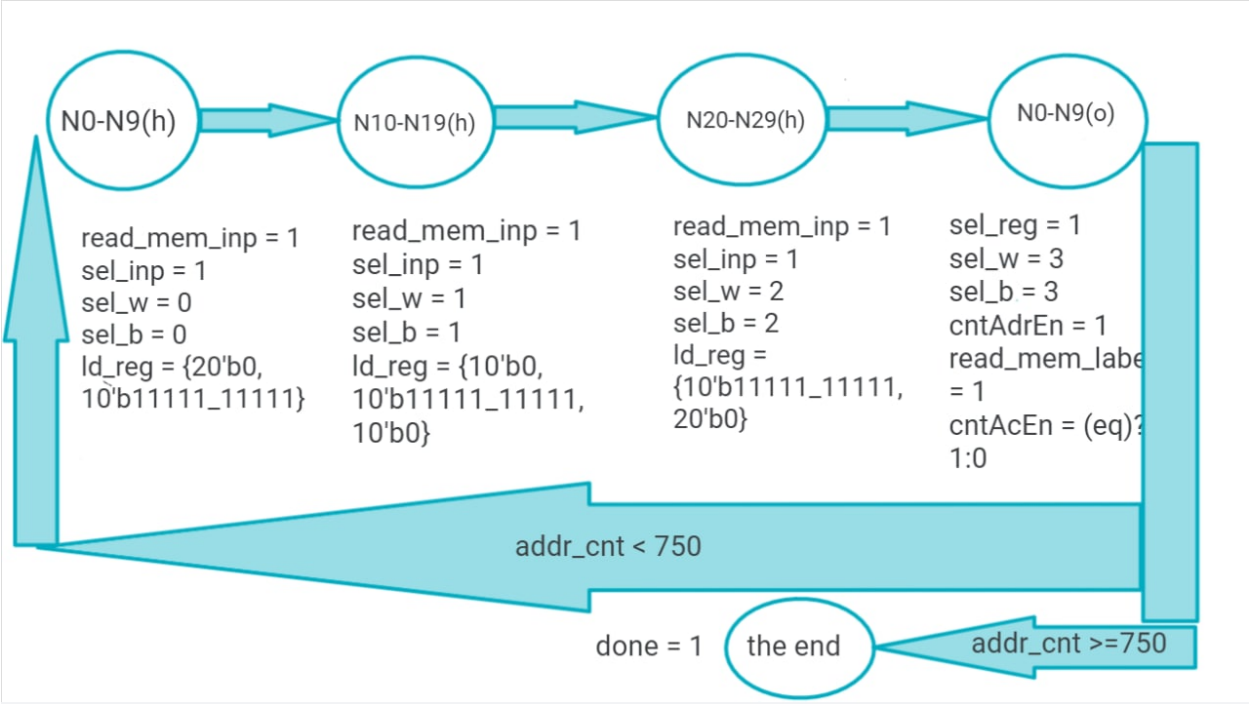
1. **Bias**: Selecting appropriate bias values based on the controller's state. They can be either hidden layer biases or output layer biases.
2. **Weight**: Selecting appropriate weight values based on the controller’s state

3. **Input:** Selecting appropriate values to multiply by weights. They can be either inputs of the FNN or the output of hidden layers coming from registers.

Registers:

Used to store the calculation result of hidden layers

Controller:

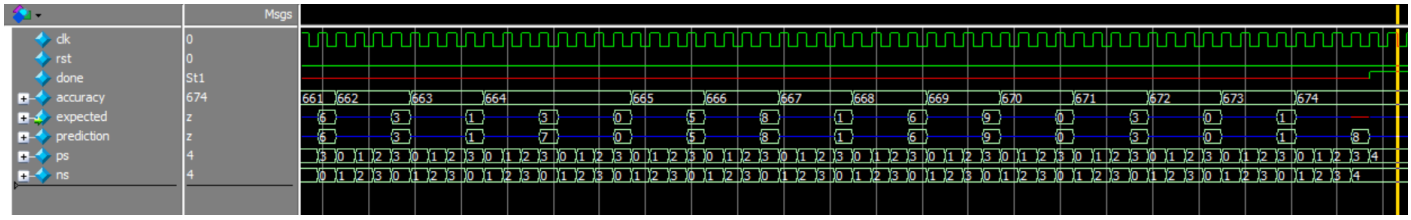


1. **State 0**: Neurons 0-9 of the hidden layer operate. The inputs of the neurons should be selected from the input memory. Weights and Biases associated with Neurons 0-9 are selected by issuing *sel_inp, sel_w, sel_b* to appropriate values. The results are stored in registers 0-9.
2. **State 1**: Neurons 10-19 of the hidden layer operate. The inputs of the neurons should be selected from the input memory. Weights and Biases associated with Neurons 10-19 are selected by issuing *sel_inp, sel_w, sel_b* to appropriate values. The results are stored in registers 10-19.
3. **State 2**: Neurons 20-29 of the hidden layer operate. The inputs of the neurons should be selected from the input memory. Weights and Biases

associated with Neurons 20-29 are selected by issuing *sel_inp, sel_w, sel_b* to appropriate values. The results are stored in registers 20-29.

4. **State 3:** Neurons 0-9 of the output layer operate. The inputs of the neurons should be selected from the register holding the results of the hidden layer calculations. Weights and Biases associated with the output layer are selected by issuing *sel_inp, sel_w, sel_b* to appropriate values.
5. **State 4:** This is the final state. When all the inputs are feeded to the network (*addr_cnt* reaches 750) we move to this state from State 3 and set the signal *done* to high.

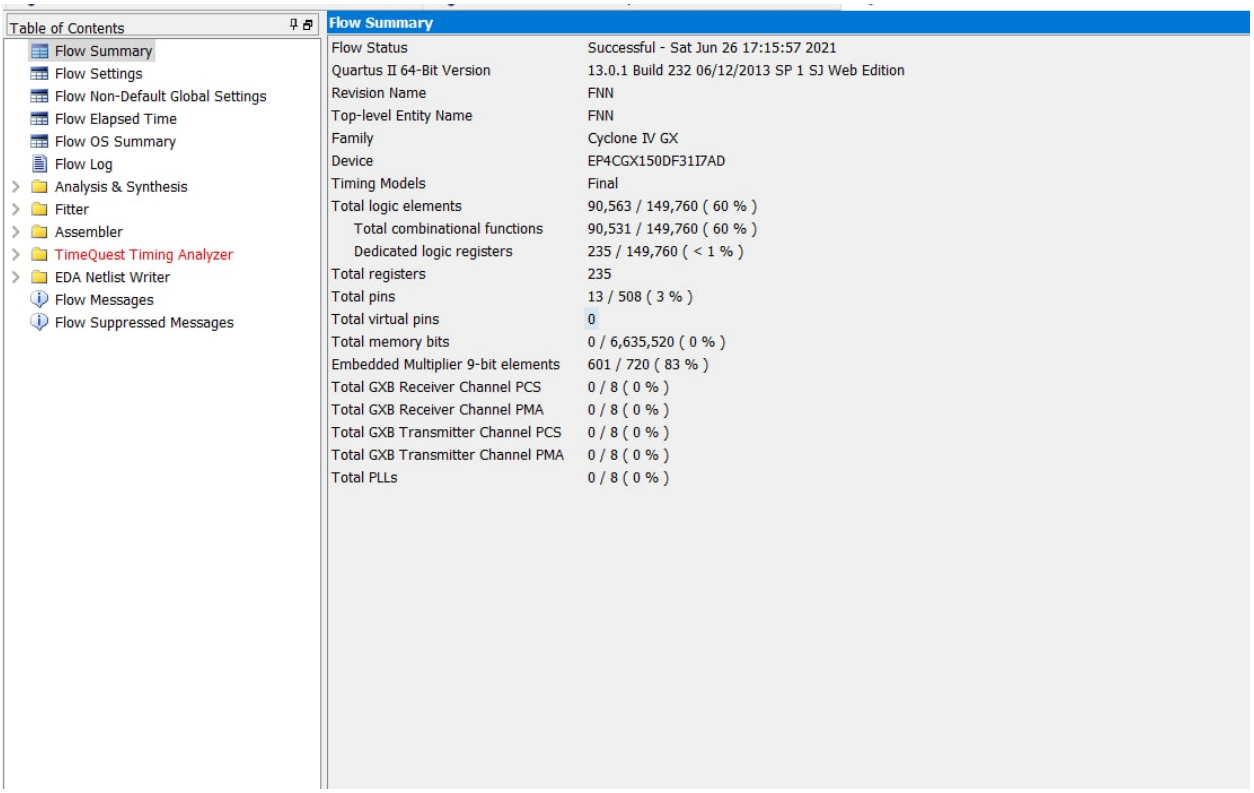
Simulation Results:



The signal named *accuracy* corresponds to the number of correct predictions.

$$Accuracy = \frac{correct}{total} = \frac{674}{750} = 89.86\%$$

Synthesis Results:



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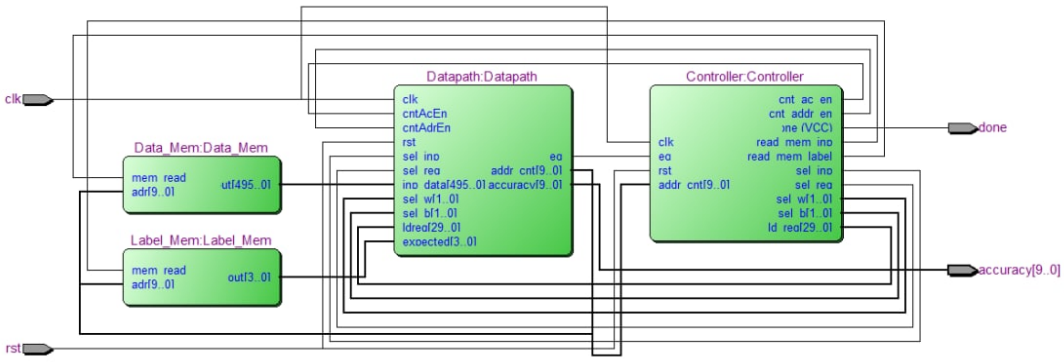
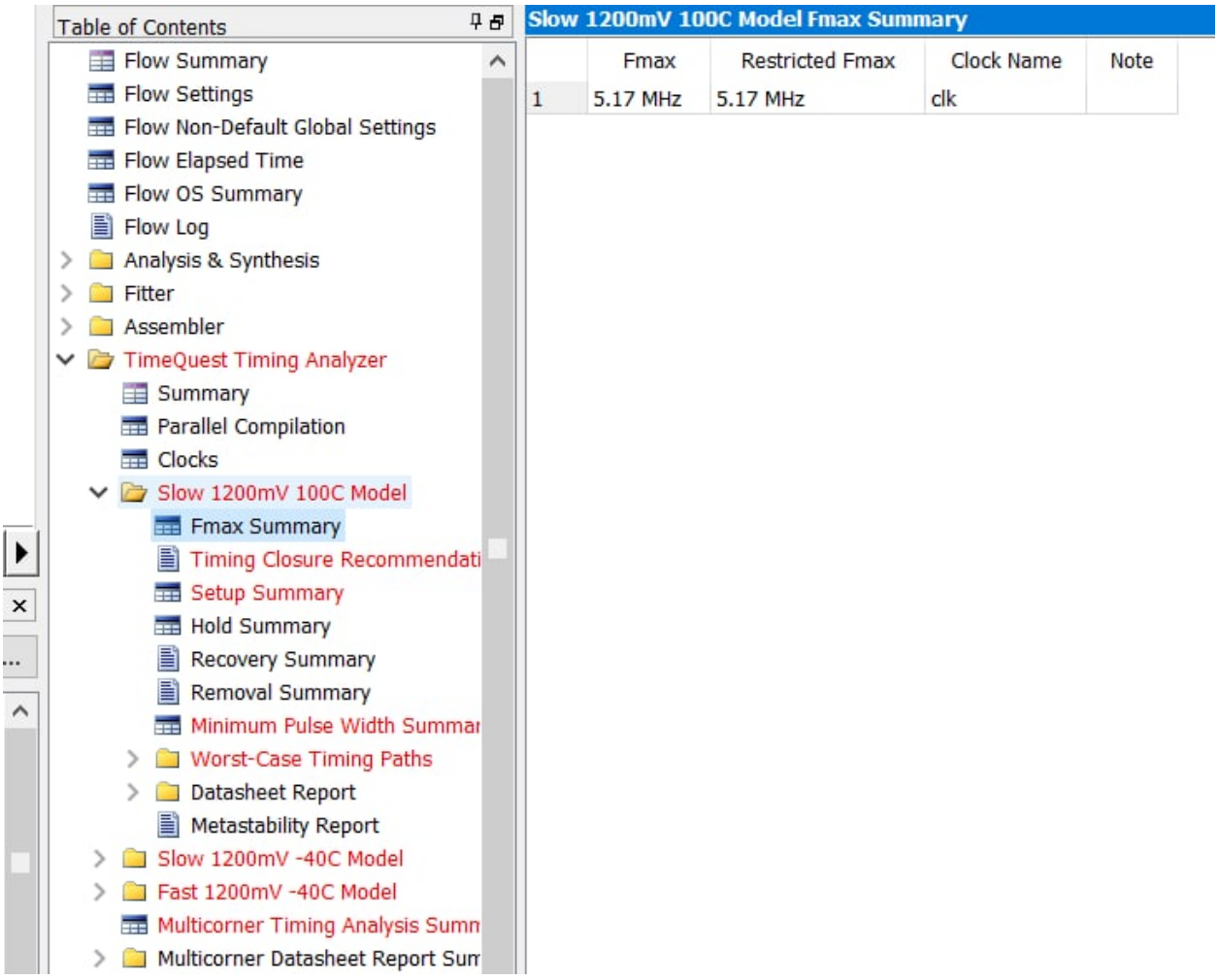
Flow Summary

Flow Status	Successful - Sat Jun 26 17:15:57 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	FNN
Top-level Entity Name	FNN
Family	Cyclone IV GX
Device	EP4CGX150DF31I7AD
Timing Models	Final
Total logic elements	90,563 / 149,760 (60 %)
Total combinational functions	90,531 / 149,760 (60 %)
Dedicated logic registers	235 / 149,760 (< 1 %)
Total registers	235
Total pins	13 / 508 (3 %)
Total virtual pins	0
Total memory bits	0 / 6,635,520 (0 %)
Embedded Multiplier 9-bit elements	601 / 720 (83 %)
Total GXB Receiver Channel PCS	0 / 8 (0 %)
Total GXB Receiver Channel PMA	0 / 8 (0 %)
Total GXB Transmitter Channel PCS	0 / 8 (0 %)
Total GXB Transmitter Channel PMA	0 / 8 (0 %)
Total PLLs	0 / 8 (0 %)

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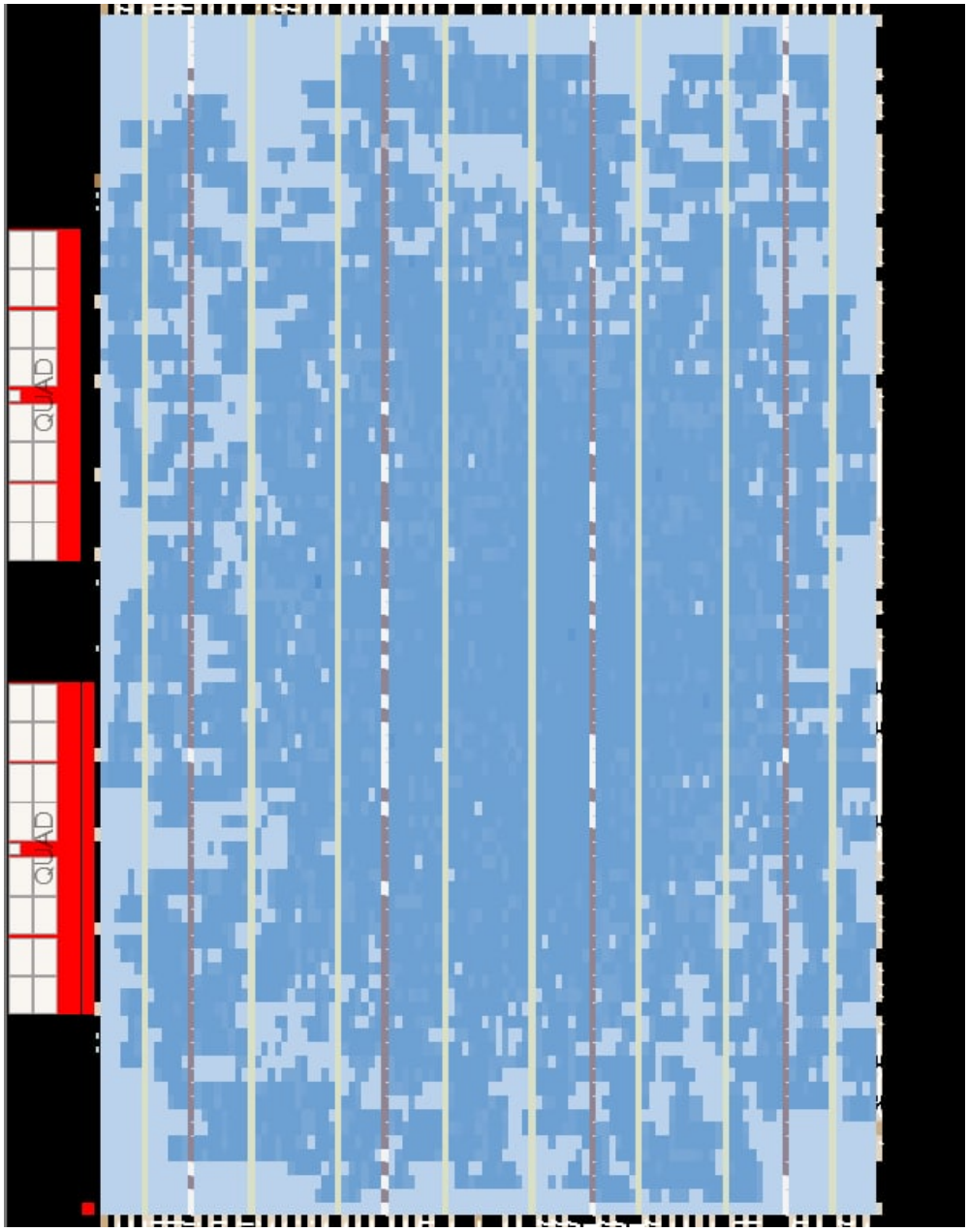
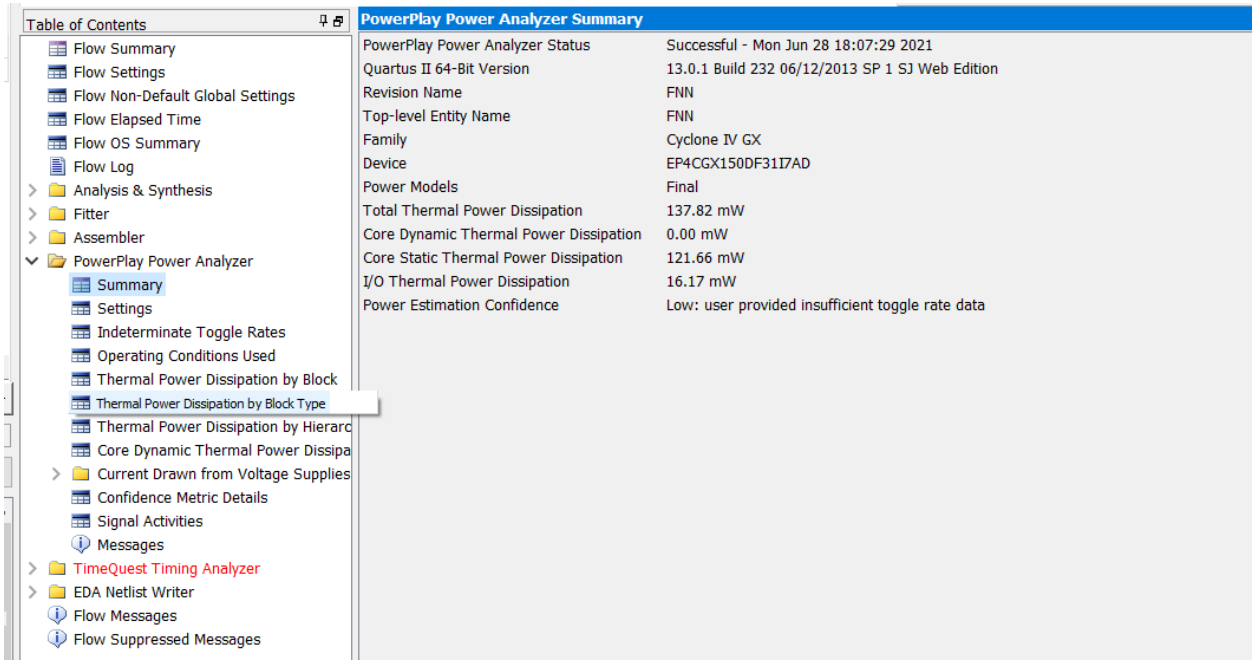
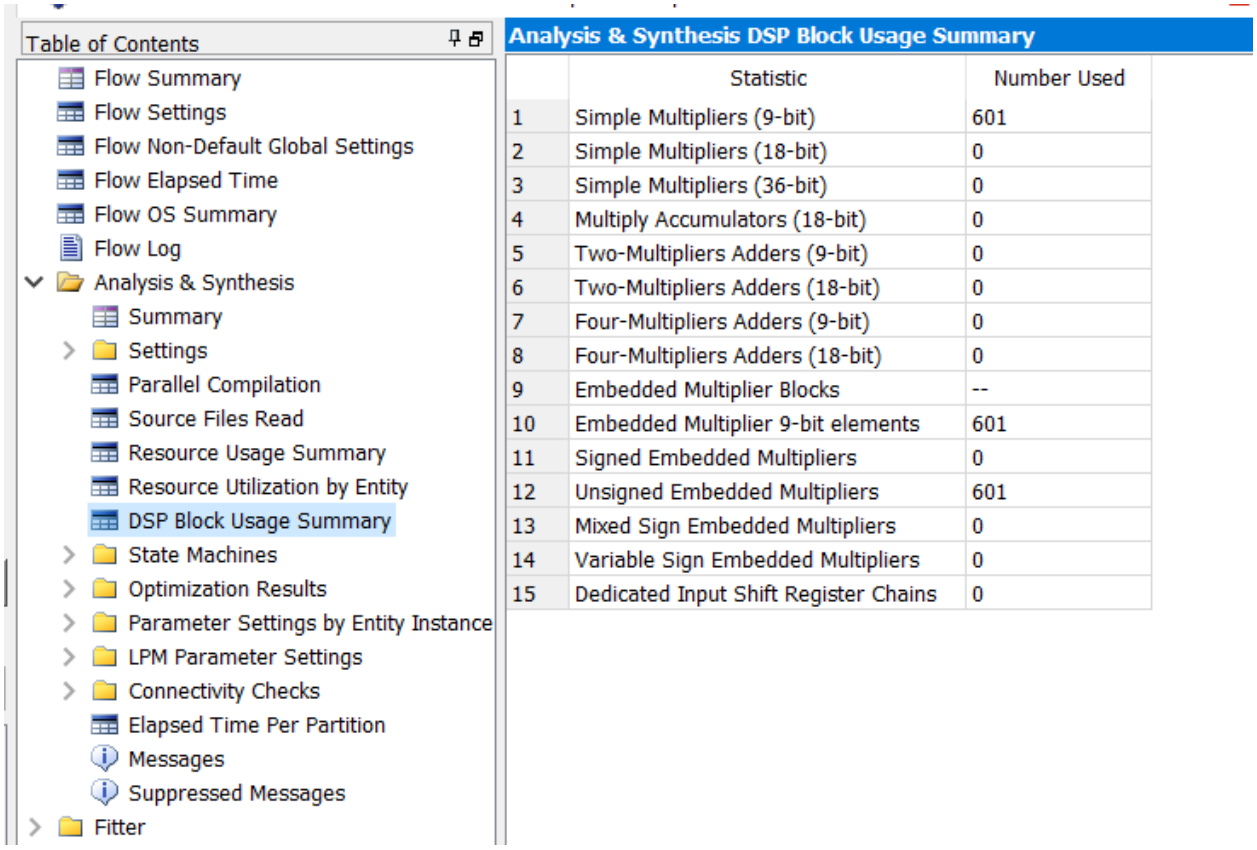
Datasheet Report
Metastability Report
Slow 1200mV -40C Model
Fast 1200mV -40C Model
Multicorner Timing Analysis Summ
Multicorner Datasheet Report Sum
Slow 1200mV 100C Model Fmax Summary
Fmax
Restricted Fmax
Clock Name
Note
1
5.17 MHz
5.17 MHz
clk



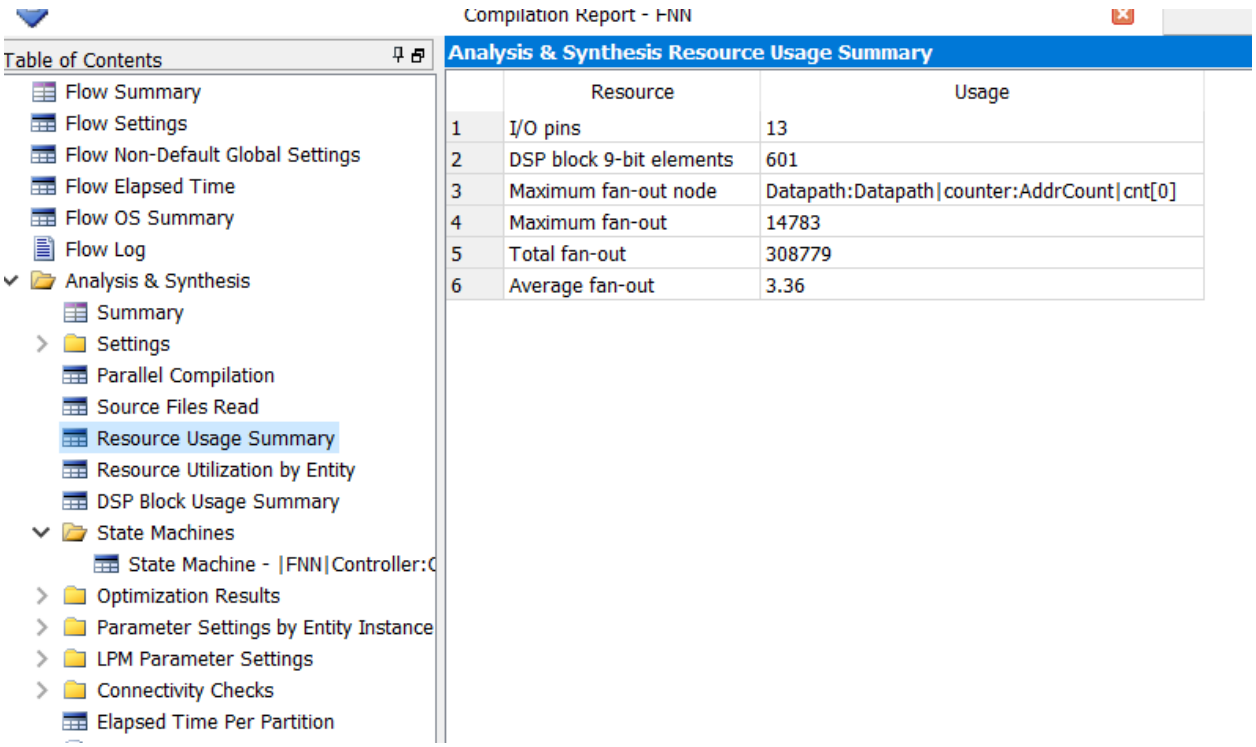
Chip Planner

Power Consumption:





	Statistic	Number Used
1	Simple Multipliers (9-bit)	601
2	Simple Multipliers (18-bit)	0
3	Simple Multipliers (36-bit)	0
4	Multiply Accumulators (18-bit)	0
5	Two-Multipliers Adders (9-bit)	0
6	Two-Multipliers Adders (18-bit)	0
7	Four-Multipliers Adders (9-bit)	0
8	Four-Multipliers Adders (18-bit)	0
9	Embedded Multiplier Blocks	--
10	Embedded Multiplier 9-bit elements	601
11	Signed Embedded Multipliers	0
12	Unsigned Embedded Multipliers	601
13	Mixed Sign Embedded Multipliers	0
14	Variable Sign Embedded Multipliers	0
15	Dedicated Input Shift Register Chains	0



	Resource	Usage
1	I/O pins	13
2	DSP block 9-bit elements	601
3	Maximum fan-out node	Datapath:Datapath|counter:AddrCount|cnt[0]
4	Maximum fan-out	14783
5	Total fan-out	308779
6	Average fan-out	3.36