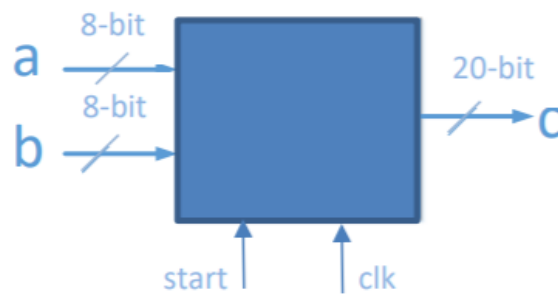# Computer Assignment #3

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MAC:

Input: (x[0], x[1], x[2], x[3]), (y[0], y[1], y[2], y[3]) where x[i] and y[i] are complex numbers each represented by 8 bits:

$$x[i][3:0]: \text{Imaginary Part}$$
$$x[i][7:0]: \text{Real Part}$$

Output: x[0]y[0] + x[1]y[1] + x[2]y[2] + x[3]y[3]

The complete Dapath and Controller is represented in the uploaded file named *design-810197(491-685).pdf*

Here we just show to the correctness of the simulation results:
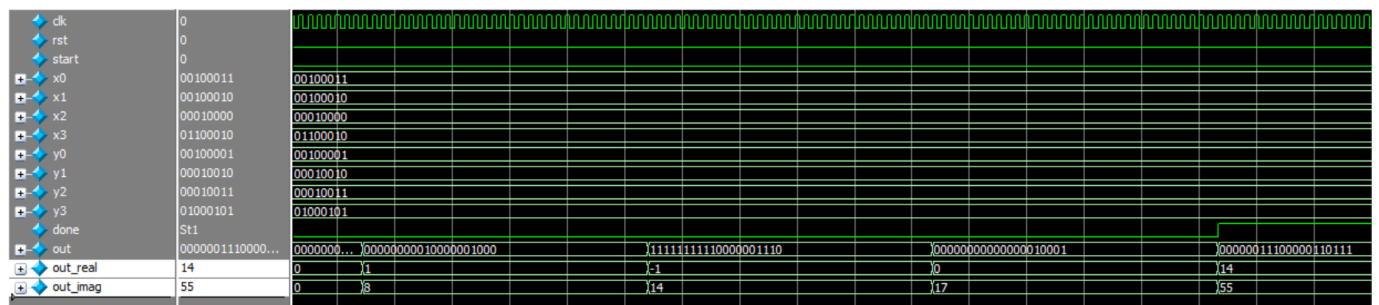
Test Bench:

```
MAC mut(clk, rst, x0, x1, x2, x3, y0, y1, y2, y3, out, out_real, out_imag,
done, start);
    always begin
        #8; clk = ~clk;
    end
        //(a, b) * (c, d) = (a + bj)(c + dj) += (ac - bd, ad + bc)
        //(2, 3) * (2, 1) = (1, 8)
        //(2, 2) * (1, 2) = (-2, 6)
        //(1, 0) * (1, 3) = (1, 3)
        //(6, 2) * (4, 5) = (14, 38)
        //---------------------------+
        //                   (14, 55)

    initial begin
        x0 = {4'd2, 4'd3}; y0 = {4'd2, 4'd1};
        x1 = {4'd2, 4'd2}; y1 = {4'd1, 4'd2};
        x2 = {4'd1, 4'd0}; y2 = {4'd1, 4'd3};
        x3 = {4'd6, 4'd2}; y3 = {4'd4, 4'd5};
        rst = 1; #25; rst = 0; start = 1; #18 start = 0;
        #2500
        $stop;
    end
```
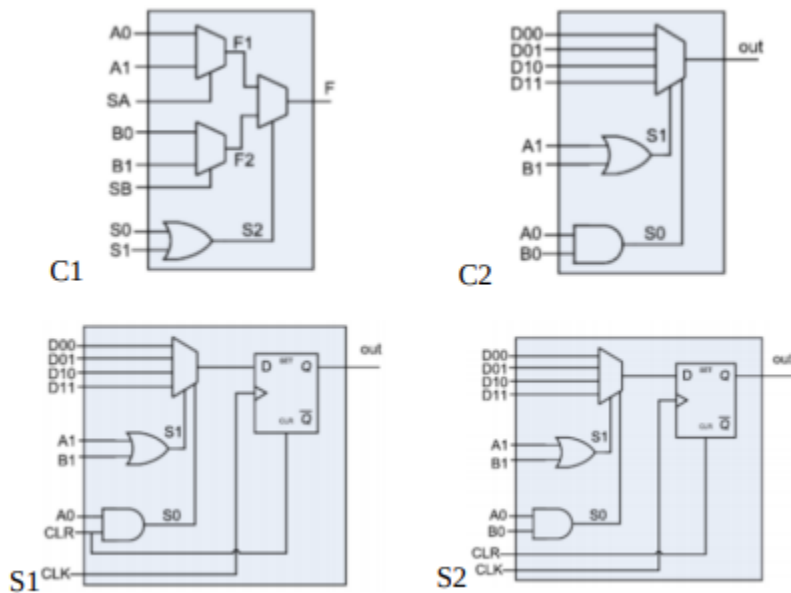
Simulation:

 As it can be seen, when *done* is set to high the output is showing the correct result
which is $14 + 55j$.

Logic Cells Used:

All components are implemented using the following logic units.

Module	C1	C2	S1	S2
Area	7	8	15	15

Total Area in each module:

Module Name	Total area
Real 2x2 Multiplier	45
Real 4x4 Multiplier	647
Complex 4x4 Multiplier	1659
Mac	3694