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EECE 573
Digital System Design II
Final Project

Synthesized Design Primitives Analysis

FSM Encoding	LUT6	LUT5	LUT4	LUT3	LUT2	LUTs Used	Total Size (LUT2 equivalent)
Off (use original module)	2	0	0	1	2	5	36
One Hot	0	6	2	0	0	8	56
Sequential	3	0	0	1	1	5	51
Johnson	3	0	0	2	0	5	52
Gray	3	0	0	1	1	5	51
Auto	3	0	0	1	1	5	51

Out of the 6 state encodings used during synthesis, “One Hot” coding provided the largest LUT area. This can most likely be attributed to the fact that one hot requires a bit for each state within the FSM, which (in certain cases) can lead to more complex combinational logic.

The original FSM encoding provided the smallest LUT area which means that the method used to select the state values provided a significant benefit compared to standardized encodings. The values 000, 010, 011, 100, 110, 101 (or 0, 2, 3, 4, 6, 7 in hex/decimal) were used because the combinational logic for the output values would only have to take into account the 2 most significant bits. The first bit signifies an “A” or “B” state and the second bit signifies if there should be an output value of “1”. This custom encoding shows to have helped minimize the complexity of the combinational logic by having a significantly smaller LUT size than the other encodings.

Shown below is the timing report for the original state encoding using a clock period of 1.065 ns or an 939.0 MHz clock. It shows the slack as 0.000ns and says that the timing requirement is still met so this is the minimum clock frequency that can be used for this module. However, this is not an advisable design choice because any slight change in timing due to external reasons (clock jitter, FPGA temperature change, V_{dd} variations) could cause timing issues. Increasing the clock period to a slightly higher value, like 1.25ns, would greatly reduce if not eliminate the possibility for external factors to create timing issues within the FPGA.

Timing report with 1.065ns period clock:

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Timing Report

Slack (MET) :             0.000ns  (required time - arrival time)
  Source:                 state_reg[1]/C
                            (rising edge-triggered cell FDRE clocked by clk  {rise@0.000ns fall@0.500ns period=1.065ns})
  Destination:            state_reg[2]/D
                            (rising edge-triggered cell FDRE clocked by clk  {rise@0.000ns fall@0.500ns period=1.065ns})
  Path Group:             clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            1.065ns  (clk rise@1.065ns - clk rise@0.000ns)
  Data Path Delay:        1.037ns  (logic 0.580ns (55.923%)  route 0.457ns (44.077%))
  Logic Levels:           1  (LUT6=1)
  Clock Path Skew:        -0.022ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.284ns = ( 5.349 - 1.065 )
    Source Clock Delay      (SCD):    4.645ns
    Clock Pessimism Removal (CPR):    0.339ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock clk rise edge)        0.000     0.000 r
    M18                                               0.000     0.000 r  clk (IN)
                         net (fo=0)                   0.000     0.000    clk
    M18                  IBUF (Prop_ibuf_I_O)         0.938     0.938 r  clk_IBUF_inst/O
                         net (fo=1, routed)           1.972     2.910    clk_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.096     3.006 r  clk_IBUF_BUFG_inst/O
                         net (fo=3, routed)           1.639     4.645    clk_IBUF_BUFG
    SLICE_X0Y2           FDRE                                       r  state_reg[1]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X0Y2           FDRE (Prop_fdre_C_Q)         0.456     5.101 r  state_reg[1]/Q
                         net (fo=4, routed)           0.457     5.558    p_0_in
    SLICE_X1Y2           LUT6 (Prop_lut6_I3_O)        0.124     5.682 r  state[2]_i_1/O
                         net (fo=1, routed)           0.000     5.682    state[2]_i_1_n_0
    SLICE_X1Y2           FDRE                                       r  state_reg[2]/D
  -------------------------------------------------------------------    -------------------

                         (clock clk rise edge)        1.065     1.065 r
    M18                                               0.000     1.065 r  clk (IN)
                         net (fo=0)                   0.000     1.065    clk
    M18                  IBUF (Prop_ibuf_I_O)         0.805     1.870 r  clk_IBUF_inst/O
                         net (fo=1, routed)           1.868     3.738    clk_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.091     3.829 r  clk_IBUF_BUFG_inst/O
                         net (fo=3, routed)           1.520     5.349    clk_IBUF_BUFG
    SLICE_X1Y2           FDRE                                       r  state_reg[2]/C
                         clock pessimism              0.339     5.688
                         clock uncertainty           -0.035     5.653
    SLICE_X1Y2           FDRE (Setup_fdre_C_D)        0.029     5.682    state_reg[2]
  -------------------------------------------------------------------
                         required time                          5.682
                         arrival time                          -5.682
  -------------------------------------------------------------------
                         slack                                  0.000
```