

Thread Scheduler Efficiency Improvements for Multiprocessor Multicore Non-Uniform Memory Access Systems

Daniel C. Frazier
Division of Science and Mathematics
University of Minnesota, Morris
Morris, Minnesota, USA 56267
frazi177@morris.umn.edu

ABSTRACT

[Abstract contents]

Keywords

Scheduling, Threads, Multiprocessing, Processors

1. INTRODUCTION

[Introduction contents]

2. BACKGROUND

[Body text]

2.1 Threads and Threading

[Body text]

2.2 Completely Fair Scheduler

[Body text]

2.3 Cache on NUMA Systems

[Body text]

2.4 Cache Locality

[Body text]

3. METHODS

[Body text]

3.1 Shuffler and Jumbler

[Body text]

3.1.1 Placing Threads to Improve Locality

[Body text]

3.1.2 Shuffler

[Body text]

3.1.3 Jumbler

[Body text]

3.1.4 Shuffler and Jumbler Performance

[Body text]

3.2 FLSCHEd for Xeon Phi Manycore Processor

[Body text]

3.2.1 Lockless Thread Scheduler

[1, 3, 2] [4]

3.2.2 FLSCHEd Performance

[Body text]

4. CONCLUSIONS

[Conclusion text]

Acknowledgments

5. REFERENCES

- [1] S. Aaronson. Guest column: NP-complete problems and physical reality. *SIGACT News*, 36:30–52, March 2005.
- [2] Y. Brun. Solving NP-complete problems in the tile assembly model. *Theor. Comput. Sci.*, 395:31–46, April 2008.
- [3] M. R. Garey and D. S. Johnson. *Computers and Intractability: A Guide to the Theory of NP-Completeness*. W. H. Freeman & Co., New York, NY, USA, 1979.
- [4] M. Oltean and O. Muntean. Solving NP-complete problems with delayed signals: An overview of current research directions. In *Proceedings of the 1st international workshop on Optical SuperComputing, OSC '08*, pages 115–127, Berlin, Heidelberg, 2008. Springer-Verlag.