PL1167/PL1166A
User Manual

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Sincerity, Cooperation, Innovation

SUZHOU POWERLINK MICROELECTRONICS INC.

Contents

1 Configuration Registers

The configuration of PL1167/PL1166A is done by programming 16-bit registers. The optimum configuration data are updated in this user manual. Complete descriptions of the registers are given in the following tables. After chip reset, all the registers have default values as shown in the tables. The optimum register setting might differ from the default value. After a reset all registers that shall be different from the default value therefore needs to be programmed through the SPI interface.

Address (Hex)		Mnemonic	Bit	Default Value	Type	Description
3	**03**	**RF Synthesizer Lock Status Register**				
		RSV	15:13	-	R	Reserved
		RF_SYN_LOCK	12	-	R	Indicate RF synthesizer lock status. 1: locked 0: unlocked
		RSV	11:0	-	R	Reserved
6	**06**	**RAW RSSI Value Register**				
		RAW_RSSI	15:10	-	R	Indicate 6 bits raw RSSI value
		RSV	11:0	-	R	Reserved
7	**07**	**TX/RX Enable and Channel Register**				
		RSV	15:9	-	W/R	Reserved
		EN_TX	8	-	W/R	Enable transmit state, active high. Can't set EN_TX and EN_RX at the same time.
		EN_RX	7	-	W/R	Enable receive state, active high. Can't set EN_TX and EN_RX at the same time.
		RF_CH_SEL	6:0	-	W/R	Select RF channel frequency: f = 2402 + RF_CH_SEL
9	**09**	**PA Control Register**				
		RSV	15	-	W/R	Reserved
		PA_PWRC	14:12	-	W/R	PA high power current control
		RSV	11	-	W/R	Reserved
		PA_GAIN	10:7	-	W/R	Transmit PA gain control
		RSV	6:0	-	W/R	Reserved
11	**0B**	**RSSI OFF Control Register**				

Address (Hex)		Mnemonic	Bit	Default Value	Type	Description
		RSV	15:9	-	W/R	Reserved
		RSSI_OFF	8	-	W/R	0: RSSI power on 1: RSSI power off
		RSV	7:0	-	W/R	Reserved
23	**17**	**VCO Calibration Enable Register**				
		RSV	15:3	-	W/R	Reserved
		EN_VCO_CAL	2	-	W/R	Enable VCO calibration before TX/RX, active high
		RSV	1:0	-	W/R	Reserved
32	**20**	**Data Configure Register**				
		LEN_PREAMBLE	15:13	000B	W/R	000: 1 byte 001: 2 bytes 010: 3 bytes …… 111: 8 bytes
		LEN_SYNCWORD	12:11	11B	W/R	00: 16 bits, SYNCWORD[15:0] 01: 32 bits, SYNCWORD[63:48,15:0] 10: 48 bits, SYNCWORD[63:32,15:0] 11: 64 bits, SYNCWORD[63:0]
		LEN_TRAILER	10:8	000B	W/R	000: 4 bits 001: 6 bits 010: 8 bits …… 111: 18 bits
		TYPE_PKT_DAT	7:6	00B	W/R	00: NRZ law data 01: Manchester data type 10: 8/10 bits line code 11: Interleave data type
		TYPE_FEC	5:4	00B	W/R	00: No FEC 01: FEC13 10: FEC23 11: Reserved
		RSV	3:0	0110B	W/R	Reserved

Address (Hex)		Mnemonic	Bit	Default Value	Type	Description
33	**21**	**Delay Time Control Register 0**				
		DLY_VCO_ON	15:8	63H	W/R	Configure delay time for VCO stable after setting TX/RX. 1 represents 1us 01H: 1us 02H: 2us …… 63H: 99us ……
		DLY_PA_OFF	7:6	00B	W/R	Configure internal PA off delay time after setting PA_OFF. 00: 4us 01: 5us 10: 6us 11: 7us
		DLY_PA_ON	5:0	07H	W/R	Configure internal PA on delay time after setting VCO_ON. 1 represents 1us 01H: 1us 02H: 2us …… 07H: 7us ……
34	**22**	**Delay Time Control Register 1**				
		BPKTCON_DIR	15	0B	W/R	When direct mode, control PA on of TX and wide/narrow mode of RX.
		DLY_TX_CW	14:8	03H	W/R	Transmit continual wave (CW) modulation data before transmit data, after PA on, continue TX CW mode time.
		RSV	7:6	00B	W/R	Reserved
		DLY_SW_ON	5:0	0BH	W/R	Delay time of internal RF switch turn on after setting VCO_ON. 1 represents 1us 01H: 1us 02H: 2us …… 0BH: 11us

Address (Hex)		Mnemonic	Bit	Default Value	Type	Description
						……
35	**23**	**Power Management and Miscellaneous Register**				
		STOP	15	0B	W/R	STOP mode，active high Set oscillator off, then power down LDO. Note: All registers value will be lost.
		SLEEP	14	0B	W/R	SLEEP mode，active high Set crystal off only, keep LDO power on.
		RSV	13	0B	W/R	Reserved
		OSC_ON_SLEEP	12	1B	W/R	Keep oscillator running in SLEEP mode, active high 1: oscillator running in sleep mode more current but fast wakeup 0: oscillator stops in sleep mode low current but slow wakeup
		RETX_TIMES	11:8	3H	W/R	Max re-transmit packet times when AUTO_ACK is used. 2H: 1 times 3H: 2 times 4H: 3 times ……
		DIS_SDO_TRI	7	0B	W/R	0: SDO is tri-state when SCSB is1 1: SDO is low-Z when SCSB is 1
		SCR_SEED	6:0	00H	W/R	Data scramble seed
36	**24**	**SYNCWORD Register 0**				
		SYNCWORD[15:0]	15:0	0000H	W/R	LSB bits of sync word are first
37	**25**	**SYNCWORD Register 1**				
		SYNCWORD[31:16]	15:0	0000H	W/R	LSB bits of sync word are first
38	**26**	**SYNCWORD Register 2**				
		SYNCWORD[47:32]	15:0	0000H	W/R	LSB bits of sync word are first
39	**27**	**SYNCWORD Register 3**				
		SYNCWORD[63:48]	15:0	0000H	W/R	LSB bits of sync word are first
40	**28**	**FIFO and SYNCWORD Threshold Register**				

Address (Hex)		Mnemonic	Bit	Default Value	Type	Description
		TH_FIFO_EMPTY	15:11	00100B	W/R	Threshold of FIFO empty
		TH_FIFO_FULL	10:6	00100B	W/R	Threshold of FIFO full
		TH_SYNCWORD	5:0	07H	W/R	Threshold of sync word
41	**29**	**Miscellaneous Register**				
		CRC_ON	15	1B	W/R	0: CRC off 1: CRC on
		SCR_ON	14	0B	W/R	0: scramble off 1: scramble on
		EN_PACK_LEN	13	1B	W/R	1: Hardware regard first byte of payload as packet length
		FW_TERM_TX	12	1B	W/R	0: Firmware handle length and terminate TX 1: When FIFO write pointer and read pointer are equal, hardware will terminate TX when firmware handle packet length
		AUTO_ACK	11	1B	W/R	0: After received data, don't send ACK/NACK, just enter IDLE state 1: After received data, send ACK/ NACK automatically
		PKT_LEVEL	10	0B	W/R	0: PKT active high 1: PKT active low
		RSV	9:8	00B	W/R	Reserved
		CRC_INIT_DAT	7:0	00H	W/R	CRC initial data
42	**2A**	**SCAN RSSI Register 0**				
		SCAN_RSSI_CH	15:10	00H	W/R	Scan RSSI channel number
		RSV	9:8	01B	W/R	Reserved
		RX_ACK_TIME	7:0	6BH	W/R	Wait RX_ACK Timer. 1 represents 1us 01H: 1us 02H: 2us …… 6BH: 107us ……
43	**2B**	**SCAN RSSI Register 1**				
		EN_SCAN_RSSI	15	0B	W/R	Start scan RSSI value, active high

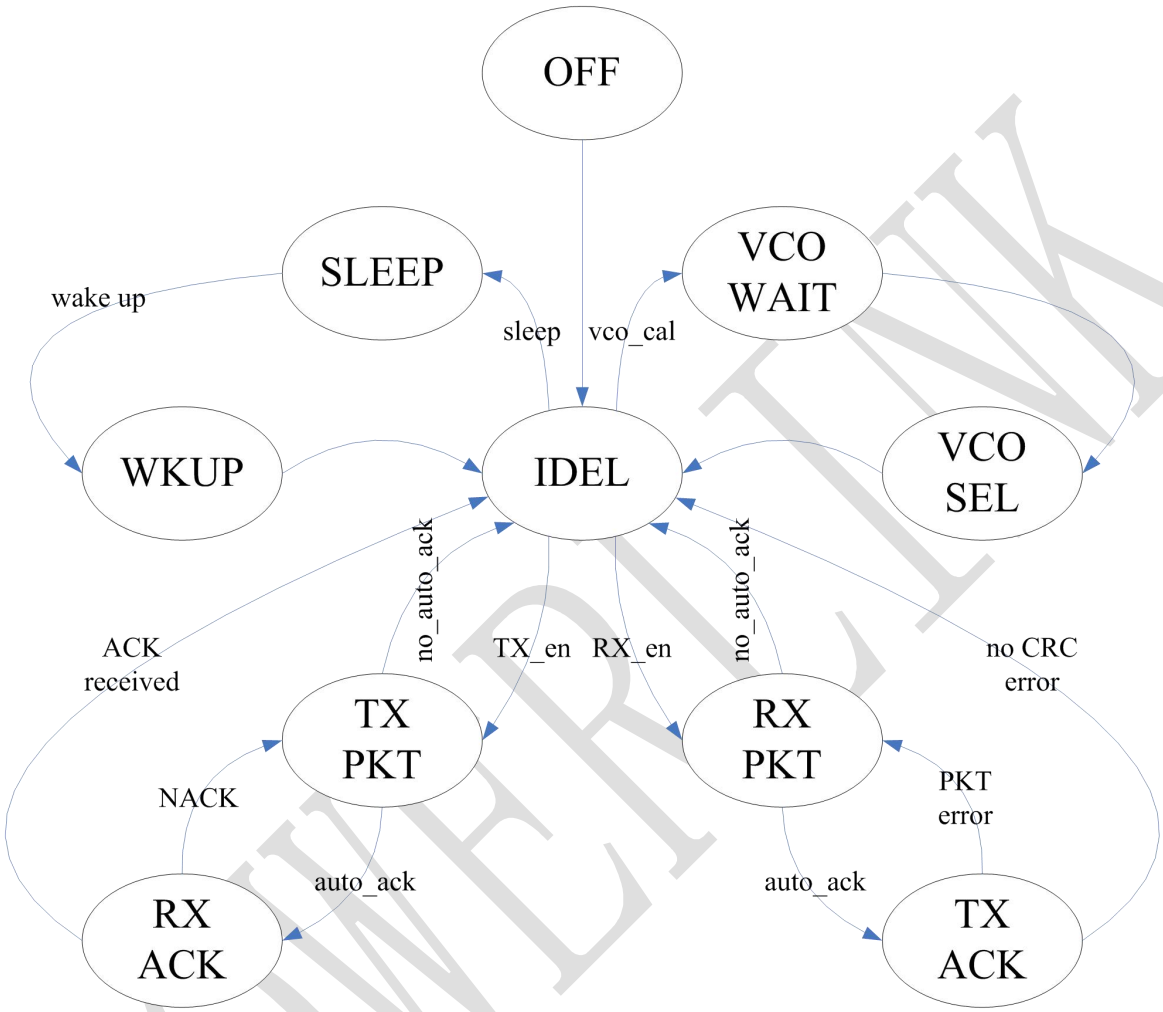
Address (Hex)		Mnemonic	Bit	Default Value	Type	Description
		OFFSET_SCAN_CH	14:8	01H	W/R	Scan RSSI start channel offset: Example: 10H, scan from 2412MHz (Usually scan RSSI from 2402MHz)
		DLY_SCAN_RSSI	7:0	6BH	W/R	Set delay time of VCO and SYN stable, when scan different channel RSSI.
48	**30**	**Status Register**				
		CRC_ERR	15	-	R	1: CRC error
		FEC23_ERR	14	-	R	1: FEC23 error
		FRAME_STAT	13:8	-	R	Frame status
		SYNCWORD_RECV	7	-	R	1: received sync word, only available in received status. When out received status, it is 0.
		PKT_FLAG	6	-	R	PKT flag
		FIFO_FLAG	5	-	R	FIFO flag
		RSV	4:0	-	R	Reserved
50	**32**	**FIFO Data Register**				
		FIFO_DAT	15:0	0000H	W/R	MCU read/write data of FIFO
52	**34**	**FIFO Pointer Register**				
		CLR_TX_PTR	15	0B	W	1: clear TX FIFO pointer and data to 0
		RSV	14	-	W	Reserved
		FIFO_WR_PTR	13:8	-	R	FIFO write pointer
		CLR_RX_PTR	7	0B	W	1: clear RX FIFO pointer and data to 0
		RSV	6	-	R	Reserved
		FIFO_RD_PTR	5:0	-	R	FIFO read pointer When AUTO_ACK, it is used as flag: When PKT is high, read the register, if it is 00H means that ACK is received.

2 Register Optimum Values

The following register values are optimum for most typical applications.

Address (Hex)		Reset Value (Hex)	Optimum Value (Hex)		Address (Hex)		Reset Value (Hex)	Optimum Value (Hex)
0	00	6FEF	6FE0		8	08	71AF	6C90
1	01	5681	5681		9	09	3000	1840
2	02	6619	6617		10	0A	7FFD	7FFD
3					11	0B	4008	0008
4	04	5447	B1A0		12	0C	0000	0000
5	05	F000	C000		13	0D	4855	48BD
6					14			
7	07	0030	0030		15			
16					24	18	307B	0067
17					25	19	1659	1659
18					26	1A	1833	19E0
19					27	1B	9100	1300
20					28	1C	1800	1800
21					29	1D	00X0	read only
22	16	C0FF	00FF		30	1E	F413	read only
23	17	8005	8005		31	1F	1002	read only
32	20	1806	4000		40	28	2107	4401
33	21	6307	3FC7		41	29	B800	B000
34	22	030B	2000		42	2A	FD6B	FDB0
35	23	1300	0380		43	2B	000F	000F
36	24	0000	sync word		44			
37	25	0000	sync word		45			
38	26	0000	sync word		46			
39	27	0000	sync word		47			

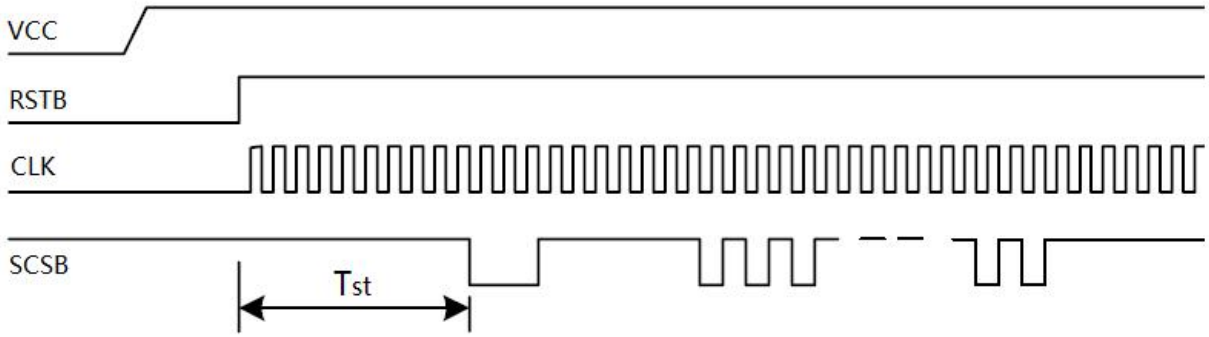
3 State Diagram



4 Operation Instruction

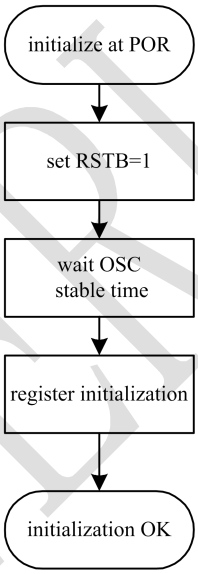
The following items show all sequences for PL1167/PL1166A. You can refer to this chapter and complete your programs. Please contact POWERLINK if any question.

4.1 Register Initialization



After the power supply VCC is ready, a valid reset on the pin RSTB is needed, which is low level active. After RSTB = 1, oscillator is running. The crystal oscillator will be stable after waiting Tst (1~5ms), then firmware can initialize registers.

After registers is initialized, PL1167/PL1166A is ready for transmit or receive.



4.2 Sleep Mode

PL1167/PL1166A will enter into sleep state, when firmware write register to enter sleep mode and pull SCSB back to high level.

PL1167/PL1166A will be waked up automatically from sleep state when pull SCSB to low level. Firmware should keep SCSB low level for oscillator stable time before write SPI data.

4.3 Packet Format

Over-the-air packet format is showed as follows.

Preamble	SyncWord	Trailer	Payload	CRC

- Preamble: 1~8 bytes
- SyncWord: 16/32/48/64 bits
- Trailer: 4~18 bits
- Payload: TX/RX data
- CRC: 16 bits CRC, optional

4.4 Clear FIFO Pointer

Before transmit, the FIFO write pointer should be cleared before firmware write data to FIFO.

The FIFO write pointer will be cleared automatically after SYNC is received.

The FIFO read pointer will indicate the byte number of received data which are in FIFO.

The FIFO read pointer will be cleared automatically after SYNC is transmitted in transmit mode or SYNC is received.

4.5 Payload Length

There are two ways to handle TX/RX packet length.

When REG41.EN_PACK_LEN = 1, hardware framer will detect packet length according to the value of the 1st payload byte.

Example: If want to transmit 8 bytes data, the 1st byte should be 8 and total byte length should be 9.

When REG41.EN_PACK_LEN = 0, the 1st byte of payload data has no special meaning, and packet length is determined by either TX FIFO is empty or EN_TX bit is cleared.

EN_PACK_LEN	FW_TERM_TX	Description
0 : Firmware handle packet length	0	Terminate transmit only when REG7.EN_TX = 0. Terminate receive only when REG7.EN_RX = 0.
	1	Terminate transmit automatically when TX FIFO is empty. Terminate receive only when REG7.EN_RX = 0.
1 : Hardware handle packet length	x	The 1st byte of payload is used as packet length. Terminate transmit automatically when all bytes are transmitted.

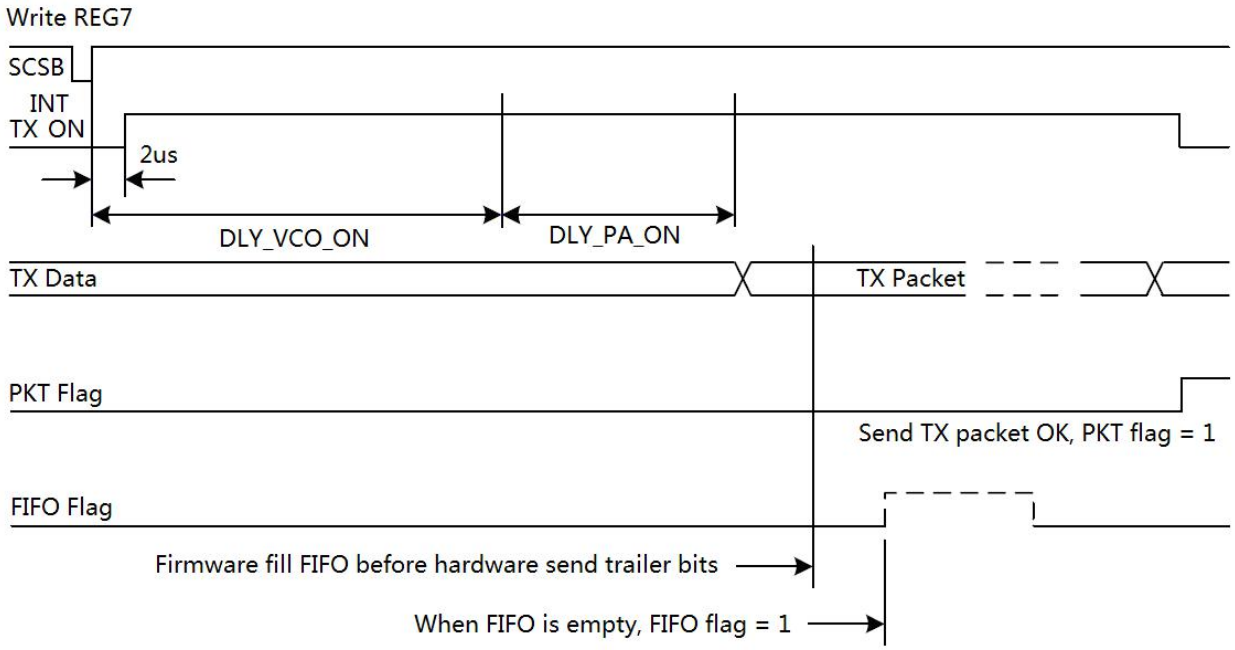
4.5.1 Hardware Handle Packet Length

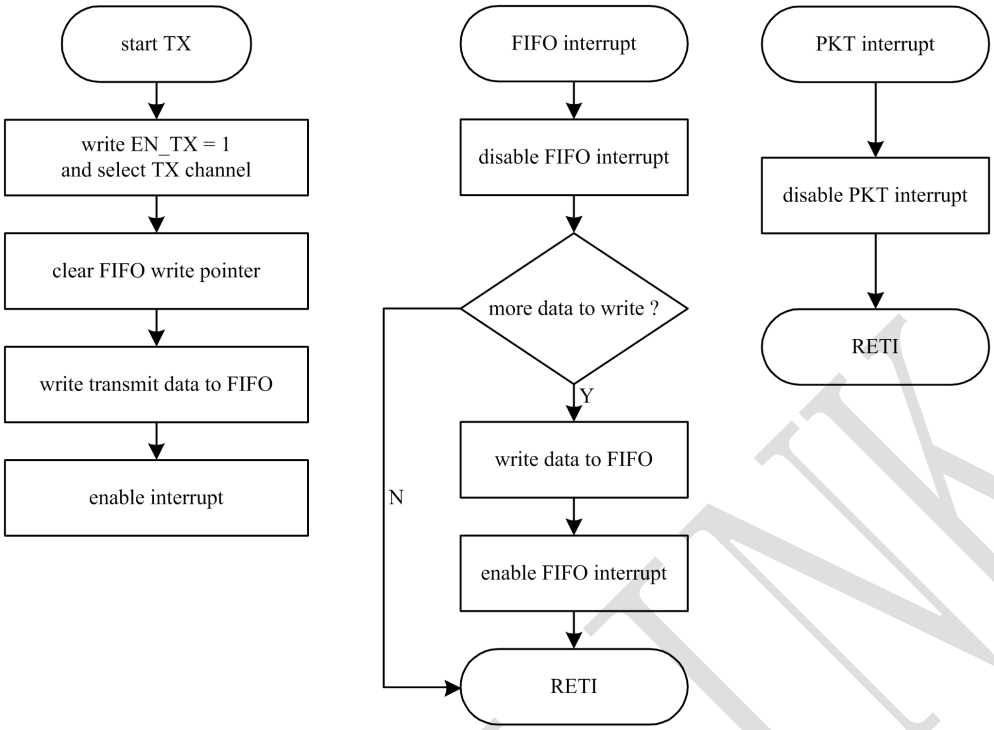
Hardware framer will handle packet length by setting REG41.EN_PACK_LEN = 1. The 1st byte of payload is used as packet length, but this length byte is not counted in packet length. Hardware framer will handle TX/RX start and stop.

4.5.1.1 Transmit

Hardware framer will automatically generate the packet by using payload data from FIFO after firmware write REG7.EN_TX = 1 and select transmit channel. Firmware should fill in transmit data before hardware framer send trailer bits.

In transmit state, when packet length exceed FIFO length, firmware should write FIFO data multiple times. FIFO flag indicate whether FIFO is empty or not.





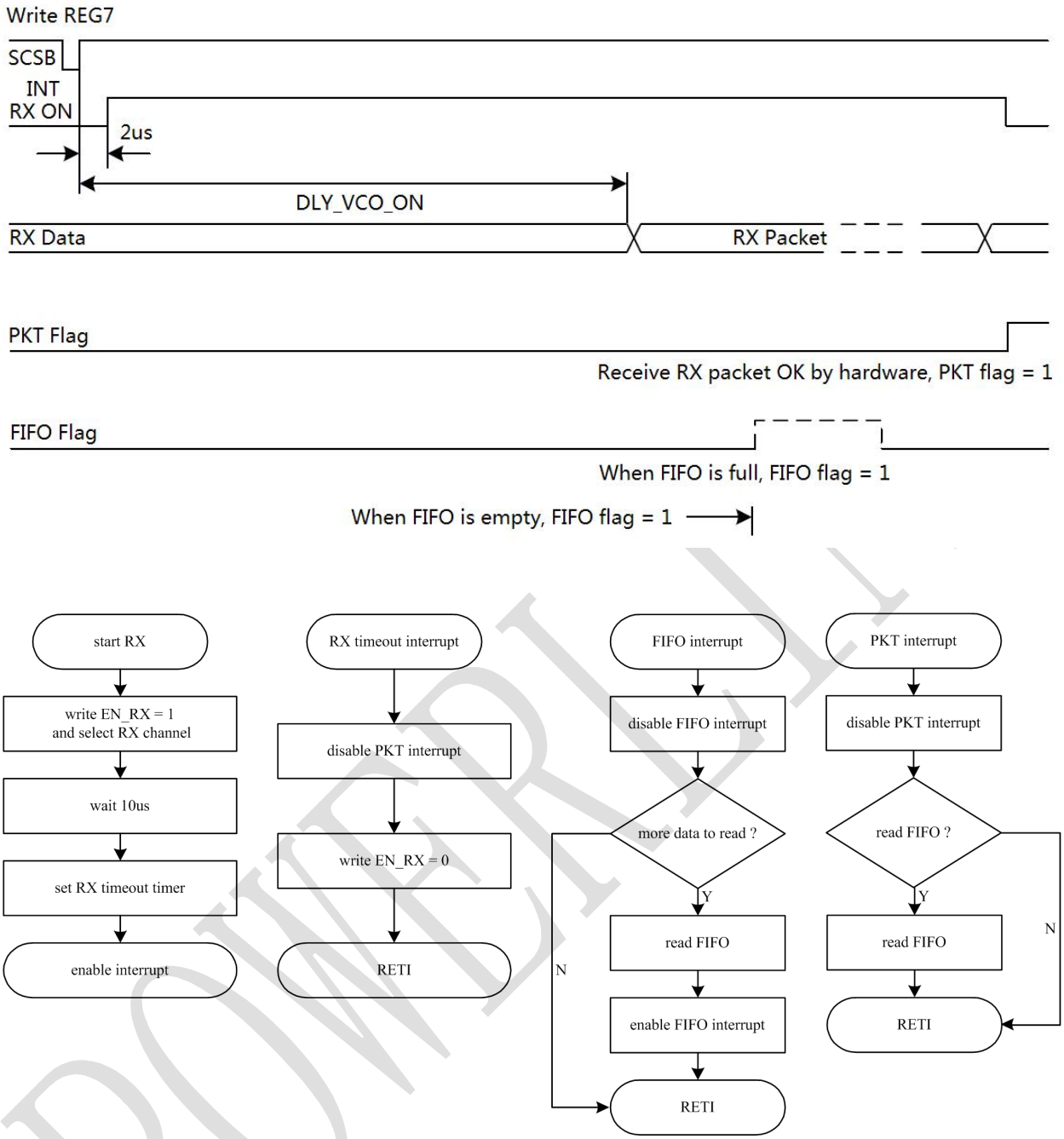
4.5.1.2 Receive

Hardware framer will turn on the receiver and wait a valid sync word to be detected after firmware writes REG7.EN_RX = 1 and select receive channel.

When received a valid sync word, hardware framer will process packet automatically. When received packet processing is completed, hardware framer will set state to IDLE.

When received packet length is longer than 63 bytes, FIFO flag will take effect, which means that firmware must read out data from FIFO.

A valid sync word will not always be received, due to weak signal, multi-path signal cancellation, devices out of range, etc. To accommodate such a condition and prevent lockup, firmware should use a receive timeout timer. In most applications, receive packet are expected to arrive within a defined time window. When the packet does not arrive in this window, system should use the timer to take corrective action.



4.5.2 Firmware handle packet length

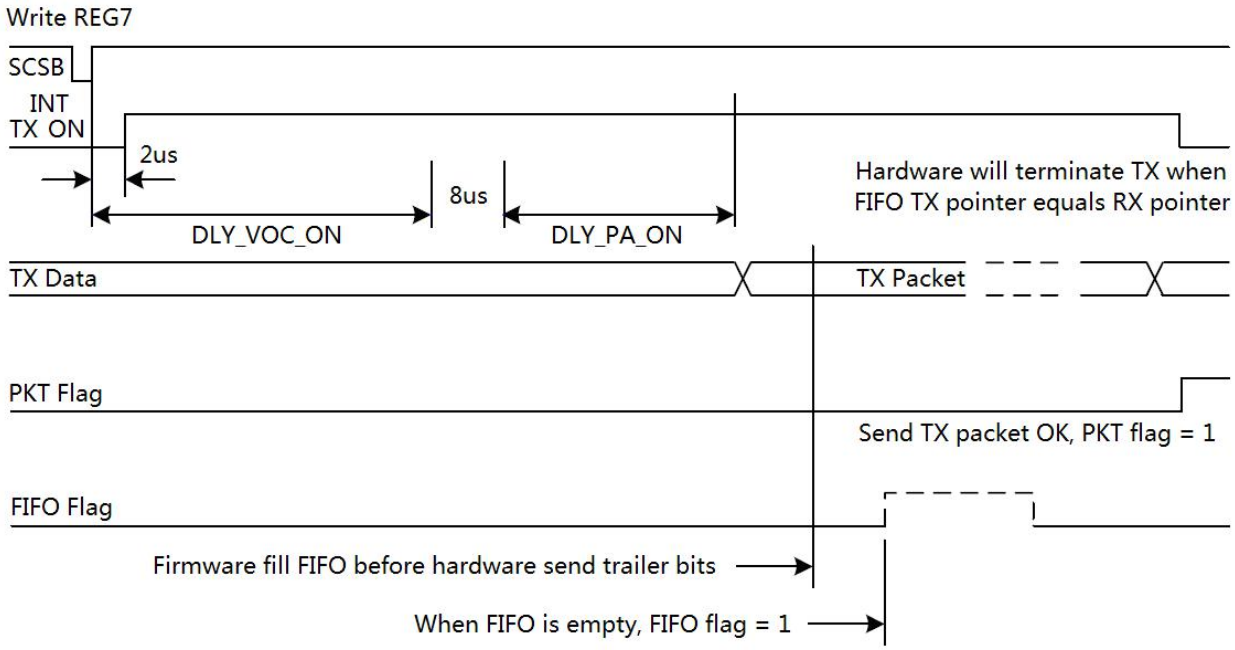
When REG41.EN_PACK_LEN = 0, the 1st byte of payload data has no special meaning.

At this time, packet length will depend on REG41.FW_TERM_TX.

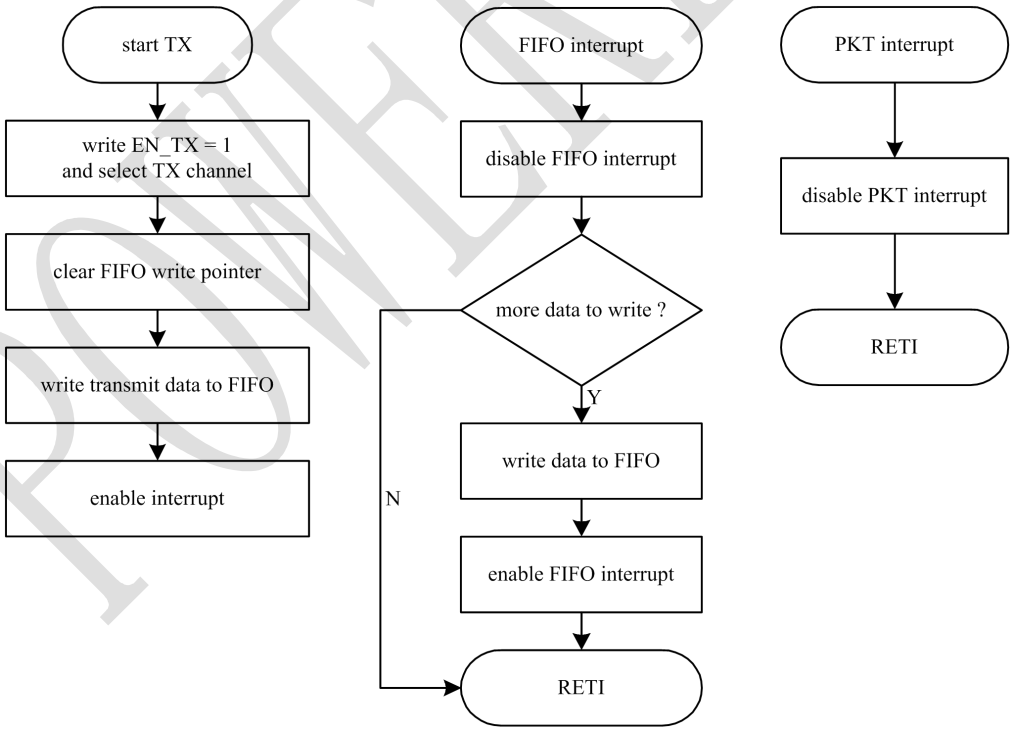
4.5.2.1 Transmit (FW_TERM_TX = 1)

When REG41.EN_PACK_LEN = 0 and REG41.FW_TERM_TX = 1, hardware framer will continue to

compare FIFO write pointer and read pointer during packet transmission. If firmware stop writing data to FIFO, hardware framer will detect that there is no data to send (FIFO is empty), then PL1167/PL1166A will terminal packet transmission automatically.

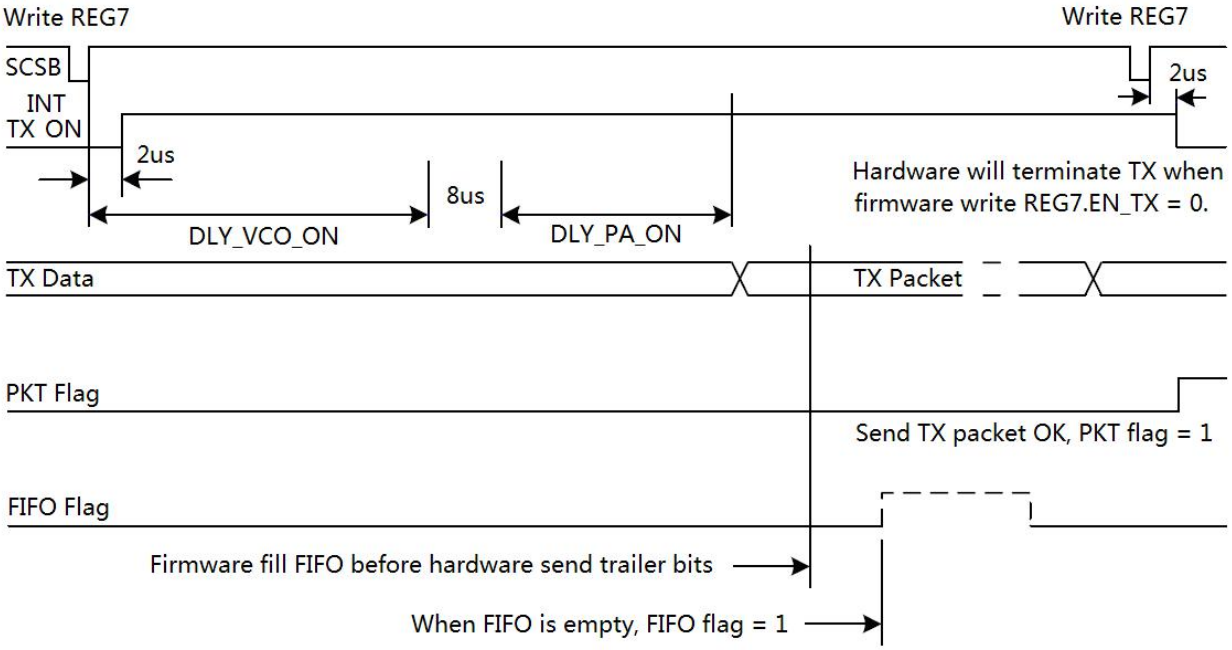


Note: When REG41.EN_PACK_LEN = 0, never let FIFO underflow or overflow. FIFO threshold can be set by REG40.TH_FIFO_EMPTY and REG40.TH_FIFO_FULL.

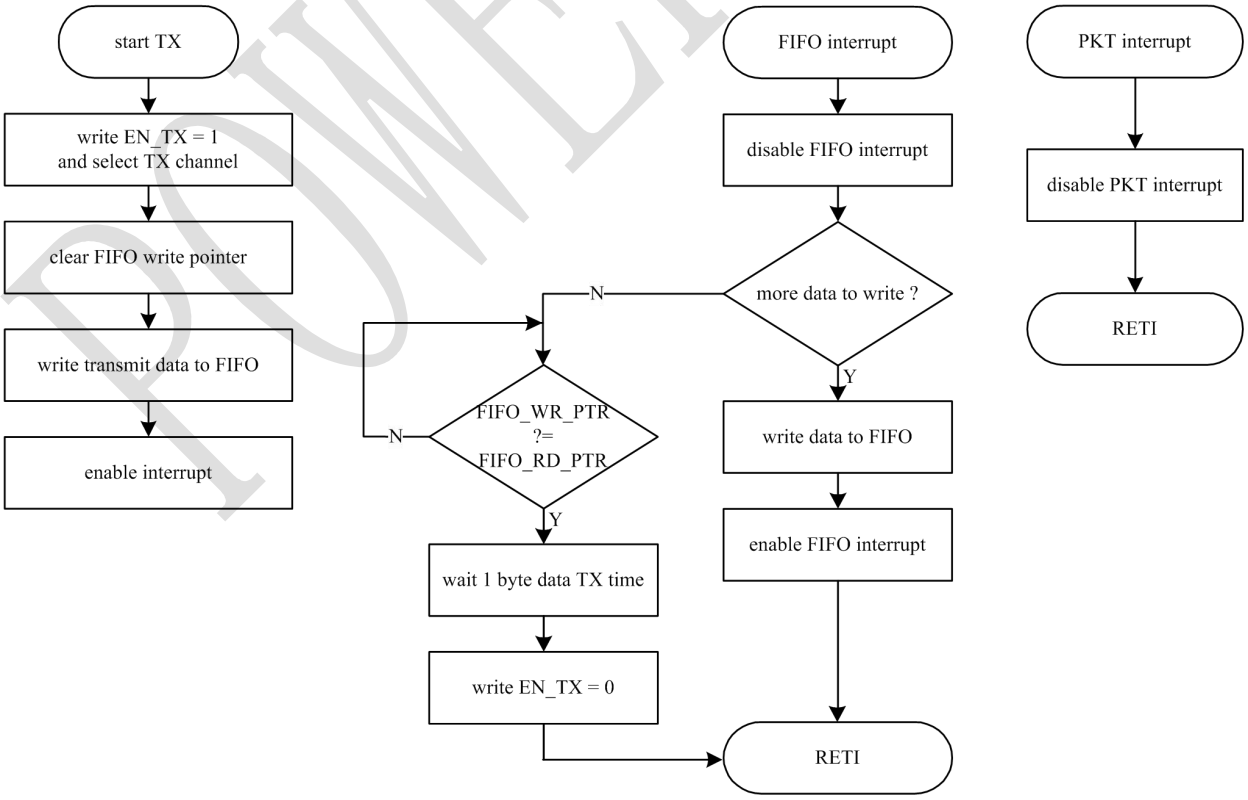


4.5.2.2 Transmit (FW_TERM_TX = 0)

When REG41.EN_PACK_LEN = 0 and REG41.FW_TERM_TX = 0, packet transmission will continue even if FIFO is empty. Hardware framer don't terminate packet transmission until firmware write REG7.EN_TX = 0.



Note: When REG41.EN_PACK_LEN = 0, never let FIFO underflow or overflow. FIFO threshold can be set by REG40.TH_FIFO_EMPTY and REG40.TH_FIFO_FULL.



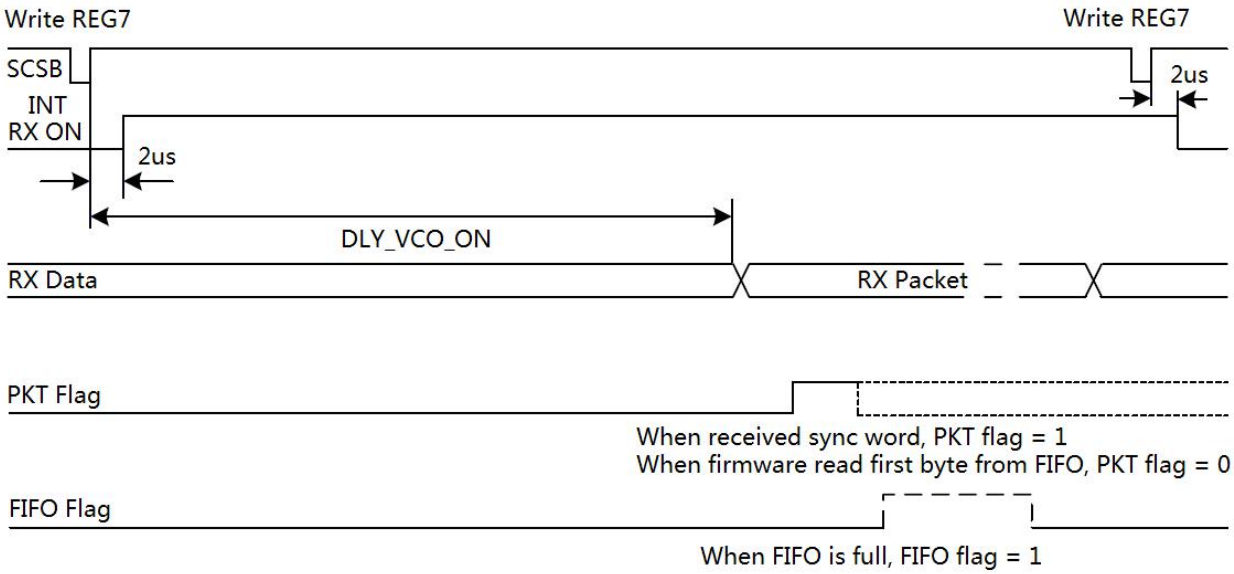
4.5.2.3 Receive

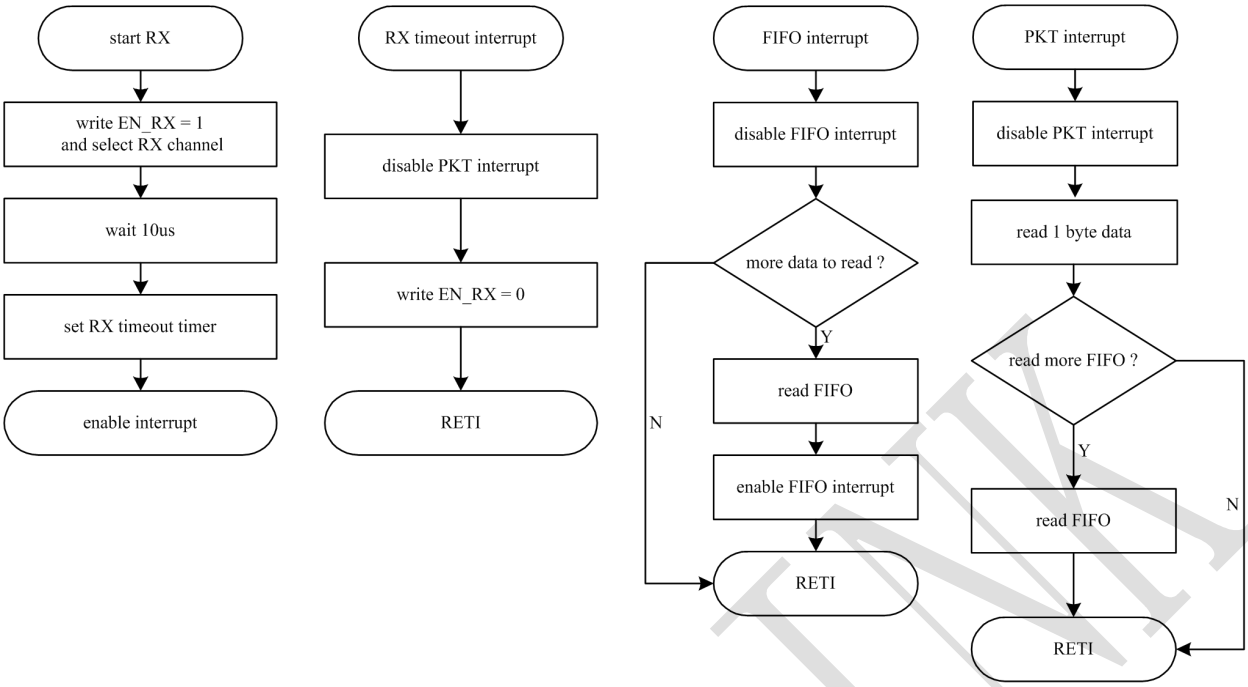
When REG41.EN_PACK_LEN = 0, packet reception will be started when firmware write REG7.EN_RX = 1. At this time, hardware framer will automatically turn on receiver to the frequency/channel which is set in REG7.

After waiting for the internal synthesizer and receiver to be stable, hardware framer will begin searching the incoming signal for a sync word. Once detected it will set PKT flag active, then start to fill FIFO with received data.

The PKT flag will remain active until firmware read out the first byte of data from FIFO register. After firmware read the first byte of received data, PKT flag will be inactive until next TX/RX period.

With REG41.FW_TERM_TX = 0 or 1, hardware will always need firmware to write REG7.EN_RX = 0 to terminate RX state.





4.6 Transceive Flow

- **Register Initialization**

  Initialize all registers according to the optimum values.

- **Transmit Flow**

  Set REG52.CLR_TX_PTR = 1 to empty TX FIFO pointer and data.

  Fill in the transmit data bytes to the FIFO data register REG50.

  Set REG7.EN_TX = 1, and select RF channel frequency.

  Wait for PKT flag to be pulled up.

- **Receive Flow**

  Set REG52.CLR_RX_PTR = 1 to empty RX FIFO pointer and data.

  Set REG7.EN_RX = 1, and select RF channel frequency.

  Wait for PKT flag to be pulled up.

  Read out data bytes from the FIFO data register REG50 once PKT flag is pulling up.

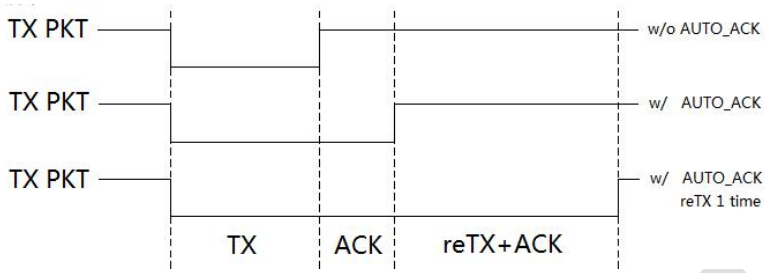
4.7 AUTO_ACK Usage

PL1167/PL1166A have AUTO_ACK function, the usage is shown below.

1. Set REG41.AUTO_ACK = 1 to enable AUTO_ACK function.
2. Set REG35.RETX_TIMES = n, it means that TX will re-transmit maximum (n-1) times if the ACK of

RX is not received.

3. Set REG42.RX_ACK_TIME = B0H, it means that TX will re-transmit if the ACK of RX is not received after 176us waiting time.



ACK time is about 150us, it is related with the length of sync word and preamble, etc.

When PKT is pulled up, read out REG52.FIFO_RD_PTR, if it is 00H means that ACK is received.

4.8 Hardware Retransmission

To improve anti-interference performance, hardware retransmission can be used.

1. Set REG41.AUTO_ACK of TX side = 1 to enable AUTO_ACK function. And set REG41.AUTO_ACK of RX side = 0 to disable AUTO_ACK function.
2. Set REG35.RETX_TIMES, the maximum value is 16.
3. Set REG42.RX_ACK_TIME, waiting time of RX ACK can be set from 150~256us.
4. TX side will retransmit certainly because the AUTO_ACK of RX side is disabled. The resend data is the same as previous data, so this time transmission should be successful if the valid data is received once.

4.9 Oscillator

PL1167/PL1166A can support crystal oscillator and external clock.

- **Crystal Oscillator**

  Rs is series resistor which limits the power to crystal oscillator, and provide for the phase shift of crystal oscillator.

  Rf is self-bias resistor from buffer output to input which provide for self-bias of the on-chip buffer to the center of linear region for maximum gain.

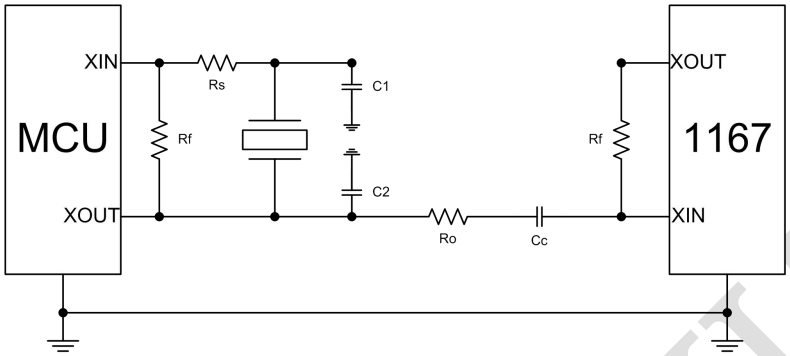
  C1 and C2 are the crystal load capacitors which should meet the crystal vendor's specification. These capacitor values can be fine-tuned to ensure the accuracy of oscillation frequency.

- **External Clock**

  The external clock may be coupled to the XIN pin via a series DC-blocked capacitor. But self-bias resistor Rf should be still used.

  Use output resistor Ro to sample the existing oscillator. The optimum value of Ro should be determined according to experiment, but around 3k Ohms is a good starting point.

In PCB layout: The CLK path should be short and direct, and far away from noise signal source. The ground between two chips should be a good low-noise, low-inductance.



Notes: Clock duty cycle should be 50%. Insufficient clock drive or phase noise of reference clock signal will cause high BER.

4.10 PA Power Test

1. Correctly setting the DUT (Testing Board), especially the power supply, the MCU control interface.
2. Correctly connecting the DUT (Testing Board) to the Spectrum Analyzer.
3. Carefully calibrating the SMA cable that connect with both the DUT (Testing Board) and the spectrum Analyzer.
4. Correctly power on the DUT (Testing Board).
5. Roughly checking the DUT (Testing Board) power consumption within the specified range, in order to ensure the DUT (Testing Board) work at the correct state.
6. Carefully checking the reference oscillator on board with Frequency Counter, in order to guarantee the accuracy of the reference clock.
7. Correctly initialing the DUT (Testing Board) with optimum register setting, which is recommended in user manual.
8. Correctly setting the DUT (Testing Board) to TX state by setting the register REG7 to value 0x0130H.
9. Correctly setting the DUT (Testing Board) to TX Continuous Wave Mode, which means that continuously power output and no modulation index, by setting the register REG11 to value 0x8008H.
10. Optionally setting the DUT (Testing Board) to Direct Mode, which means directly output, bypass the baseband, by setting the register REG32 to value 0x1807H and the register REG34 to value 0x830BH.
11. Carefully checking the TX output power value measured on the Spectrum Analyzer.
12. Modify the related Channel Number Control, Gain Control and etc. register, then, measure again.

Register	Value (Hex)
REG7	0130
REG11	8008
REG32	1807

Register	Value (Hex)
REG34	830B

After all the above registers are written, PA spectrum can be tested from a spectrum analyzer, only carrier, no modulation. PA power can be controlled by REG9.PA_PWRC and REG9.PA_GAIN.

4.11 RSSI Test

1. Initialize all registers according to the optimum values after POR.
2. Set chip to RX state, write REG7 to 00B0H.
3. Read out raw RSSI from REG6.RAW_RSSI.

5 Document Revision History

Rev.	Date	Comments
0.2	2012/03/19	Preliminary Version
1.0	2016/11/07	Formal release Version: PL1167/PL1166A 1) Optimize the Optimum Value (Reg4-0xB1A0, Reg5-0xC000) to reduce the bit error rate and improve the RF received performance 2) Fixed 4.5.1.2 Receive: writes REG7.EN_RX = 1 and select receive channel

6 Important Notice

POWERLINK reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.