



– Handwritten Digits Recognition System – Research Report

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1 Introduction

1.1 Project

The target is to implement a Handwritten Digits Recognition system using Machine learning based on the Zedboard FPGA development kit. The tool used to program the Zedboard is the Xilinx Vivado High-Level Synthesis (HLS). The project is built based on two programming languages: Python and C.

1.2 Zedboard

ZedBoard™ is a complete development kit for designers using Xilinx Zynq®-7000 All Programmable SoC. The board provides various interfaces such as USB-JTAG Programming, USB OTG 2.0, USB-UART bridge, SD card and so on. Combining a dual Corex-A9 Processing System (PS) with Programmable Logic (PL) cells, the Zedboard can be targeted to use in many applications.

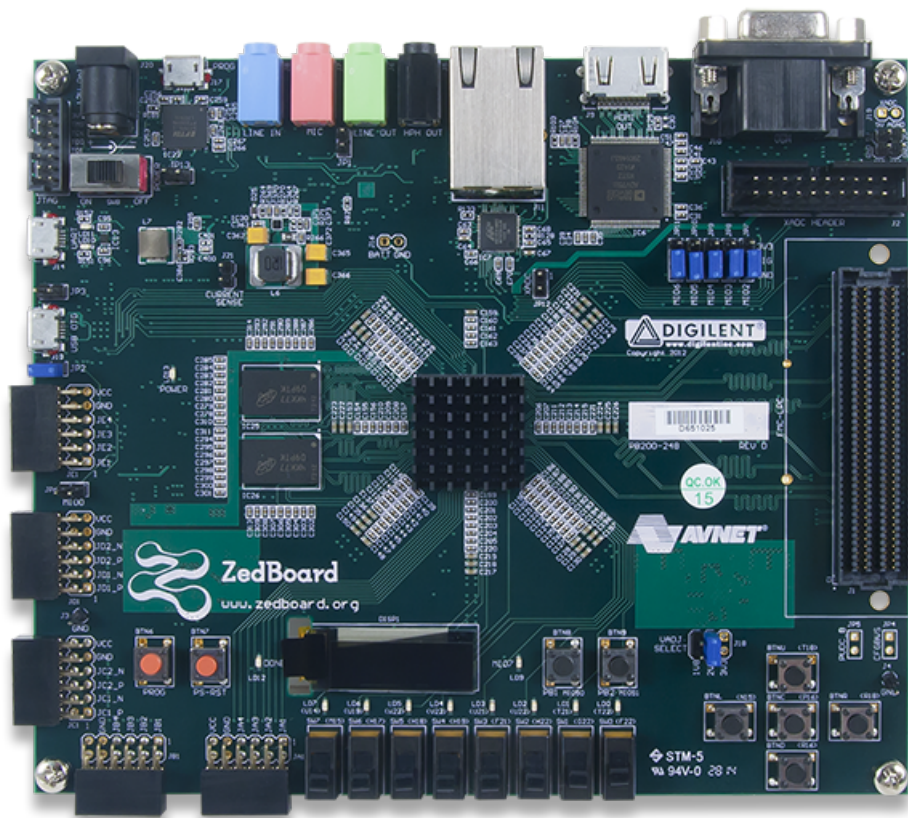


Figure 1: Zedboard

1.3 MNIST Database

The dataset consists of 60000 digits for the training set and 10000 examples for the test set. Each digit have been size-normalized and centered in a fixed-size 28x28 pixel image.



Figure 2: MNIST Database

1.4 Algorithm

In this project, the implementation of the system is based on Perceptron Learning Algorithm (PLA) - an algorithm for supervised learning of binary classifiers. A binary classifier is a function which can decide whether or not an input, represented by a vector of numbers, belongs to some specific class.

2 Methods

2.1 Pre-processing

2.2 Implement on Zedboard

In this project, the Perceptron algorithm is programed on the Zedboard via Quad SPI Flash, which is a non-volatile memory Zedboard's Zynq chip looks at on every startup. If Quad SPI is flashed



Figure 3: Quad SPI Flash

then the Zynq will program itself with the contents found in Quad SPI's Flash memory. A picture below indicates the set up of the Zedboard.

In a high productivity design flow, the primary means of generating the core design IP is through the use of C-based IP and High-Level Synthesis (HLS) of C code into RTL. The design flow for Vivado HLS is shown in the figure below.

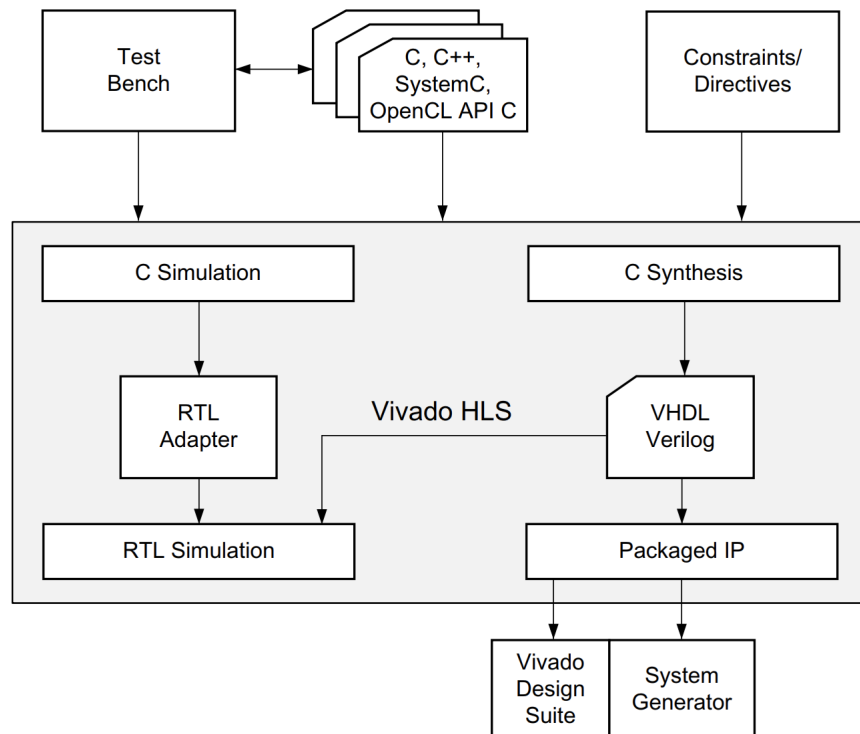


Figure 4: Vivado HLS design flow

3 Results

The source code of the project: <https://github.com/dangne/tk11HTR/>

4 Discussion

References

- [1] Zedboard
<http://zedboard.org/>
- [2] THE MNIST DATABASE of handwritten digits
<http://yann.lecun.com/exdb/mnist/>
- [3] Zedboard
<https://machinelearningcoban.com/2017/01/21/perceptron/>