

PseudowireCodeChip™Family

Jitter and Wander

Revision History

Revision	Date Updated	Author	Description
1.0	1-Jul-2017	Nguyen Khoa Minh Tri	Initial
2.0	1-Sep-2017	Nguyen Khoa Minh Tri	Add Jitter Tolerance and Jitter Transfer for STM Add JDSU's configuration for Jitter and Wander Add Anue's configuration Add sample result
3.0	20-Sep-2017	Nguyen Khoa Minh Tri	Add Jitter Generation for SONET <ul style="list-style-type: none"> - Category I Mapping Jitter - Category I Jitter due to Single Pointer - Category I Jitter due to Burst Pointer - Category I Jitter due to Periodic Pointer Add Wander Generation for SONET <ul style="list-style-type: none"> - Mapping Phase - Pointer Adjustment Phase Add Jitter Transfer for SONET Add Jitter Tolerance for SONET
4.0	03-Oct-2017	Nguyen Khoa Minh Tri	<ul style="list-style-type: none"> • Add E1 and E3 interface • Add Table and Mask of Jitter Tolerance for OC-x into Appendix • Add Configuration for ANUE and CALNEX
5.0	20-Dec-2017	Nguyen Khoa Minh Tri	<ul style="list-style-type: none"> • Add more section in Appendix <ul style="list-style-type: none"> ◦ Arrive common test models ◦ JDSU configuration ◦ Calnex configuration

			<ul style="list-style-type: none">○ ANUE configuration○ PRC box○ ADM (HPX) Configuration○ Get result and compare with Mask○ Network jitter recommendations for network interface
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ITU-T - G.812: Timing requirements of slave clocks suitable for use as node clocks in synchronization networks

ITU-T - G.813: Timing characteristics of SDH equipment slave clocks (SEC)

ITU-T - G.823: The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy

ITU-T - G.824: The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy

ITU-T - G.825: The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy (SDH)

ITU-T - G.783: Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks

ITU-T - G.8261: Timing and synchronization aspects in packet networks

GR-253: Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria

GR-499: Transport Systems Generic Requirements (TSGR) - Common Requirements

1 Requirements for DS1 Network Interface:

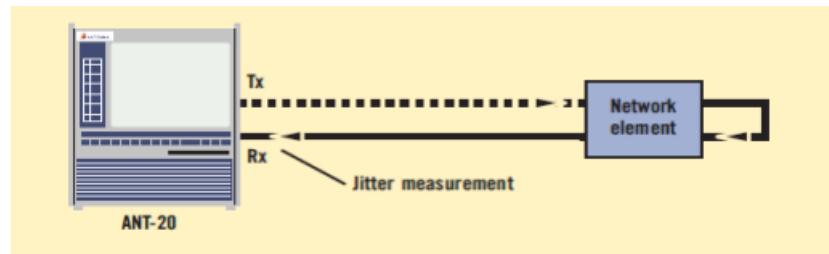
1.1 Jitter Generation:

1.1.1 Standard requirement:

Jitter output of DS1 signal at any network interface **Must** not exceed corresponding value in the table below

Bit Rate (Mb/s)	Network Jitter Limits (UI _{pp}) ^a		Measurement Filter Cutoff Frequencies		
	B ₁ (F ₁ to F ₄)	B ₂ (F ₃ to F ₄)	Lower Cutoff, F ₁	Lower Cutoff, F ₃	Minimum Upper Cutoff, F ₄
1.544	5	0.1	10 Hz	8 kHz	40 kHz
3.152	5	0.1	10 Hz	1.5 kHz	40 kHz
6.312	3	0.1	10 Hz	3 kHz	60 kHz
44.736	5	0.1	10 Hz	30 kHz	400 kHz

1.1.2 The testing model:



1.1.3 The sequence configuration:

- Step#1: Configure data path on DUT:
- Step#2: [Configure Jitter function on Tester](#)
- Step#3: Use Tester to measure B1 and B2 value in the following cases:
 - Loop-time/System/External/ACR/DCR
 - Test with temperature range
 - Test with many payload size
 - Test with RTP timestamp rates
 - Test with PDV and None-PDV

1.2 Jitter and Wander Tolerance:

1.2.1 Standard requirements:

- a. The jitter tolerance for DS1 interface **Must** follow Table-8/G824.
- b. The wander tolerance is basically like the Jitter Tolerance test, except that wander is a long-term phenomenon.

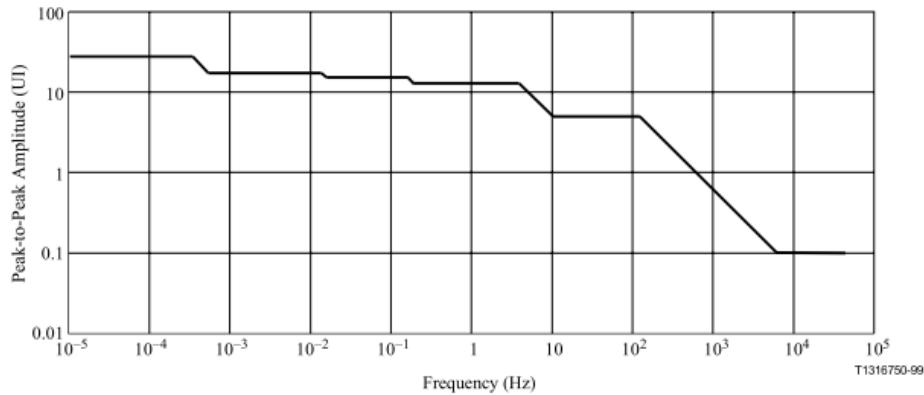
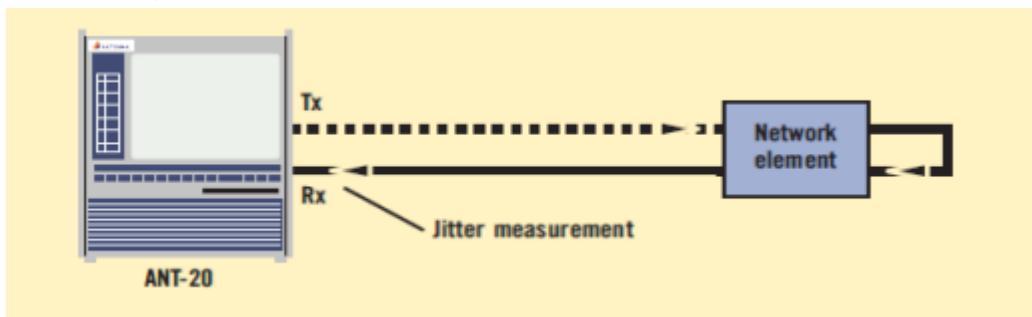


Table 8/G.824 – Jitter and wander tolerance of 1544 kbit/s input ports

Frequency f (Hz)	Peak-to-Peak Amplitude (UI)
$1.2 \times 10^{-5} \leq f \leq 3.5 \times 10^{-4}$	28 (18 μ s) (Note 2)
$3.5 \times 10^{-4} < f \leq 5.6 \times 10^{-4}$	$9.8 \times 10^{-3} f^{-1}$ ($6.35 \times 10^{-3} f^{-1} \mu$ s)
$5.6 \times 10^{-4} < f \leq 0.014$	17 (11 μ s)
$0.014 < f \leq 0.016$	$0.238 f^{-1}$ ($0.154 f^{-1} \mu$ s)
$0.016 < f \leq 0.16$	15 (10 μ s)
$0.16 < f \leq 0.19$	$2.4 f^{-1}$ ($1.6 f^{-1} \mu$ s)
$0.19 < f \leq 3.9$	13 (8.4 μ s)
$3.9 < f \leq 10$	$50.7 f^{-1}$ ($32.8 f^{-1} \mu$ s)
$10 < f \leq 120$	5 (3.2 μ s)
$120 < f \leq 6000$	$600 f^{-1}$ ($384 f^{-1} \mu$ s)
$6000 < f \leq 40\,000$	0.1 (0.0648 μ s) (Note 1)

NOTE 1 – This value requires further study.
 NOTE 2 – The value 18 μ s represents a relative phase deviation between the incoming signal and the internal local timing signal derived from the reference clock. An example of a reference configuration explaining the 18 μ s value is given in Annex A.

1.2.2 The testing model:



1.2.3 The sequence configuration

- a. Step#1: configure data path on DUT and start Jitter Tolerance function on Tester
- b. Step#2:configure Jitter Tolerance Mask on Tester
- c. Step#3: start measure Jitter Tolerance for the following cases. After Tester finished, save result
 - Loop-time/System/External/ACR/DCR
 - Test with temperature range
 - Test with many payload size
 - Test with RTP timestamp rates
 - Test with PDV and None-PDV

1.3 Wander generation:

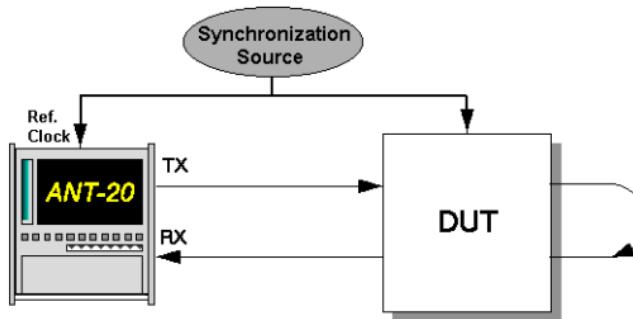
1.3.1 Standard requirement:

At the network interface, the wander of DS1 network signal shall not exceed an MTIE of 28UI (18us) for 24 hours nor shall it exceed an MTIE of 13UI (8.4us) for 15 minutes.

Table 2/G.824 – Synchronous network interface for 1544 kbit/s rate

Observation interval (τ) in seconds	MTIE in μ s
$\tau \leq 900$	8.4
$900 < \tau \leq 86\,400$	18.0

1.3.2 The testing model:



1.3.3 Test wander None-PDV for one channel:

- Step#1: Configure data path on DUT with the following cases:
 - ACR mode
 - DCR mode (enable RTP in this case)
- Step#2: [Configure wander function on Tester](#).
- Step#3: Start wander to check Locking time (in worst case, Locking time is around 15 minutes)
- Step#4: After check Locking time, get result and compare with G.824 mask
- Step#5: Restart Tester to measure wander around 1 hour
- Step#6: [Save wander result, get result and compare with G.824 mask](#)

1.3.4 Test wander None-PDV for multi-channels:

Refer the steps in section 1.3.3 with configuration is multi-channels.

1.3.5 Test Phase Transient:

At the network interface, during phase transients (typically due to network synchronization rearrangements), phase deviation shall not exceed 1us, and the frequency of signal shall not be offset from nominal frequency by more than 61 ppm. Phase transient are expected to be a rare occurrence.

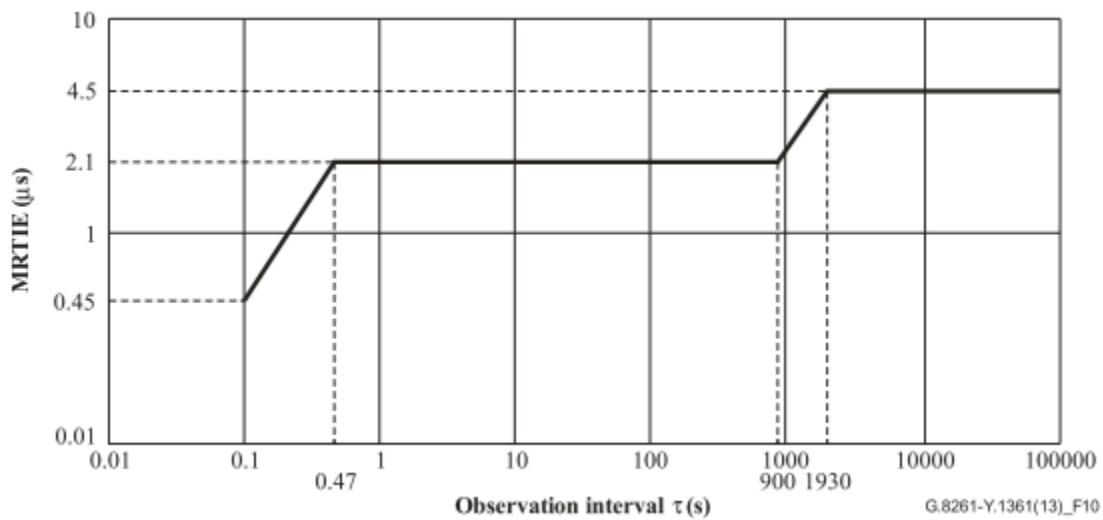
- a. Step#1: Configure data path on DUT:
 - ACR mode
 - DCR mode (enable RTP in this case)
- b. Step#2: Waiting for ACR/DCR was locked, start wander around 15 minutes
- c. Step#3: Unplug LIU around 15 minutes after plug LIU again.
- d. Step#4: Continuous measuring (around 15 minutes) to check Locking time and Phase Transient.
- e. Step#5: Repeat step#3 and #4 one more. Save total wander result

1.3.6 Measure test-case G.8261:

1.3.6.1 Standard requirement:

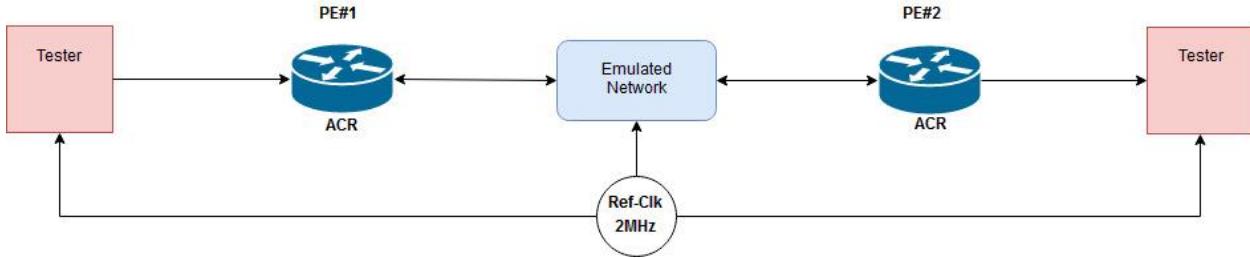
The wander budget, expressed in maximum relative time interval error, for DS1 signal is defined in Table below

Observation interval (τ) in seconds	MTIE in μs
$\tau \leq 0.1$	No Requirement (see Note)
$0.1 < \tau \leq 0.47$	4.5τ
$0.47 < \tau \leq 900$	2.1
$900 < \tau \leq 1930$	$2.33 \times 10^{-3} \tau$
$1930 < \tau \leq 86'400$	4.5
NOTE – This region is covered by jitter requirements.	



G.8261-Y.1361(13)_F10

1.3.6.2 Test-cases for ACR mode:



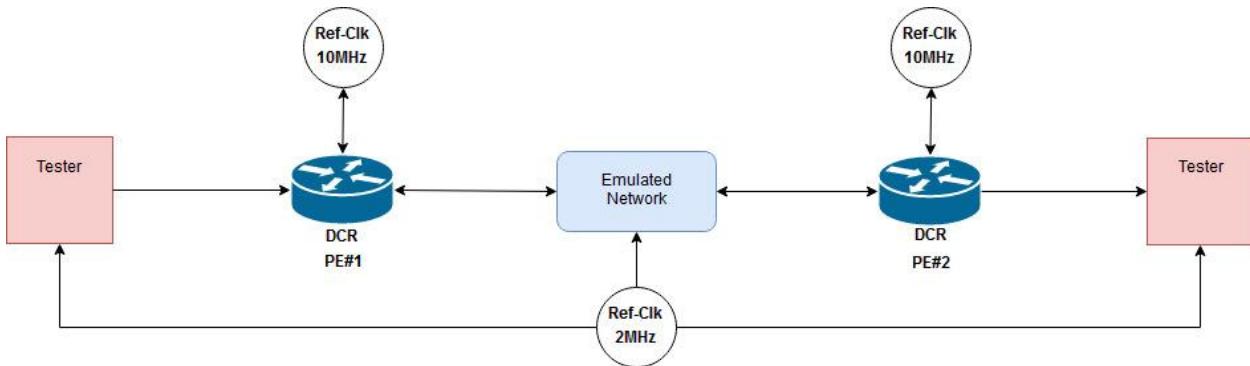
1.3.6.2.1 Test-case #1:

- a. Step#1: Configure data DS1 on DUT (only one channel) with ACR mode
- b. Step#2: Start Test-case #1 on ANUE Tester.
- c. Step#3: Waiting for ACR was locked, restart Tester to measure wander for Test-case #1
- d. Step#4: After Test-case#1 finished (check on ANUE), stop ANUE and save TIE data to compare with mask above.

1.3.6.2.2 Test-case #2, #3, #4, #5, #6, #7, #8:

Refer steps in section 1.3.6.2.1 to measure Test-case #2, #3, #4, #5, #6, #7, #8.

1.3.6.3 Test-cases for DCR mode:



1.3.6.3.1 Test-case #9:

- a. Step#1: Configure data path DS1 on DUT (only one channel) with DCR mode
- b. Step#2: Start Test-case #9 on ANUE Tester
- c. Step#3: Waiting for DCR was locked, restart Tester to measure wander for Test-case #9
- d. Step#4: After Test-case #9 finished (Check on ANUE), stop ANUE and save TIE data to compare with mask above.

1.3.6.3.2 Test-case #10, #11:

Refer steps in section 1.3.6.3.1 to measure Test-case #10, #11

2 Requirements for E1 Network Interface:

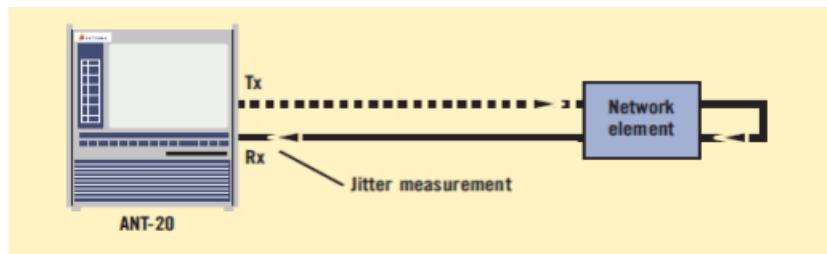
2.1 Jitter Generation:

2.1.1 Standard requirement:

Jitter output of E1 signal at any network interface **Must** not exceed corresponding value in the table below

Interface	Measurement bandwidth, -3 dB frequencies (Hz)	Peak-to-peak amplitude (UIpp) (Note 3)
64 kbit/s (Note 1)	20 to 20 k	0.25
	3 k to 20 k	0.05
2048 kbit/s	20 to 100 k	1.5
	18 k to 100 k (Note 2)	0.2
8448 kbit/s	20 to 400 k	1.5
	3 k to 400 k (Note 2)	0.2
34 368 kbit/s	100 to 800 k	1.5
	10 k to 800 k	0.15
139 264 kbit/s	200 to 3.5 M	1.5
	10 k to 3.5 M	0.075

2.1.2 The testing model:



2.1.3 The sequence configuration:

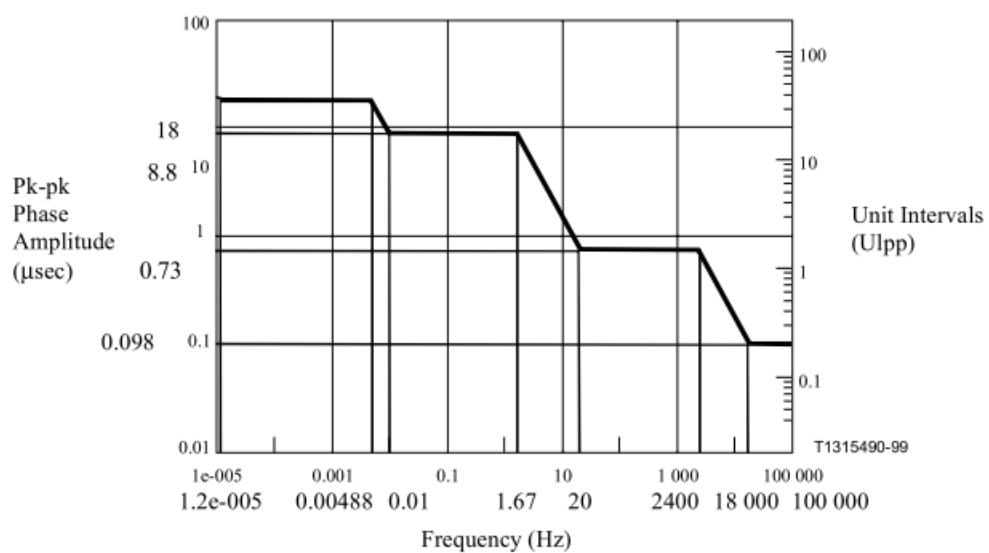
- d. Step#1: Configure data path on DUT;
- e. Step#2: [Configure Jitter function on Tester](#)
- f. Step#3: Use Tester to measure B1 and B2 value in the following cases:
 - Loop-time/System/External/ACR/DCR
 - Test with temperature range
 - Test with many payload size
 - Test with RTP timestamp rates
 - Test with PDV and None-PDV

2.2 Jitter and Wander Tolerance:

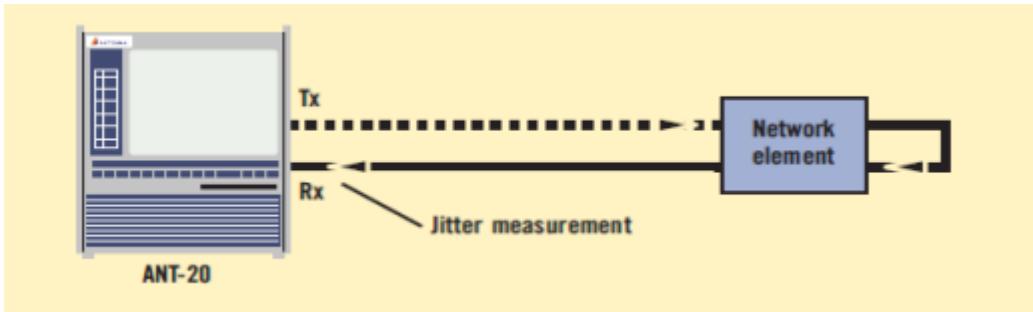
2.2.1 Standard requirements:

- c. The jitter tolerance for E1 interface **Must** follow Table-16/G823.
- d. The wander tolerance is basically like the Jitter Tolerance test, except that wander is a long-term phenomenon.

Frequency f (Hz)	Requirement (pk-pk phase amplitude)
$12 \mu < f \leq 4.88$ m	$18 \mu\text{s}$
$4.88 \text{ m} < f \leq 10 \text{ m}$	$0.088 f^{-1} \mu\text{s}$
$10 \text{ m} < f \leq 1.67$	$8.8 \mu\text{s}$
$1.67 < f \leq 20$	$15 f^{-1} \mu\text{s}$
$20 < f \leq 2.4 \text{ k}$ (Note 1)	1.5 UI
$2.4 \text{ k} < f \leq 18 \text{ k}$ (Note 1)	$3.6 \times 10^3 f^{-1} \text{ UI}$
$18 \text{ k} < f \leq 100 \text{ k}$ (Note 1)	0.2 UI
NOTE 1 – For 2048 kbit/s interfaces within the network of an operator, the frequencies may be specified as 93 Hz (instead of 2.4 kHz) and 700 Hz (instead of 18 kHz). However, at interfaces between different operator networks, the values in the table apply, unless involved parties agree otherwise.	
NOTE 2 – 1 UI = 488 ns.	



2.2.2 The testing model:



2.2.3 The sequence configuration

- d. Step#1: configure data path on DUT and start Jitter Tolerance function on Tester
- e. Step#2:configure Jitter Tolerance Mask on Tester
- f. Step#3: start measure Jitter Tolerance for the following cases. After Tester finished, save result
 - Loop-time/System/External/ACR/DCR
 - Test with temperature range
 - Test with many payload size
 - Test with RTP timestamp rates
 - Test with PDV and None-PDV

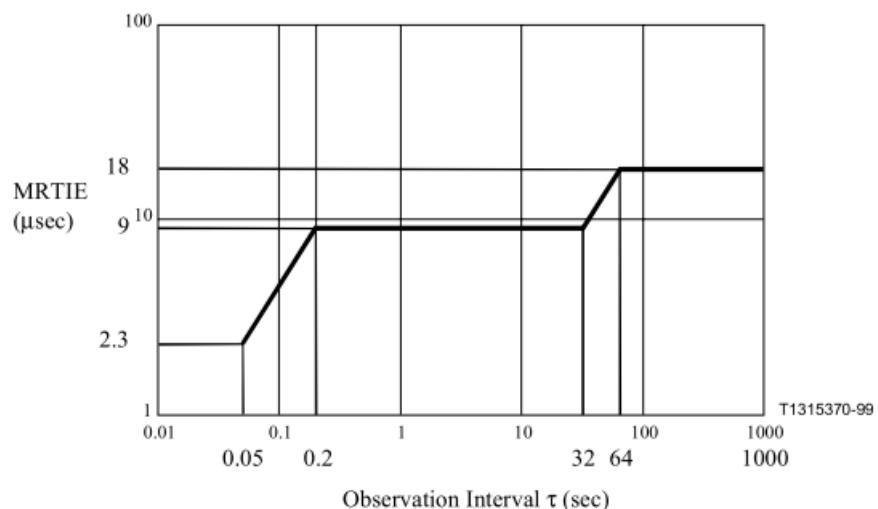
2.3 Wander generation:

2.3.1 Standard requirement:

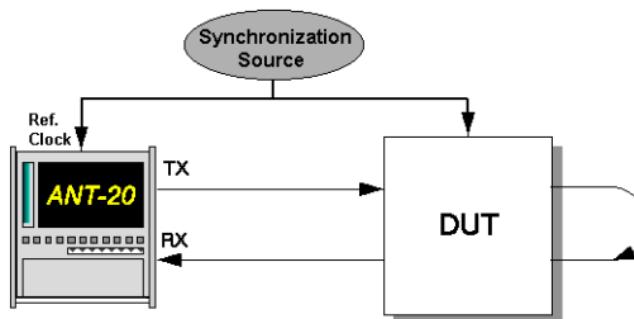
The maximum level of wander that may exist at a 2048 kbit/s network interface, expressed in MRTIE, shall not exceed the limit given in table below

Observation Interval τ (sec)	MRTIE requirement (μ s)
$0.05 < \tau \leq 0.2$	46τ
$0.2 < \tau \leq 32$	9
$32 < \tau \leq 64$	0.28τ
$64 < \tau \leq 1\,000$ (Note)	18

NOTE – For the asynchronous configuration (refer to Figure B.1), the maximum observation interval to be considered is 80 seconds.



2.3.2 The testing model:



2.3.3 Test wander None-PDV for one channel:

- g. Step#1: Configure data path on DUT with the following cases:
 - ACR mode
 - DCR mode (enable RTP in this case)
- h. Step#2: [Configure wander function on Tester](#).
- i. Step#3: Start wander to check Locking time (in worst case, Locking time is around 15 minutes)
- j. Step#4: After check Locking time, get result and compare with G.823 mask
- k. Step#5: Restart Tester to measure wander around 1 hour
- l. Step#6: [Stop wander, get result and compare with G.824 mask](#)

2.3.4 Test wander None-PDV for multi-channels:

Refer the steps in section.1.3.3 with configuration is multi-channels.

2.3.5 Test Phase Transient:

At the network interface, during phase transients (typically due to network synchronization rearrangements), phase deviation shall not exceed 1us, and the frequency of signal shall not be offset from nominal frequency by more than 61 ppm. Phase transient are expected to be a rare occurrence.

- f. Step#1: Configure data path on DUT:
 - ACR mode
 - DCR mode (enable RTP in this case)
- g. Step#2: Waiting for ACR/DCR was locked, start wander around 15 minutes
- h. Step#3: Unplug LIU around 15 minutes after plug LIU again.
- i. Step#4: Continuous measuring (around 15 minutes) to check Locking time and Phase Transient.
- j. Step#5: Repeat step#3 and #4 one more. Save total wander result

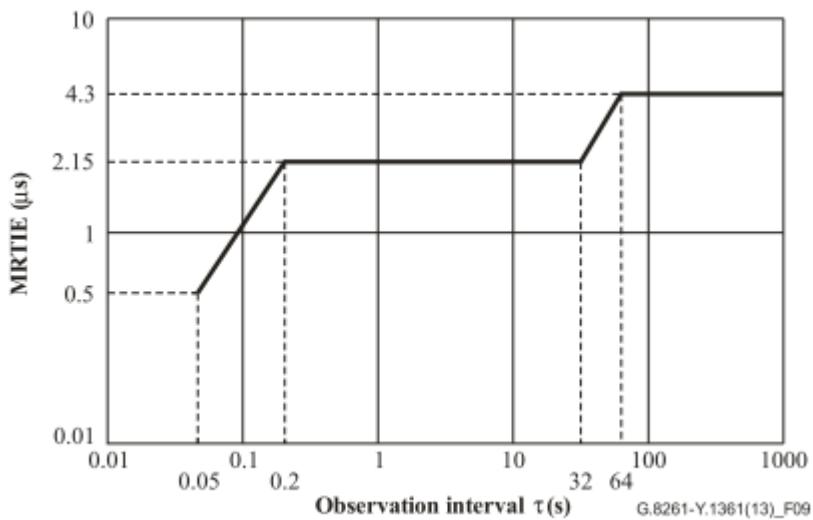
2.3.6 Measure test-case G.8261:

2.3.6.1 Standard requirement:

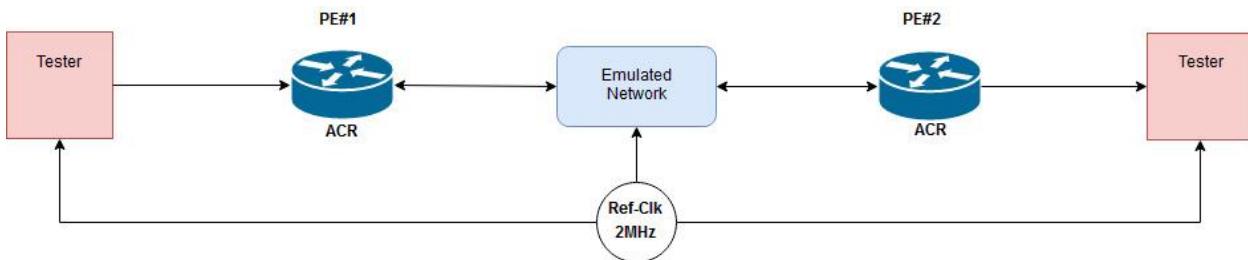
The wander budget, expressed in maximum relative time interval error, for E1 signal is defined in Table below

Observation Interval τ (s)	MRTIE requirement (μ s)
$0.05 < \tau \leq 0.2$	10.75τ
$0.2 < \tau \leq 32$	$9 \times 0.24 = 2.15$
$32 < \tau \leq 64$	0.067τ
$64 < \tau \leq 1000$	$18 \times 0.24 = 4.3$

Note that for the asynchronous configuration, the maximum observation interval to be considered is 80 s.
The specification between 80 s and 1000 s for the asynchronous interfaces is for further study.



2.3.6.2 Test-cases for ACR mode:



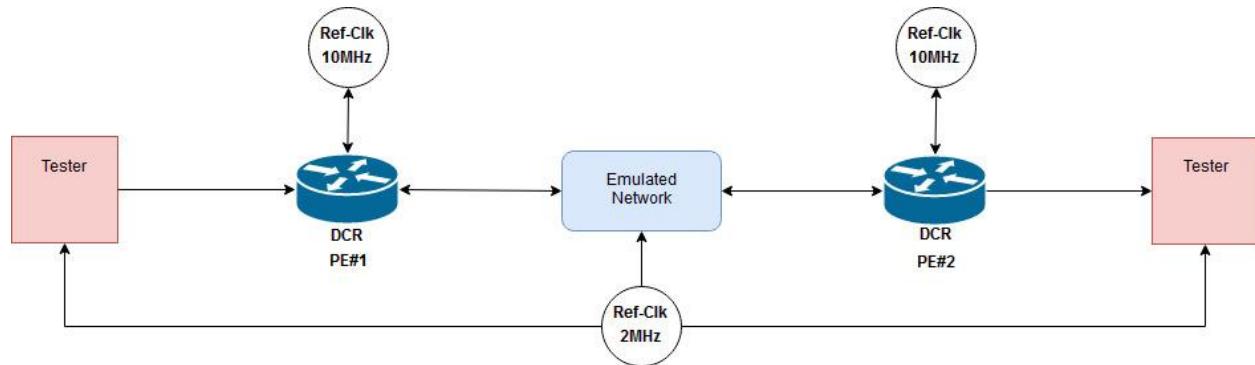
2.3.6.2.1 Test-case #1:

- e. Step#1: Configure data DS1 on DUT (only one channel) with ACR mode
- f. Step#2: Start Test-case #1 on ANUE Tester.
- g. Step#3: Waiting for ACR was locked, restart Tester to measure wander for Test-case #1
- h. Step#4: After Test-case#1 finished (check on ANUE), stop ANUE and save TIE data result to compare with mask above.

2.3.6.2.2 Test-case #2, #3, #4, #5, #6, #7, #8:

Refer steps in section 1.3.6.2.1 to measure Test-case #2, #3, #4, #5, #6, #7, #8.

2.3.6.3 Test-cases for DCR mode:



2.3.6.3.1 Test-case #9:

- e. Step#1: Configure data path DS1 on DUT (only one channel) with DCR mode
- f. Step#2: Start Test-case #9 on ANUE Tester
- g. Step#3: Waiting for DCR was locked, restart Tester to measure wander for Test-case #9
- h. Step#4: After Test-case #9 finished (Check on ANUE), stop ANUE and save TIE data to compare with mask above.

2.3.6.3.2 Test-case #10, #11:

Refer steps in section 1.3.6.3.1 to measure Test-case #10, #11

3 Requirements for DS3 Network Interface:

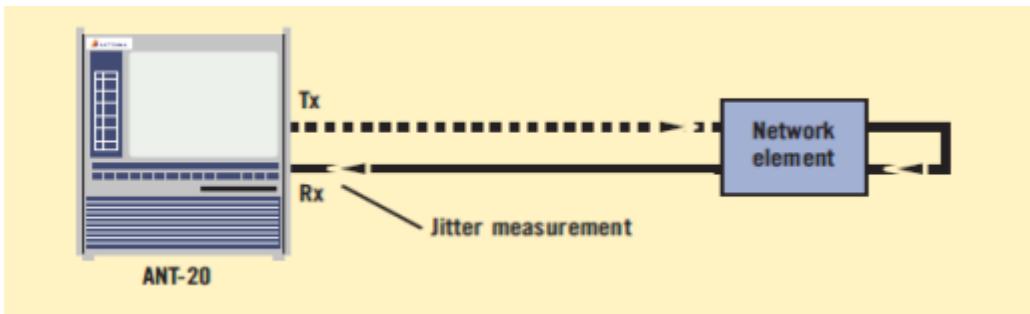
3.1 Jitter Generation:

3.1.1 Standard requirement:

Jitter output of DS3 signal at any network interface **Must** not exceed corresponding value in the table below

Bit Rate (Mb/s)	Network Jitter Limits (UI _{pp}) ^a		Measurement Filter Cutoff Frequencies		
	B ₁ (F ₁ to F ₄)	B ₂ (F ₃ to F ₄)	Lower Cutoff, F ₁	Lower Cutoff, F ₃	Minimum Upper Cutoff, F ₄
1.544	5	0.1	10 Hz	8 kHz	40 kHz
3.152	5	0.1	10 Hz	1.5 kHz	40 kHz
6.312	3	0.1	10 Hz	3 kHz	60 kHz
44.736	5	0.1	10 Hz	30 kHz	400 kHz

3.1.2 The testing model:



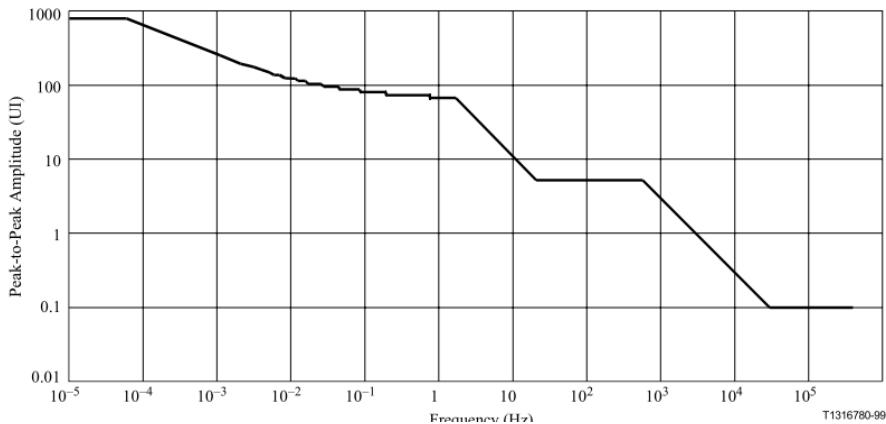
3.1.3 The sequence configuration:

- Step#1: Configure data path on DUT and start Jitter function on Tester
- Step#2: Use Tester to measure B1 and B2 value. Refer table above

3.2 Jitter and Wander Tolerance:

3.2.1 Standard requirements:

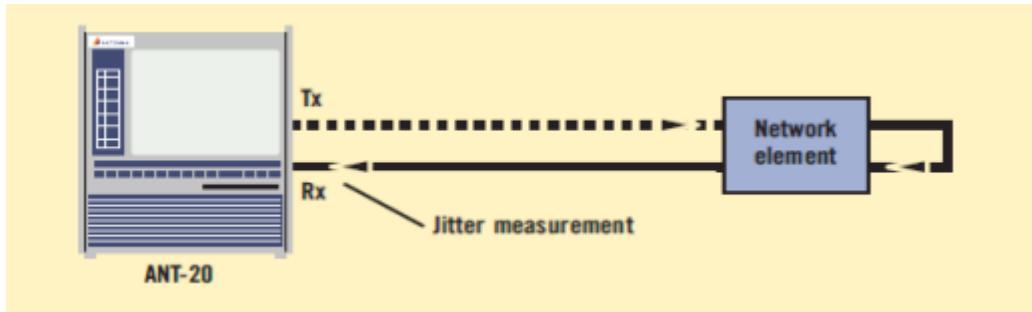
- The jitter tolerance for DS3 interface **Must** follow Table-8/G824.
- The wander tolerance is basically like the Jitter Tolerance test, except that wander is a long-term phenomenon.



Frequency f (Hz)	Peak-to-Peak Amplitude (UI)
$1.2 \times 10^{-5} \leq f \leq 6.12 \times 10^{-5}$	805 (18 μ s) (Note)
$6.12 \times 10^{-5} < f \leq 1.675$	$62.6 + 5.81 f^{-1/2}$ ($1.4 + 0.130 f^{-1/2}$ μ s)
$1.675 < f \leq 21.9$	$110 f^{-1}$ ($2.45 f^{-1}$ μ s)
$21.9 < f \leq 600$	5 (0.112 μ s)
$600 < f \leq 30\,000$	$3000 f^{-1}$ ($67.1 f^{-1}$ μ s)
$30\,000 < f \leq 400\,000$	0.1 (2.24×10^{-3} μ s)

NOTE – The value 18 μ s represents a relative phase deviation between the incoming signal and the internal local timing signal derived from the reference clock. An example of a reference configuration explaining the 18 μ s value is given in Annex A.

3.2.2 The testing model:



3.2.3 The sequence configuration

- Step#1: configure data path on DUT and start Jitter Tolerance function on Tester
- Step#2: configure Jitter Tolerance Mask on Tester
- Step#3: start measure Jitter Tolerance. After Tester finished, save result

3.3 Wander generation:

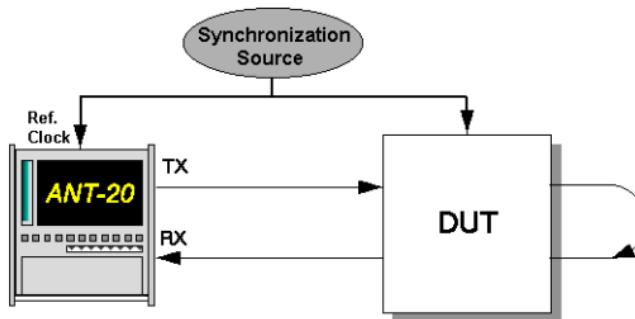
3.3.1 Standard requirement:

The wander of a 44736 Kbit/s network signal shall not exceed the MTIE limits given in table 3

Table 3/G.824 – Wander limit for 44 736 kbit/s network interface

Observation interval τ in seconds	MRTIE (τ) in ns
$0.1 < \tau \leq 0.195$	7700τ
$0.195 < \tau \leq 5200$	$1400 + 230 \tau^{0.5}$
$5200 < \tau$	18 000

3.3.2 The testing model:



3.3.3 Test wander None-PDV for one channel:

- Step#1: Configure data path with ACR or DCR mode on DUT; configure wander function on Tester.
- Step#2: Start wander to check Locking time (in worst case, Locking time is around 15 minutes)
- Step#3: After check Locking time, get result and compare with G.824 mask.
- Step#4: Restart Tester to measure wander around 1 hour
- Step#5: Stop wander , get result and compare with G.824 mask

3.3.4 Test wander None-PDV for multi-channels:

Refer the steps in section 2.3.3 with configuration is multi-channels.

3.3.5 Test Phase Transient:

At the network interface, during phase transients (typically due to network synchronization rearrangements), phase deviation shall not exceed 1us, and the frequency of signal shall not be offset from nominal frequency by more than 61 ppm. Phase transient are expected to be a rare occurrence.

- a. Step#1: Configure data path with ACR or DCR mode on DUT
- b. Step#2: Waiting for ACR/DCR was locked, start wander around 15 minutes
- c. Step#3: Unplug LIU around 15 minutes after plug LIU again.
- d. Step#4: Continuous measuring (around 15 minutes) to check Locking time and Phase Transient.
- e. Step#5: Repeat step#3 and #4 one more. Save total wander result

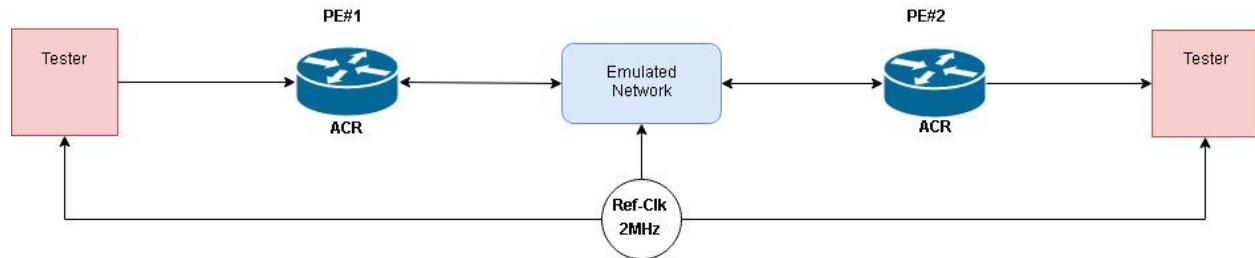
3.3.6 Measure test-case G.8261:

3.3.6.1 Standard requirement:

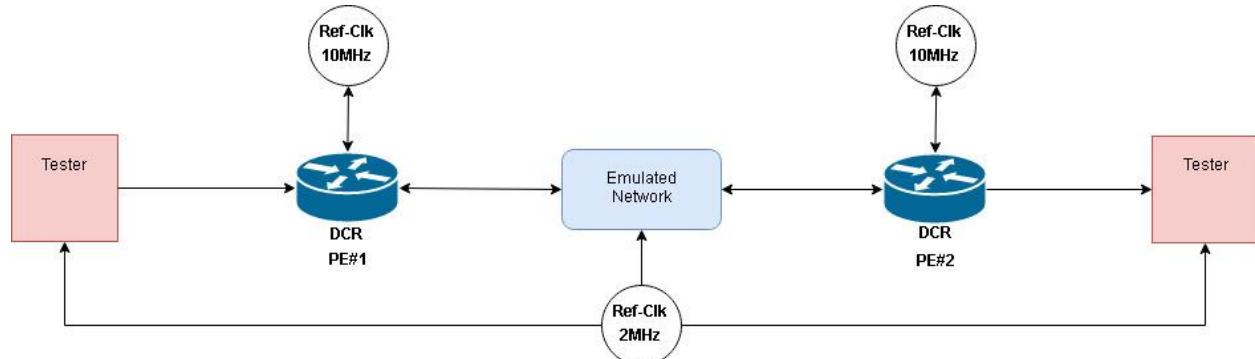
The network limits for DS3, E3 carried over the CES segments are for further study. Therefore, we will use Table 3/G.824

3.3.6.2 The testing model:

3.3.6.2.1 Testing model for ACR:



3.3.6.2.2 Testing model for DCR:



3.3.6.3 Test-cases for ACR mode:

3.3.6.3.1 Test-case #1:

- i. Step#1: Configure data path with ACR mode on DUT (only one channel)
- j. Step#2: Start Test-case #1 on ANUE Tester.
- k. Step#3: Waiting for ACR was locked, restart Tester to measure wander for Test-case #1
- l. Step#4: After Test-case#1 finished (check on ANUE), stop ANUE and save TIE data to compare with mask above.

3.3.6.3.2 Test-case #2, #3, #4, #5, #6, #7, #8:

Refer steps in section 2.3.6.3.1 to measure Test-case #2, #3, #4, #5, #6, #7, #8.

3.3.6.4 Test-cases for DCR mode:

3.3.6.4.1 Test-case #9:

- i. Step#1: Configure data path with DCR mode on DUT (only one channel)
- j. Step#2: Start Test-case #9 on ANUE Tester
- k. Step#3: Waiting for DCR was locked, restart Tester to measure wander for Test-case #9
- l. Step#4: After Test-case #9 finished (Check on ANUE), stop ANUE and save TIE data to compare with mask above.

3.3.6.4.2 Test-case #10, #11:

Refer steps in section 2.3.6.4.1 to measure Test-case #10, #11

4 Requirements for E3 Network Interface:

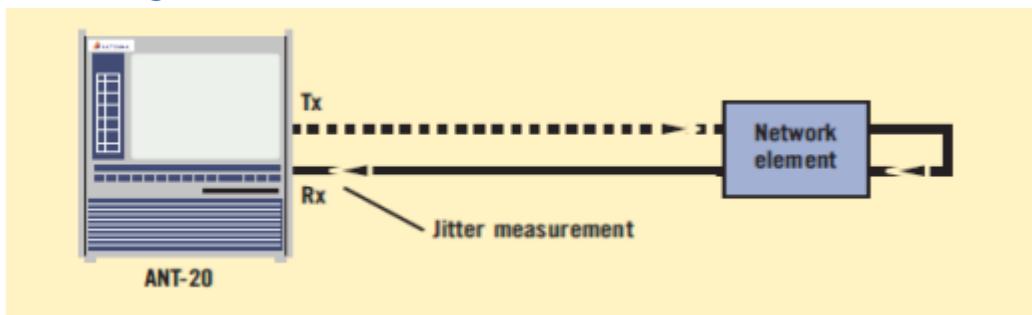
4.1 Jitter Generation:

4.1.1 Standard requirement:

Jitter output of DS3 signal at any network interface **Must** not exceed corresponding value in the table below

Interface	Measurement bandwidth, -3 dB frequencies (Hz)	Peak-to-peak amplitude (UIpp) (Note 3)
64 kbit/s (Note 1)	20 to 20 k	0.25
	3 k to 20 k	0.05
2048 kbit/s	20 to 100 k	1.5
	18 k to 100 k (Note 2)	0.2
8448 kbit/s	20 to 400 k	1.5
	3 k to 400 k (Note 2)	0.2
34 368 kbit/s	100 to 800 k	1.5
	10 k to 800 k	0.15
139 264 kbit/s	200 to 3.5 M	1.5
	10 k to 3.5 M	0.075

4.1.2 The testing model:



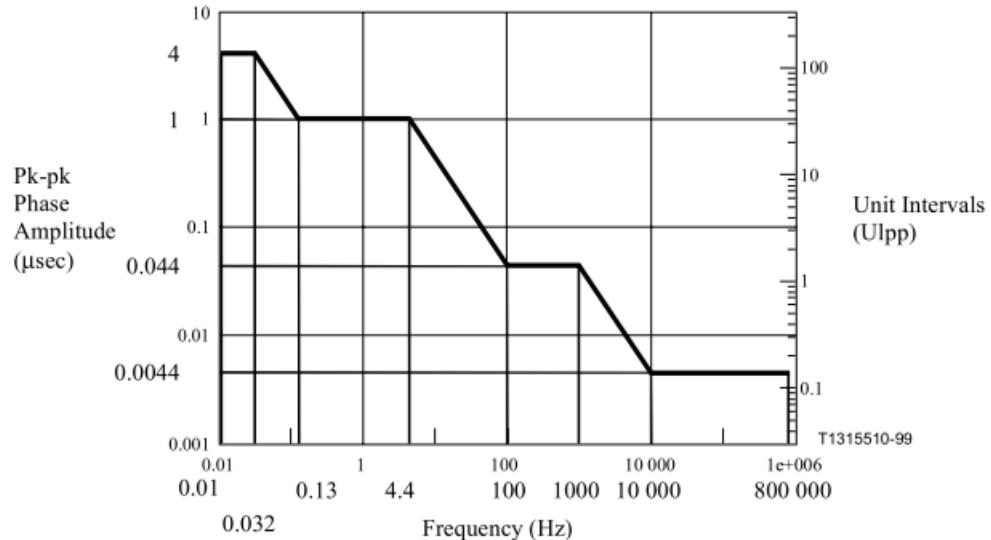
4.1.3 The sequence configuration:

- c. Step#1: Configure data path on DUT and start Jitter function on Tester
- d. Step#2: Use Tester to measure B1 and B2 value. Refer table above

4.2 Jitter and Wander Tolerance:

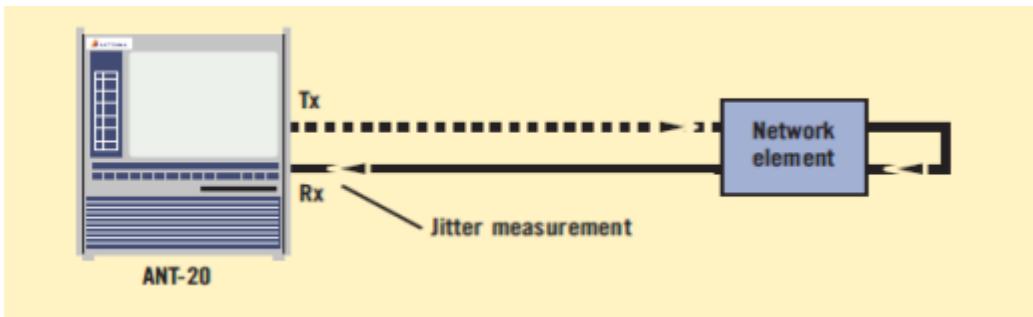
4.2.1 Standard requirements:

- c. The jitter tolerance for DS3 interface **Must** follow G823.
- d. The wander tolerance is basically like the Jitter Tolerance test, except that wander is a long-term phenomenon.



Frequency f (Hz)	Requirement (pk-pk phase amplitude)
$10 \text{ m} < f \leq 32 \text{ m}$	$4 \mu\text{s}$
$32 \text{ m} < f \leq 130 \text{ m}$	$0.13 f^{-1} \mu\text{s}$
$130 \text{ m} < f \leq 4.4$	$1 \mu\text{s}$
$4.4 < f \leq 100$	$4.4 f^{-1} \mu\text{s}$
$100 < f \leq 1 \text{ k}$	1.5 UI
$1 \text{ k} < f \leq 10 \text{ k}$	$1.5 \times 10^3 f^{-1} \text{ UI}$
$10 \text{ k} < f \leq 800 \text{ k}$	0.15 UI
NOTE – 1 UI = 29.1 ns.	

4.2.2 The testing model:



4.2.3 The sequence configuration

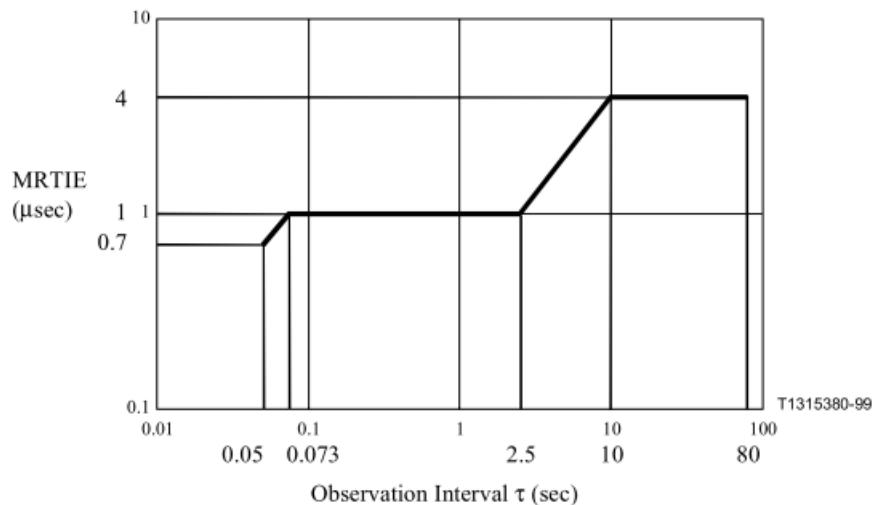
- d. Step#1: configure data path on DUT and start Jitter Tolerance function on Tester
- e. Step#2: configure Jitter Tolerance Mask on Tester
- f. Step#3: start measure Jitter Tolerance. After Tester finished, save result

4.3 Wander generation:

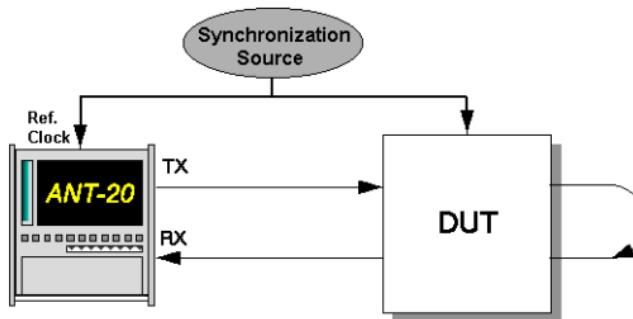
4.3.1 Standard requirement:

The maximum level of wander that may exist at a 34368 kbit/s network interface, expressed in MRTIE, shall not exceed the limit given in table below

Observation Interval τ (sec)	MRTIE requirement (μ s)
$0.05 < \tau \leq 0.073$	14τ
$0.073 < \tau \leq 2.5$	1
$2.5 < \tau \leq 10$	0.4τ
$10 < \tau \leq 80$	4



4.3.2 The testing model:



4.3.3 Test wander None-PDV for one channel:

- f. Step#1: Configure data path with ACR or DCR mode on DUT; configure wander function on Tester.
- g. Step#2: Start wander to check Locking time (in worst case, Locking time is around 15 minutes)
- h. Step#3: After check Locking time, get result and compare with G.823 mask.
- i. Step#4: Restart Tester to measure wander around 1 hour
- j. Step#5: Stop wander , get result and compare with G.823 mask

4.3.4 Test wander None-PDV for multi-channels:

Refer the steps in section.2.3.3 with configuration is multi-channels.

4.3.5 Test Phase Transient:

At the network interface, during phase transients (typically due to network synchronization rearrangements), phase deviation shall not exceed 1us, and the frequency of signal shall not be offset from nominal frequency by more than 61 ppm. Phase transient are expected to be a rare occurrence.

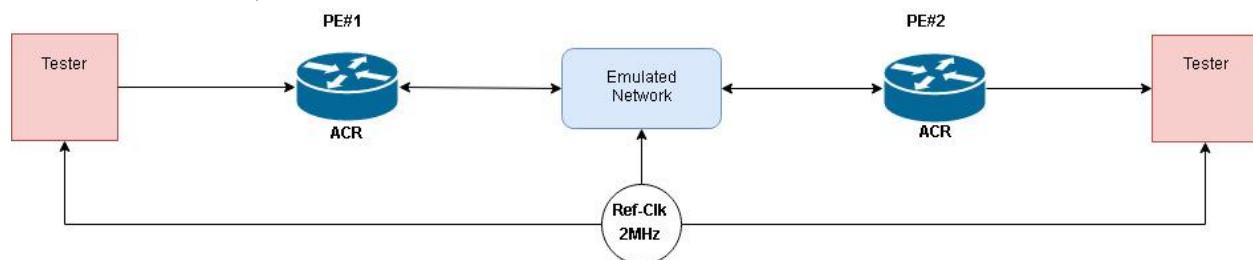
- f. Step#1: Configure data path with ACR or DCR mode on DUT
- g. Step#2: Waiting for ACR/DCR was locked, start wander around 15 minutes
- h. Step#3: Unplug LIU around 15 minutes after plug LIU again.
- i. Step#4: Continuous measuring (around 15 minutes) to check Locking time and Phase Transient.
- j. Step#5: Repeat step#3 and #4 one more. Save total wander result

4.3.6 Measure test-case G.8261:

4.3.6.1 Standard requirement:

The network limits for DS3, E3 carried over the CES segments are for further study. Therefore, we will use Table 3/G.824

4.3.6.2 Test-cases for ACR mode:



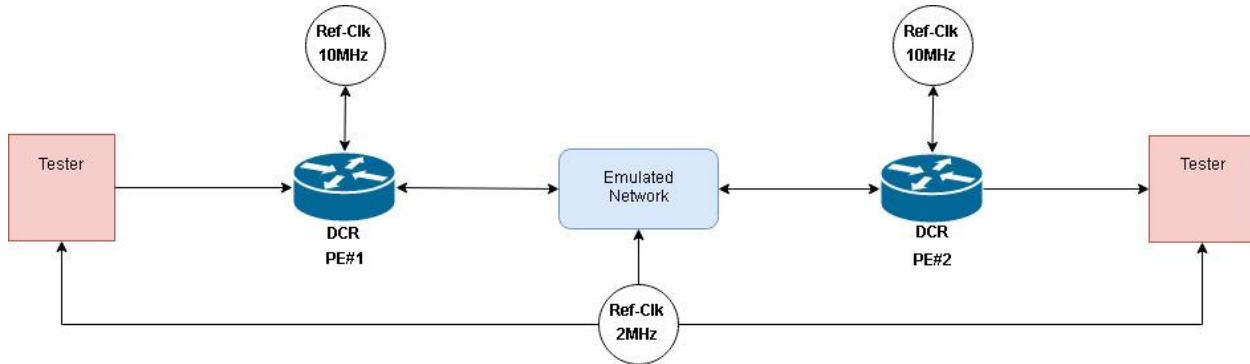
4.3.6.2.1 Test-case #1:

- m. Step#1: Configure data path with ACR mode on DUT (only one channel)
- n. Step#2: Start Test-case #1 on ANUE Tester.
- o. Step#3: Waiting for ACR was locked, restart Tester to measure wander for Test-case #1
- p. Step#4: After Test-case#1 finished (check on ANUE), stop ANUE and save TIE data to compare with mask above.

4.3.6.2.2 Test-case #2, #3, #4, #5, #6, #7, #8:

Refer steps in section 2.3.6.3.1 to measure Test-case #2, #3, #4, #5, #6, #7, #8.

4.3.6.3 Test-cases for DCR mode:



4.3.6.3.1 Test-case #9:

- m. Step#1: Configure data path with DCR mode on DUT (only one channel)
- n. Step#2: Start Test-case #9 on ANUE Tester
- o. Step#3: Waiting for DCR was locked, restart Tester to measure wander for Test-case #9
- p. Step#4: After Test-case #9 finished (Check on ANUE), stop ANUE and save TIE data to compare with mask above.

4.3.6.3.2 Test-case #10, #11:

Refer steps in section 2.3.6.4.1 to measure Test-case #10, #11

5 Requirements for STM-N/OC-X Network Interface:

5.1 Jitter Generation:

5.1.1 Standard requirement:

Jitter output of signal at any network interface **Must** not exceed corresponding value in the tables below

- GR-253

OC-N/STS-N Level	B ₁	B ₂	B ₃	A ₁ (UI _{pp})	A ₂ (UI _{pp})
1	100 Hz	20 kHz	400 kHz	1.5	0.15
3	500 Hz	65 kHz	1.3 MHz	1.5	0.15
12	1 kHz	250 kHz	5 MHz	1.5	0.15
48	5 kHz	1 MHz	20 MHz	1.5	0.15
48(B)	5 kHz	12 kHz	20 MHz	1.5	0.15
192	20 kHz	4 MHz	80 MHz	1.5	0.15
768 ^a	20 kHz	16 MHz	320 MHz	6.0	0.15

5.1.1.1 Category I Mapping Jitter

To measure the mapping jitter it is necessary for the system to be configured so that no STS or VT pointer adjustments occur during the tests.

For a Category I DS1 or DS3 interface, the mapping jitter generation shall be less than the value given in Table 5-12.

Table 5-12 Category I Mapping Jitter Limits

Interface	Jitter (UI _{pp})
DS1	0.70
DS3	0.40

5.1.1.2 Category I Jitter Generation Due to Single Pointer Adjustments

The jitter appearing at a Category I DS_n interface shall be less than the corresponding value in Table 5-14 when the pointer test sequence in Figure 5-30 is applied.

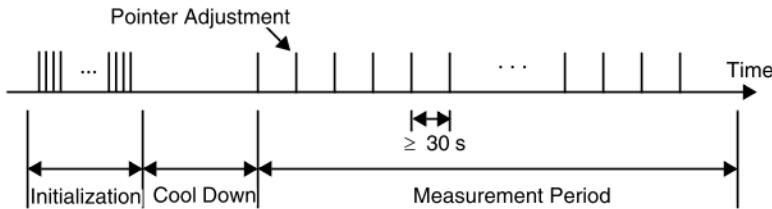
Table 5-14 Jitter Due to Single Pointer Adjustments

SPE/Payload	Jitter (UI _{pp})
VT1.5/DS1	$A_0 + 0.60^1$
VT2/DS1A	Under Study
VT3/DS1C	Under Study
VT6/DS2	Under Study
STS-1/DS3	$A_0 + 0.30^1$
STS-3c/DS4NA	Under Study

Note:

1 A_0 is the mapping jitter generated by the NE under test.

Figure 5-30 Single Pointer Adjustment Test Sequence

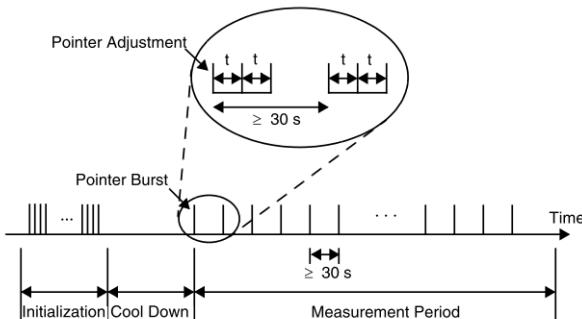


5.1.1.3 Category I Jitter Generation Due to Bursts of Pointer Adjustments

Jitter generation criteria for bursts of pointer adjustments are currently specified **only for DS3** interfaces.

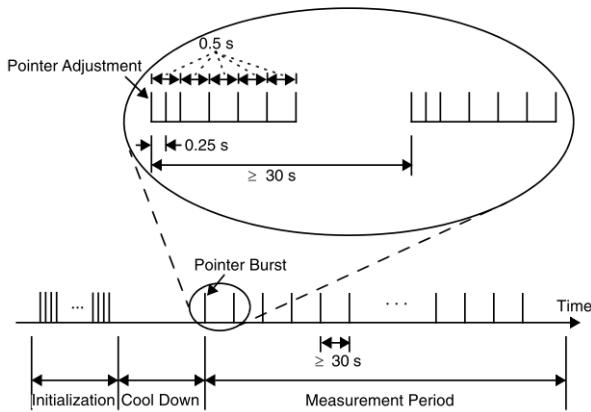
The jitter appearing at a Category I DS3 interface shall be less than 1.3 UI_{pp} when the pointer test sequence described in Figure 5-31 is applied.

Figure 5-31 Maximum Rate Pointer Burst Test Sequence



The jitter appearing at a Category I DS3 interface shall be less than 1.2 UI_{pp} when the pointer test sequence described in Figure 5-32 is applied.

Figure 5-32 Phase Transient Pointer Burst Test Sequence



5.1.1.4 Category I Jitter Generation Due to Periodic Pointer Adjustments

The jitter appearing at a Category I DS1 or DS3 interface shall be less than the corresponding value given in Table 5-15 when the pointer test sequences described in Figures 5-33, 5-34 and 5-35 are applied with T in the required range.

Table 5-15 Jitter Generation Limits for Periodic Pointer Adjustment Sequences

SPE/Payload	Figure Number of Test Sequence					
	Figure 5-33b	Figures 5-33c and 5-33d	Figure 5-34b	Figures 5-34c and 5-34d	Figure 5-35b	Figures 5-35c and 5-35d
VT1.5/DS1	1.3 UI _{pp}	1.9 UI _{pp}	-	-	1.3 UI _{pp}	1.9 UI _{pp}
STS-1/DS3	-	-	1.0 UI _{pp}	1.3 UI _{pp}	1.0 UI _{pp}	1.3 UI _{pp}

Figure 5-33 Periodic VT1.5 Pointer Adjustment Test Sequence (26-1 Pattern)

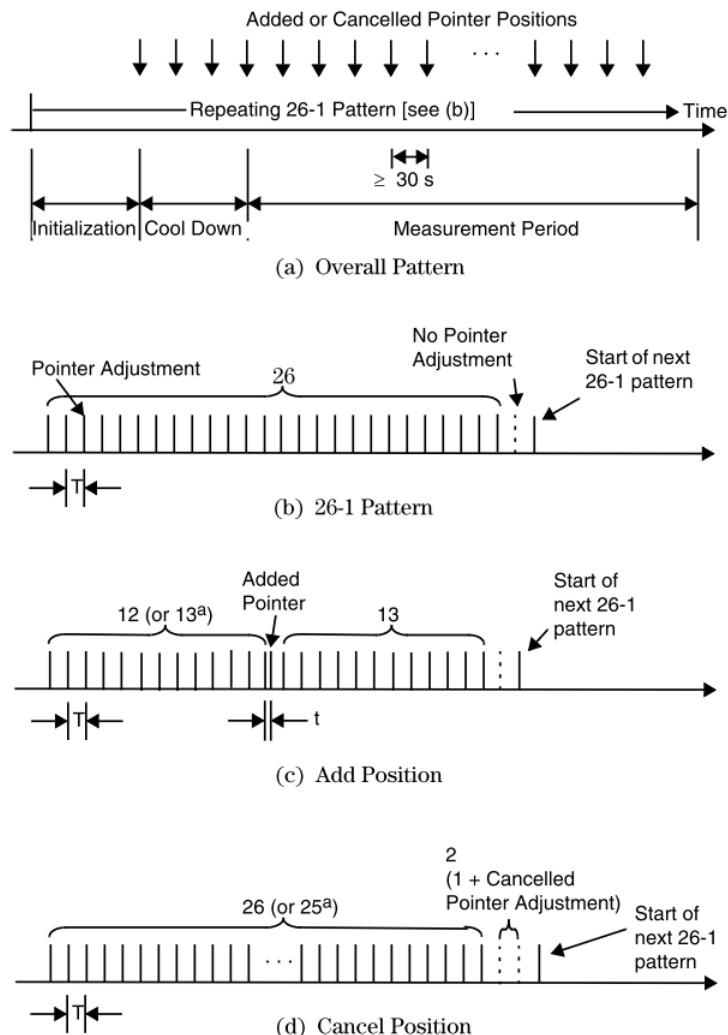


Figure 5-33 Periodic VT1.5 Pointer Adjustment Test Sequence (26-1 Pattern)

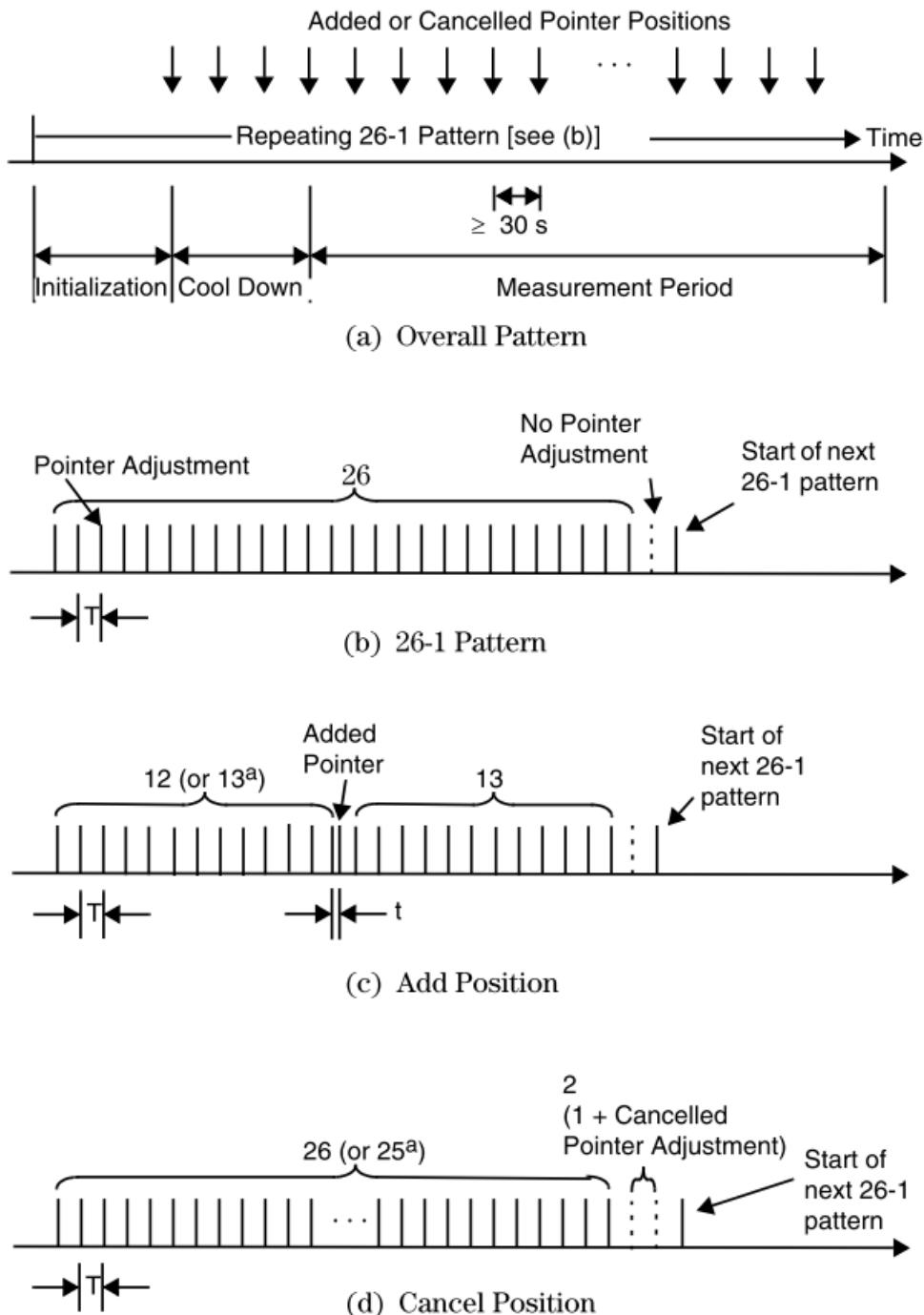


Figure 5-34 Periodic STS Pointer Adjustment Test Sequence (87-3 Pattern)

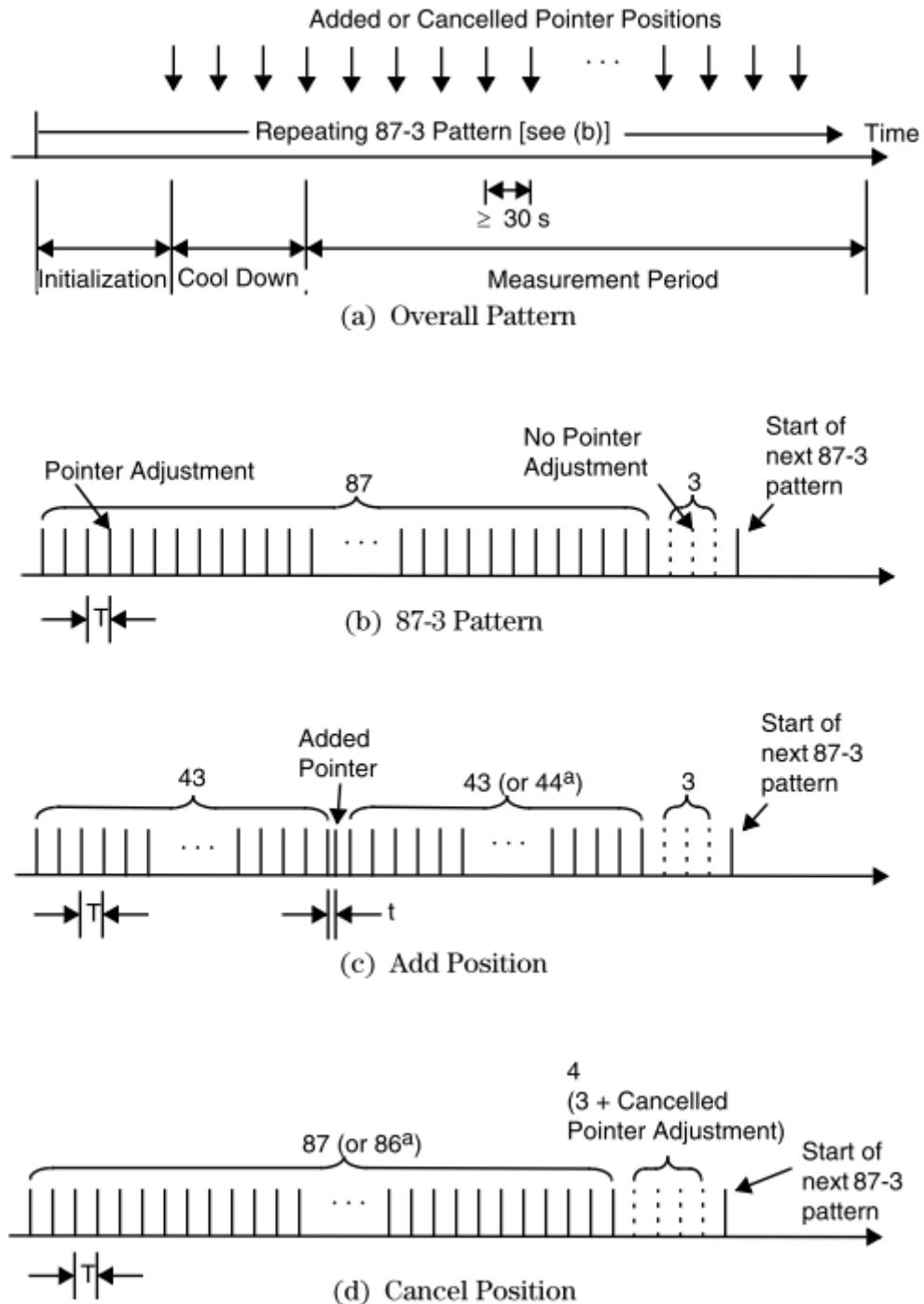
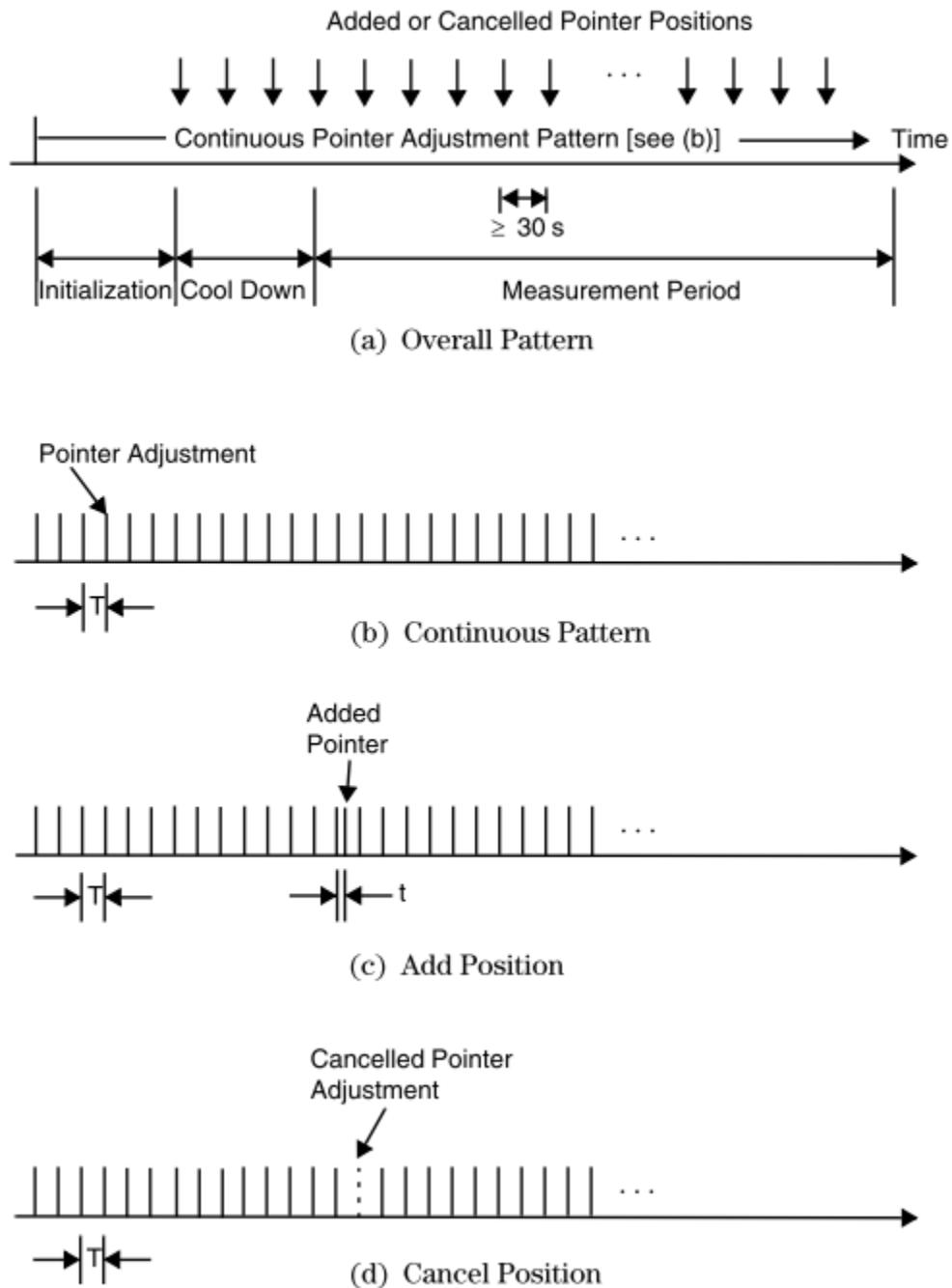
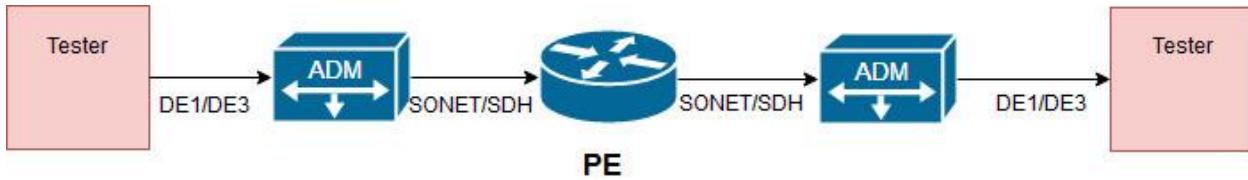


Figure 5-35 Periodic Pointer Adjustment Test Sequence (Continuous Pattern)



5.1.2 The testing model:



- Tester: use DE1 or DE3 Tester
- ADM: use HPX
- PE: use System/Looptime/ACR/DCR clock

5.1.3 The sequence configuration

- a. Step#1: Configure data path on DUT with System/Loop/ACR/DCR clock
- b. Step#2: Configure HPX (ADM) with recovery clock from SONET
- c. Step#3: Start Jitter function on Tester
- d. Step#2: Refer standard above to measure Jitter.

5.2 Jitter and Wander Tolerance:

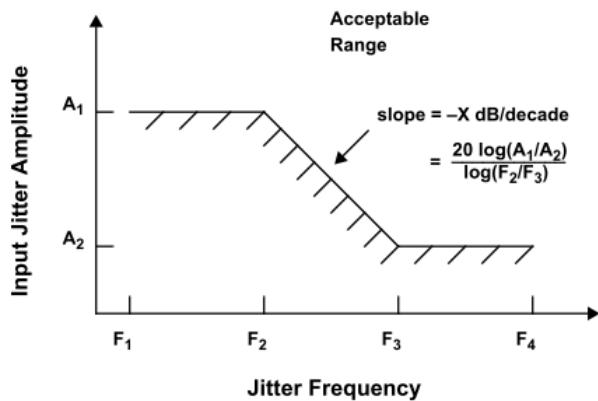
5.2.1 Standard requirements:

Input jitter tolerance is defined as the minimum amplitude of sinusoidal jitter at a given frequency that, when modulating the signal at an equipment input port, results in more than 2 errored seconds in a 30-second measurement interval. Requirements on input jitter tolerance are then given in terms of a jitter tolerance mask, which represents the minimum acceptable jitter tolerances for a specified range of jitter frequencies.

5.2.1.1 Category I Jitter Tolerance:

Category I interfaces to SONET NEs shall meet the Category I input jitter tolerance requirement in Section 7.3.1 of GR-499-CORE.

The equipment's jitter tolerance at Category I interfaces shall be greater than or equal to the jitter tolerance mask shown in Figure 7-1 (over the range of jitter frequencies indicated).



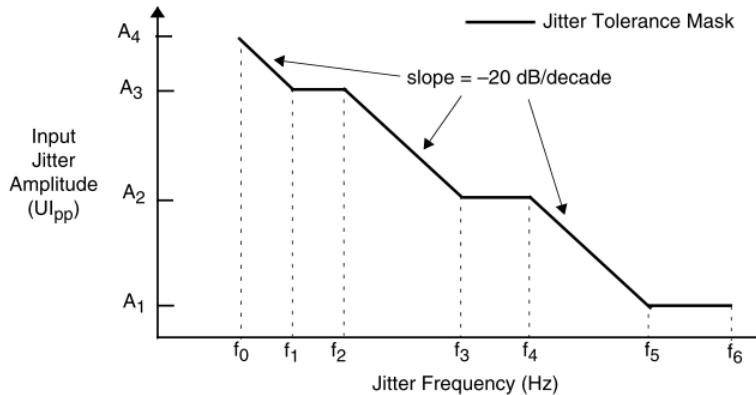
Interface Rate	A_1 (UI _{pp})	A_2 (UI _{pp})	F_1 (Hz)	F_2 (Hz)	F_3 (Hz)	F_4 (Hz)
DS1	5	0.1	10	500	8.0×10^3	40×10^3
DS1C	5	0.1	10	60	3.0×10^3	40×10^3
DS2	5	0.1	10	900	4.0×10^3	20×10^3
DS3	5	0.1	10	2.3×10^3	60×10^3	300×10^3

Figure 7-1. Input Jitter Tolerance - Category I Interfaces

5.2.1.2 Category II Jitter Tolerance:

For OC-N interfaces, jitter tolerance is defined as the maximum peak-to-peak amplitude of sinusoidal jitter applied on the input OC-N signal that causes no more than a 1-dB power penalty and does not cause any failures to be declared. This is a stress test intended to ensure that no additional penalty is incurred under operating conditions.

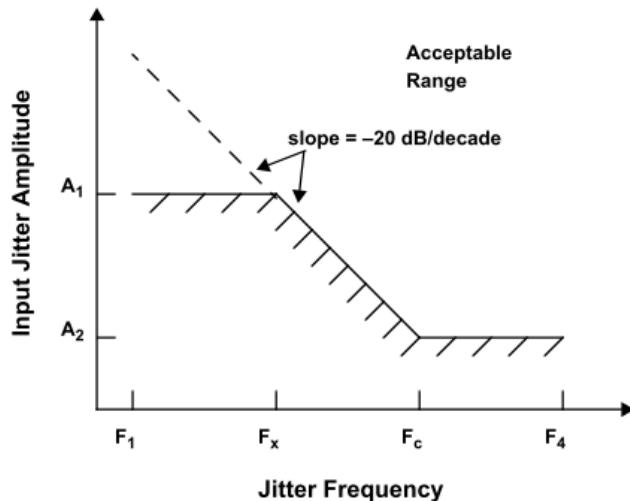
Figure 5-29 SONET Category II Jitter Tolerance Mask



OC-N/ STS-N Level	f_0 (Hz)	f_1 (Hz)	f_2 (Hz)	f_3^a (Hz)	f_4 (kHz)	f_5^a (kHz)	f_6^a (MHz)	A_4 (UI _{pp})	A_3 (UI _{pp})	A_2^a (UI _{pp})	A_1^a (UI _{pp})
1	10	NA	41.3	100	2	20	0.4	NA	3.63	1.5	0.15
3	10	NA	68.7	500	6.5	65	1.3	NA	10.9	1.5	0.15
12	10	18.5	100	1000	25	250	5.0	27.8	15	1.5	0.15
48	10	70.9	500	5000	100	1000	20	106.4	15	1.5	0.15
192	10	296	2000	20000	400	4000	80	444.6	15	1.5	0.15
768 ^b	10	1184	8000	20000	400	16000	320	1776	15	6.0	0.15

Also note that in several cases the parameter values that define the mask in **Figure 5-29** are different than those that appeared in earlier issues of GR-253. These changes were made to better align this section with the new or revised jitter tolerance specifications that appeared in the 2003 version of ANSI T1.105.03 (OC-1 through OC-192) and ITU-T Rec. G.8251 (OTU3, which is expected to be used as the basis for future STM-256/OC-768 specifications). (Appendix 4.5)

For STS-N electrical interfaces, application of the above definition is not feasible, and the jitter tolerance definition provided in Section 7 of GR-499-CORE is used instead.



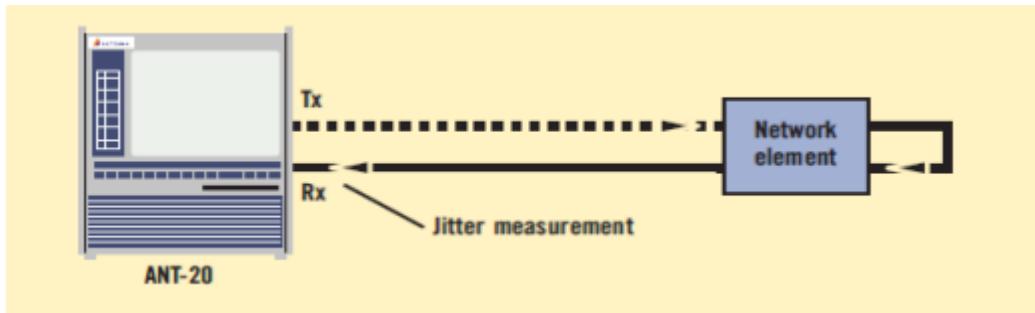
Interface Rate	A_1 (UI _{pp})	A_2 (UI _{pp})	F_1 (Hz)	F_x (Hz)	F_c (Hz)	F_4 (Hz)
DS1	10	0.3	10	192.9	6.43×10^3	40×10^3
DS1C	10	0.3	10	39.3	1.31×10^3	40×10^3
DS2	10	0.3	10	78.9	2.63×10^3	20×10^3
DS3	10	0.3	10	669	22.3×10^3	300×10^3
HR ^a	10	0.3	10	3R/200000	R/2000	Under Study

a. HR denotes any non-SONET level above DS3 whose corresponding bit rate is R.

Figure 7-2. Input Jitter Tolerance - Non-SONET Category II Interfaces

5.2.2 Jitter Tolerance for OC-x interface:

5.2.2.1 Testing model:

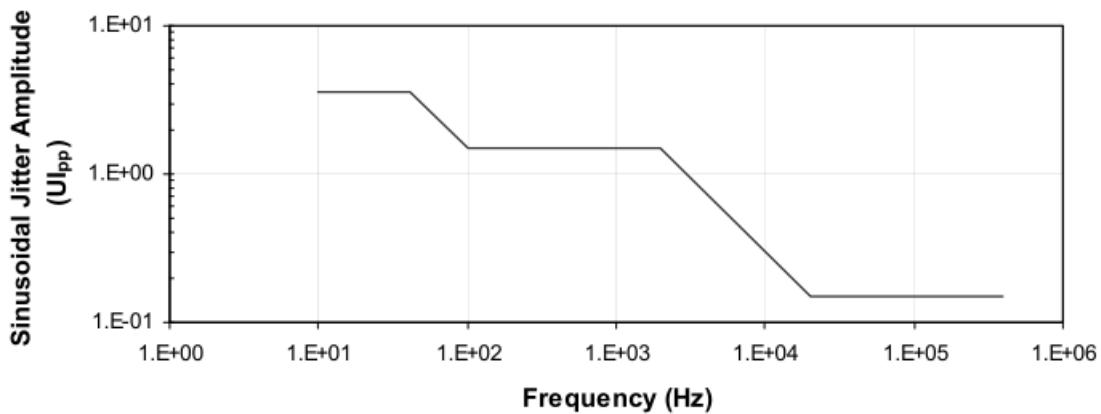


5.2.2.2 The sequence configuration

- Step#1: Configure data path on DUT with System/Loop/ACR/DCR clock
- Step#2: Start Jitter function on Tester
- Step#3: Refer standard above to measure Jitter

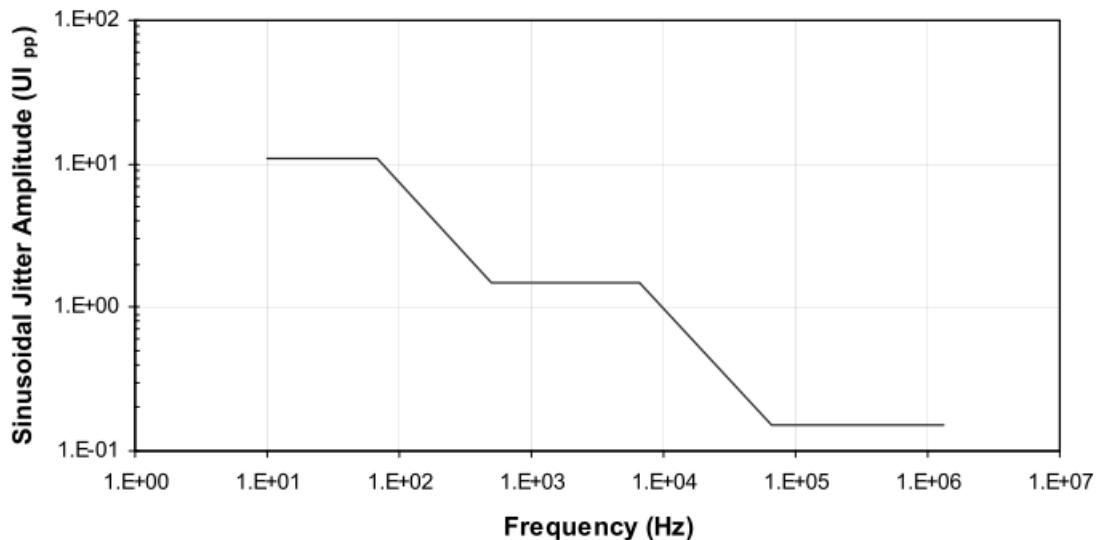
5.2.2.3 OC-1/STS-1 Jitter Tolerance

Frequency, f (Hz)	Minimum jitter tolerance (UI _{pp})
10 ≤ f ≤ 41.3	3.63 (70 ns)
41.3 < f ≤ 100	$150 \times f^{-1}$
100 < f ≤ 2.0 k	1.5
2.0 k < f ≤ 20 k	$3.0 \times 10^3 \times f^{-1}$
20 k < f ≤ 0.4 M	0.15



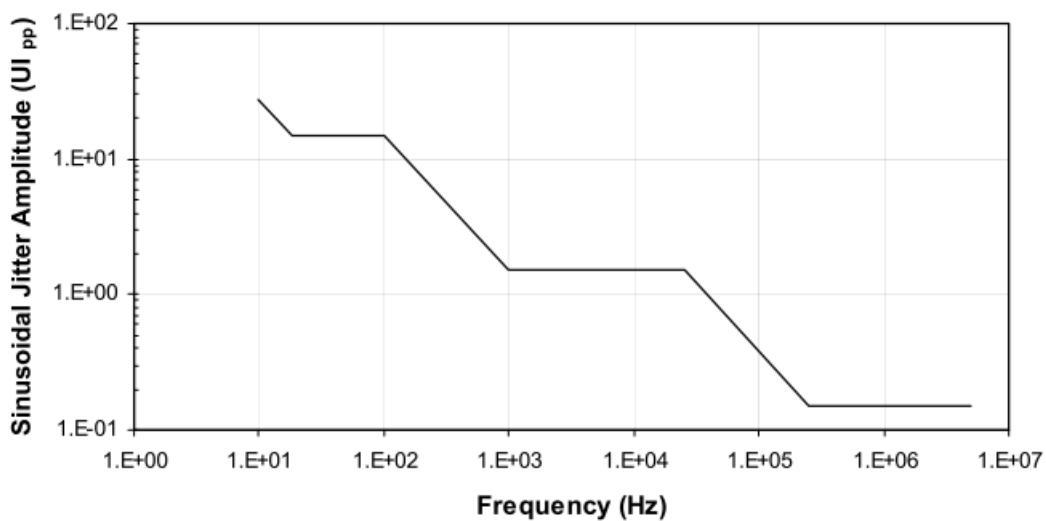
5.2.2.4 OC-3/STS-3 Jitter Tolerance

Frequency, f (Hz)	Minimum jitter tolerance (UI _{pp})
10 ≤ f ≤ 68.7	10.9 (70 ns)
68.7 < f ≤ 500	$750 \times f^{-1}$
500 < f ≤ 6.5 k	1.5
6.5 k < f ≤ 65 k	$9.8 \times 10^3 \times f^{-1}$
65 k < f ≤ 1.3 M	0.15



5.2.2.5 OC-12 Jitter Tolerance

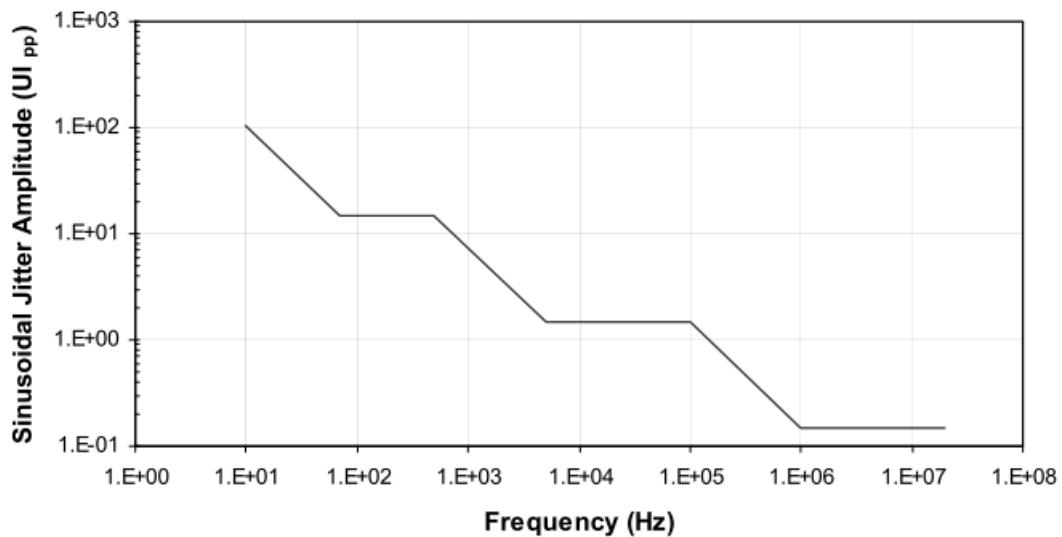
Frequency, f (Hz)	Minimum jitter tolerance (UI _{pp})
10 ≤ f ≤ 18.5	$277.5 \times f^{-1}$
18.5 < f ≤ 100	15
100 < f ≤ 1000	$1500 \times f^{-1}$
1 k < f ≤ 25 k	1.5
25 k < f ≤ 250 k	$3.8 \times 10^4 \times f^{-1}$
250 k < f ≤ 5 M	0.15



5.2.2.6 OC-48 Jitter Tolerance

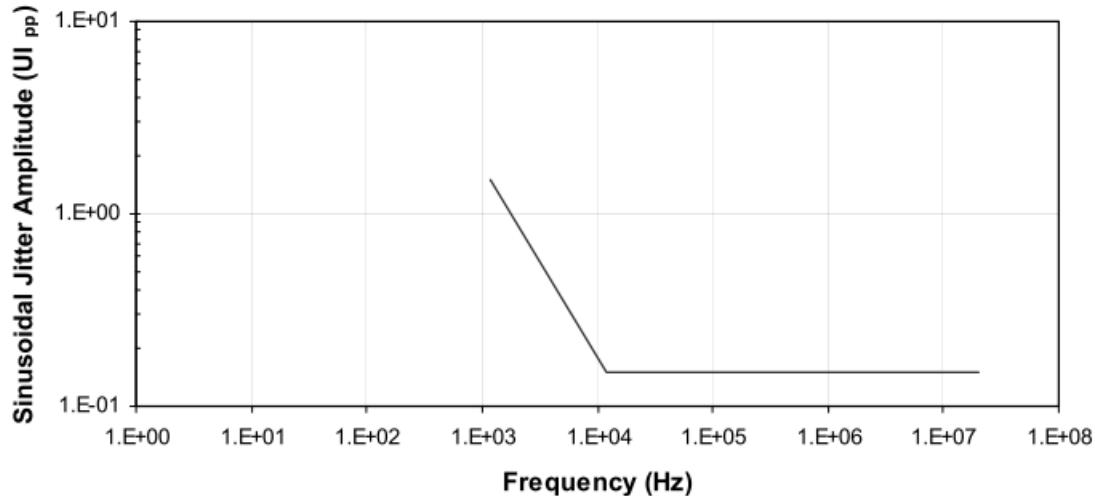
5.2.2.6.1 OC-48 Jitter Tolerance (Type A)

Frequency, f (Hz)	Minimum jitter tolerance (UI _{pp})
$10 \leq f \leq 70.9$	$1063.5 \times f^{-1}$
$70.9 < f \leq 500$	15
$500 < f \leq 5 \text{ k}$	$7500 \times f^{-1}$
$5 \text{ k} < f \leq 100 \text{ k}$	1.5
$100 \text{ k} < f \leq 1 \text{ M}$	$1.5 \times 10^5 \times f^{-1}$
$1 \text{ M} < f \leq 20 \text{ M}$	0.15



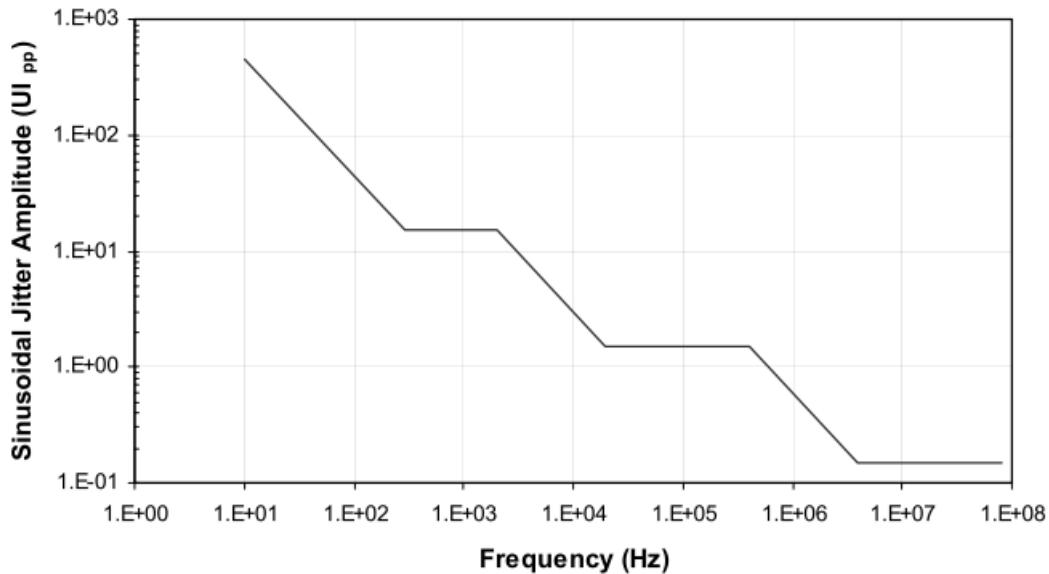
5.2.2.6.2 OC-48 Jitter Tolerance (Type B)

Frequency, f (Hz)	Minimum jitter tolerance (UI _{pp})
$1.2 \text{ k} \leq f \leq 12 \text{ k}$	$1.8 \times 10^3 f^{-1}$
$12 \text{ k} < f \leq 20 \text{ M}$	0.15



5.2.2.6.3OC-192 Jitter Tolerance

Frequency, f (Hz)	Minimum jitter tolerance (UI _{pp})
10 ≤ f ≤ 296	$4446 \times f^{-1}$
296 < f ≤ 2 000	15
2 000 < f ≤ 20 k	$3.0 \times 10^4 \times f^{-1}$
20 k < f ≤ 400 k	1.5
400 k < f ≤ 4 M	$6.0 \times 10^5 \times f^{-1}$
4 M < f ≤ 80 M	0.15



5.3 Jitter Transfer:

5.3.1 Standard requirements:

5.3.1.1 For SONET:

In SONET, Category II to Category I jitter transfer (e.g., the OC-N line jitter that appears on an asynchronous DSn output) is not expected to be significant. Therefore, this section contains only “Category I” criteria (i.e., Category I to Category I jitter transfer, such as that through a multiplexer/demultiplexer pair), and “Category II” criteria [i.e., Category II to Category II jitter transfer, such as that through a SONET regenerator or Electronic Digital Signal Cross-connect (EDSX)].

5.3.1.1.1 Category I Jitter Transfer:

For Category I DS1 and DS3 interfaces, the jitter transfer function shall be under the mask

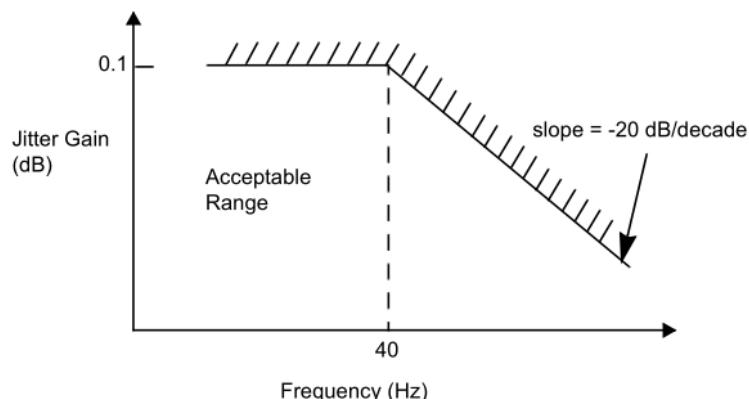


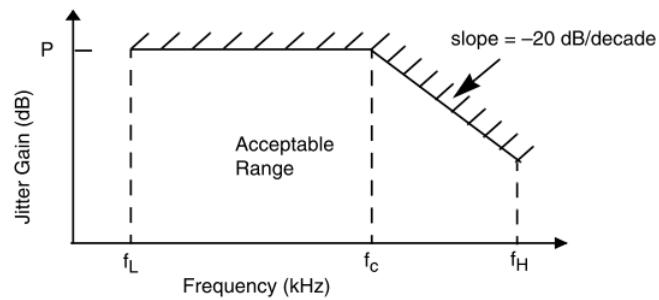
Figure 5-26. Category I DS1 and DS3 Jitter Transfer Mask

5.3.1.1.2 Category II Jitter Transfer:

The jitter transfer requirement in this section limits the amount of jitter on an input OC-N or STS-N electrical signal that can be transferred to the output OC-N or STS-N electrical signal. As noted, jitter transfer is primarily of concern within two decades or less of the breakpoint in the jitter transfer mask. This is reflected in the values of f_L and f_H that appear in **Figure 5-28** and limit the jitter frequency range over which the following requirement applies. In particular, each value of f_L is a factor of 100 less than the breakpoint frequency (f_c), and each value of f_H is either 10 or 80 times larger than f_c (and in all cases is equal to B_3 from the network interface jitter limits given).

For Category II interfaces, the jitter transfer function shall be under the mask.

Figure 5-28 Category II Jitter Transfer Mask

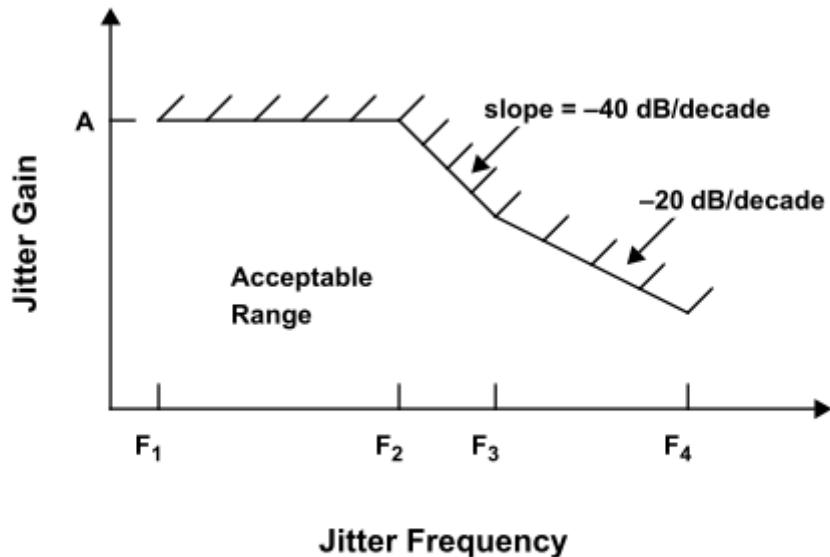


OC-N/STS-N Level	f_L (kHz)	f_c (kHz)	f_H (MHz)	P (dB)
1	0.4	40	0.4	0.1
3	1.3	130	1.3	0.1
12	5	500	5	0.1
48	20	2000	20	0.1
192	10	1000	80	0.1
768 ^a	40	4000	320	0.1

5.3.1.2 For none-SONET:

The jitter transfer requirements cover the transfer of sinusoidal jitter applied to an input port, which can be at either a Category I or Category II interface, to an output port. The output port can also be at either a Category I or Category II interface, with the Category II interfaces further divided between those where the timing of the outgoing signal is directly controlled by the timing of the incoming signal that is being regenerated (i.e., Category II interfaces in timing-transparent NEs) and those where it is controlled by a clock (which in turn can be externally-timed, line-timed, through-timed, or free-running). Requirements for non-SONET equipment and systems are given in this section for the following three of the five possible combinations:

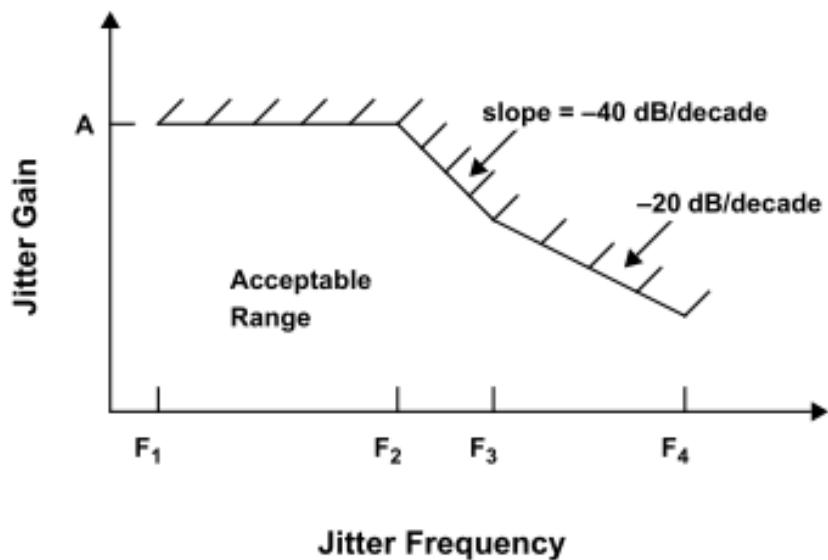
1. Category II to Category I (i.e., through a de-synchronizer)
2. Category I to Category I (i.e., through a multiplexer/de-multiplexer pair)
3. Category II to Category II in timing-transparent NEs (e.g., through a regenerator or repeater).



Demultiplexer Rates ^a	A (dB)	F_1 (Hz)	F_2 (Hz)	F_3 (Hz)	F_4 (Hz)
DS2 to DS1	0.5	10	350	2.5×10^3	15×10^3
DS3 to DS1	0.1	10	350	2.5×10^3	15×10^3
DS3 to DS2	0.1	10	500	2.5×10^3	15×10^3
HR1 ^b to DS3	0.1	10	1000	None ^d	15×10^3
HR3 to HR2 ^c	0.1	10	1250	None ^d	15×10^3

- a. Parameters have not been determined for the jitter transfer through a DS1C to DS1 demultiplexer, and the requirement does not apply for DS3 or DS2 to DS1C demultiplexers.
- b. HR1 denotes any non-SONET level above DS3.
- c. HR2 and HR3 denote non-SONET levels above DS3, where the bit rate of HR2 is less than or equal to 140 Mb/s.
- d. The rolloff between F_2 and F_4 is 20 dB/decade.

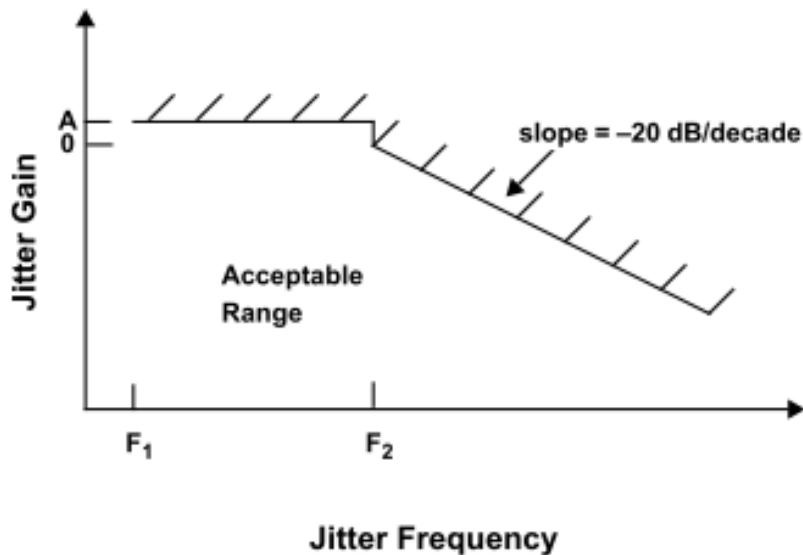
Figure 7-3. Non-SONET Category II Interface to Category I Interface Jitter Transfer



Interface Rate ^a	A (dB)	F_1 (Hz)	F_2 (Hz)	F_3 (Hz)	F_4 (Hz)
DS1	0.1	10	350	2.5×10^3	15×10^3
DS1C	0.1	10	350	2.5×10^3	15×10^3
DS2	0.1	10	500	2.5×10^3	15×10^3
DS3	0.1	10	1000	None ^c	15×10^3
HR ^b	0.1	10	1250	None ^c	15×10^3

- a. The parameters for the Category I to Category I jitter transfer requirement are independent of the particular non-SONET high-speed signal that the low-speed signal is multiplexed into and demultiplexed from. GR-253-CORE contains the parameters for cases where the low-speed signal is mapped into a SONET signal.
- b. HR denotes any non-SONET level above DS3.
- c. The rolloff between F_2 and F_4 is 20 dB/decade.

Figure 7-4. Category I Interface to Category I Interface Jitter Transfer (Non-SONET Systems)

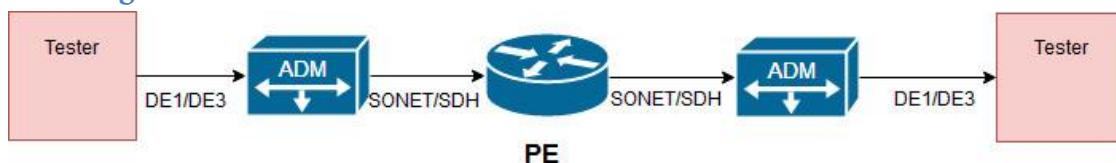


Interface Rate ^a	A (dB)	F_1 (Hz)	F_2 (Hz)
DS1	0.1	10	9.65×10^3
DS1C	0.1	10	3.00×10^3
DS2	0.1	10	3.94×10^3
DS3	0.1	10	59.6×10^3
HR ^b	0.1	10	R/1600

- a. The Category II to Category II jitter transfer requirement applies to equipment where the timing of the outgoing signal is directly controlled by the timing of the incoming signal that is being regenerated (e.g., regenerators and repeaters).
- b. HR denotes any non-SONET level above DS3 whose corresponding bit rate is R.

Figure 7-5. Non-SONET Category II Interface to Category II Interface Jitter Transfer

5.3.2 Testing model:



5.3.3 The sequence configuration:

- Step#1: Configure data path on DUT with System/Loop/ACR/DCR clock
- Step#2: Configure ADM (HPX) with recovery clock from SONET
- Step#3: Start Jitter function on Tester
- Step#2: Refer standard above to measure Jitter.

5.4 Wander Generation:

5.4.1 Phase Variations on Payload Signals

5.4.1.1 Mapping Phase Variations

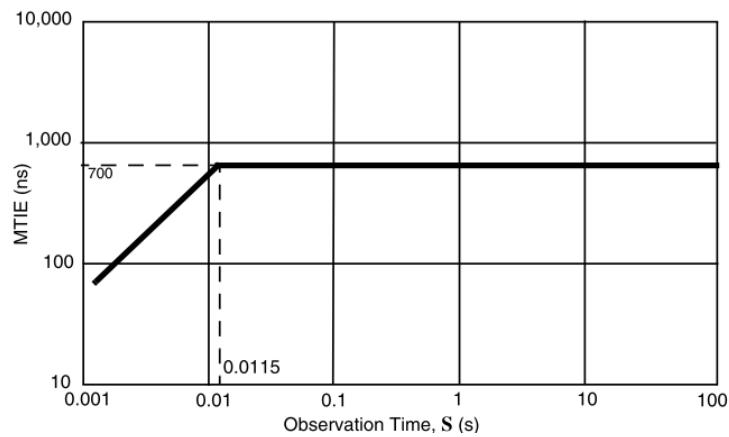
In the asynchronous DS1 to VT1.5 and DS3 to STS-1 mappings, a bit-stuffing mechanism is used to accommodate frequency differences between the DS1 or DS3 and the VT1.5 or STS-1 SPE. This mechanism causes phase variations on DS1 and DS3 signals carried on SONET networks, and these phase variations must be limited for interworking with other network equipment.

To measure the mapping phase variations, it is necessary for the system to be configured so that no STS or VT pointer adjustments occur during the tests. In a single-product test, this can be accomplished by looping back the OC-N or STS-N electrical signal.

5.4.1.1.1 DS1 output from a SONET

The mapping phase variations on a DS1 output from a SONET NE shall be below the mask in Figure 5-36

Figure 5-36 DS1 Mapping Phase Variation Limits

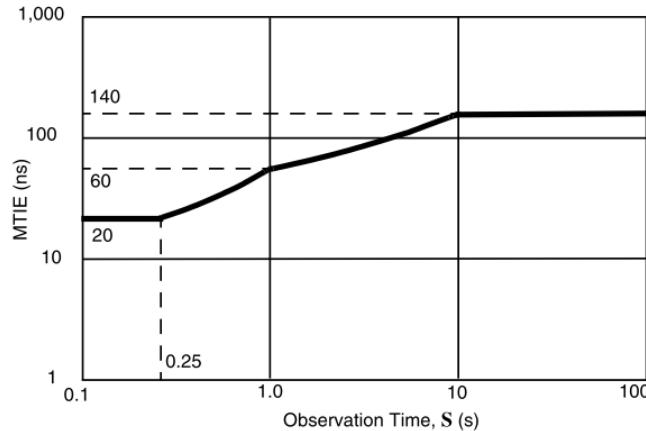


Observation Time, S (seconds)	MTIE (nanoseconds)
$S < 0.001326$	N/A
$0.001326 \leq S \leq 0.0115$	$61000 \times S$
$0.0115 < S$	700

5.4.1.1.2 DS3 output from a SONET

The mapping phase variations on a DS3 output from a SONET NE shall be below the mask in Figure 5-37.

Figure 5-37 DS3 Mapping Phase Variation Limits



Observation Time, S (seconds)	MTIE (nanoseconds)
$S < 0.1$	N/A
$0.1 \leq S \leq 0.25$	20
$0.25 < S \leq 1.0$	$7 + 53 \times S$
$1.0 < S \leq 10$	$23 + 37 \times S^{0.5}$
$10 < S \leq 100$	140
$100 < S$	N/A

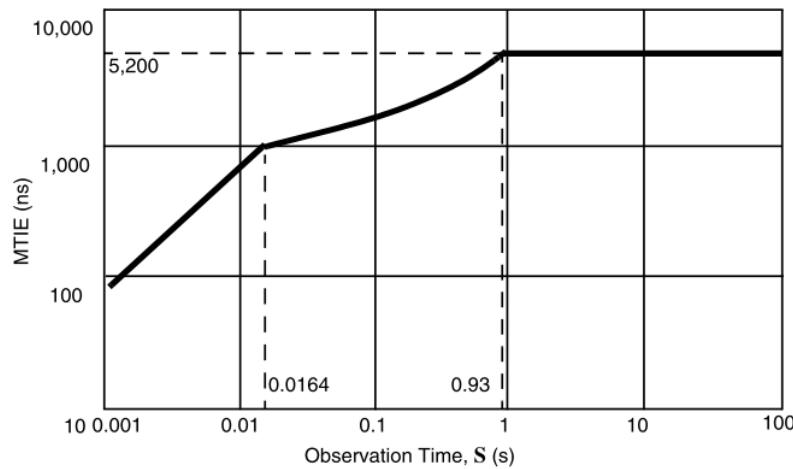
5.4.1.2 Pointer Adjustment Phase Variations

5.4.1.2.1 Single Pointer Adjustments

5.4.1.2.1.1 DS1 output from a SONET

The MTIE of a DS1 output from a SONET NE shall be below the mask in Figure 5-38 when the pointer adjustment test sequence is applied

Figure 5-38 Single VT Pointer Adjustment Phase Variation Limits

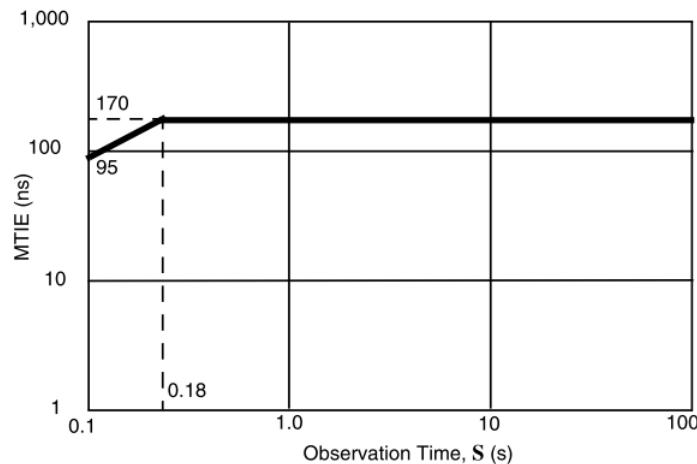


Observation Time, S (seconds)	MTIE (nanoseconds)
$S < 0.001326$	N/A
$0.001326 \leq S \leq 0.0164$	$61000 \times S$
$0.0164 < S \leq 0.93$	$925 + 4600 \times S$
$0.93 < S$	5200

5.4.1.2.1.2 DS3 output from a SONET

The MTIE of a DS3 output from a SONET NE shall be below the mask in Figure 5-39 when the pointer adjustment test sequence is applied

Figure 5-39 Single STS-1 Pointer Adjustment Phase Variation Limits



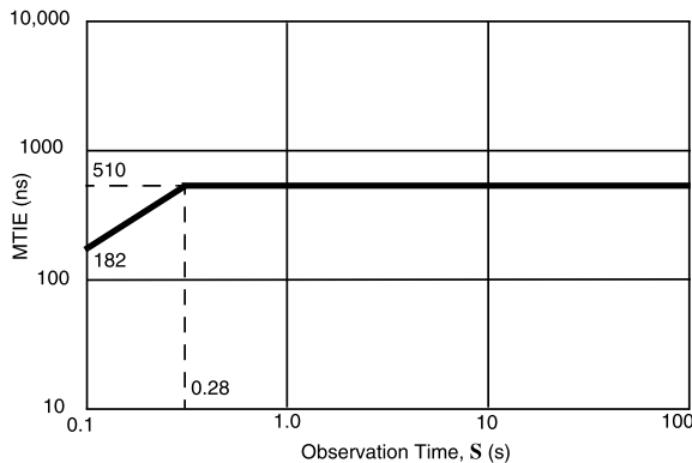
Observation Time, S (seconds)	MTIE (nanoseconds)
$S < 0.1$	N/A
$0.1 \leq S \leq 0.18$	$945 \times S$
$0.18 < S \leq 100$	170
$100 < S$	N/A

5.4.1.2.2 Pointer Adjustment Bursts

5.4.1.2.2.1 DS3 output from a SONET

The MTIE of a DS3 output from a SONET NE shall be below the mask in Figure 5-40 when the pointer test sequence described is applied.

Figure 5-40 Maximum Rate Pointer Burst Phase Variation Limits



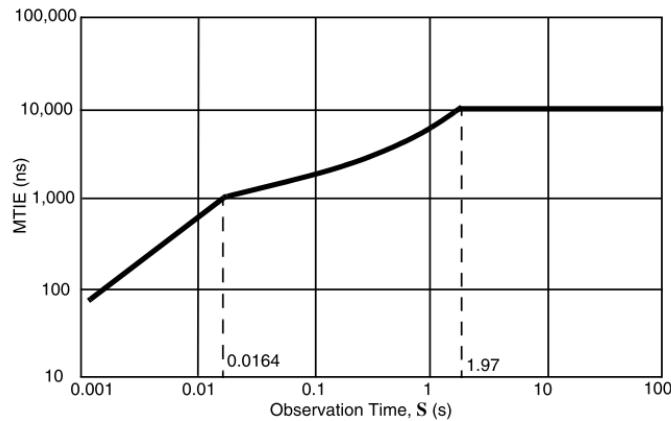
Observation Time, S (seconds)	MTIE (nanoseconds)
$S < 0.1$	N/A
$0.1 \leq S \leq 0.28$	$1820 \times S$
$0.28 < S \leq 100$	510
$100 < S$	N/A

5.4.1.2.3 Periodic Pointer Adjustments

5.4.1.2.3.1 DS1 output from a SONET

The MTIE of a DS1 output from a SONET NE shall be below the mask

Figure 5-42 Periodic VT Pointer Adjustment Phase Variation Limits

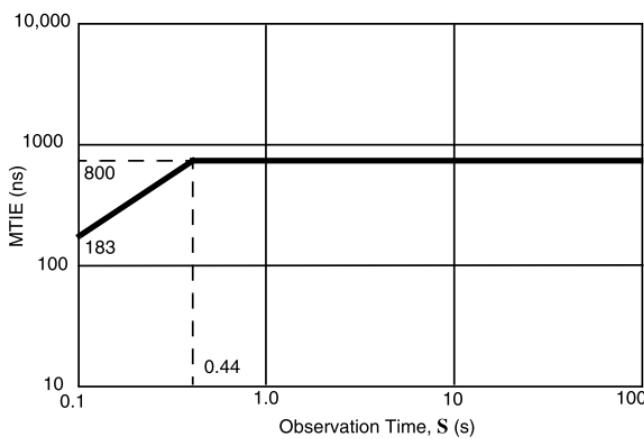


Observation Time, S (seconds)	MTIE (nanoseconds)
$S < 0.001326$	N/A
$0.001326 \leq S \leq 0.0164$	$61000 \times S$
$0.0164 < S \leq 1.97$	$925 + 4600 \times S$
$1.97 < S$	10,000

5.4.1.2.3.2 DS3 output from a SONET

The MTIE of a DS3 output from a SONET NE shall be below the mask

Figure 5-43 Periodic STS-1 Pointer Adjustment Phase Variation Limits



Observation Time, S (seconds)	MTIE (nanoseconds)
$S < 0.1$	N/A
$0.1 \leq S \leq 0.44$	$1830 \times S$
$0.44 < S \leq 100$	800
$100 < S$	N/A

5.4.2 The testing model:



- Tester: use DE1 or DE3 Tester
- ADM: use HPX
- PE: use System/Looptime/ACR/DCR clock

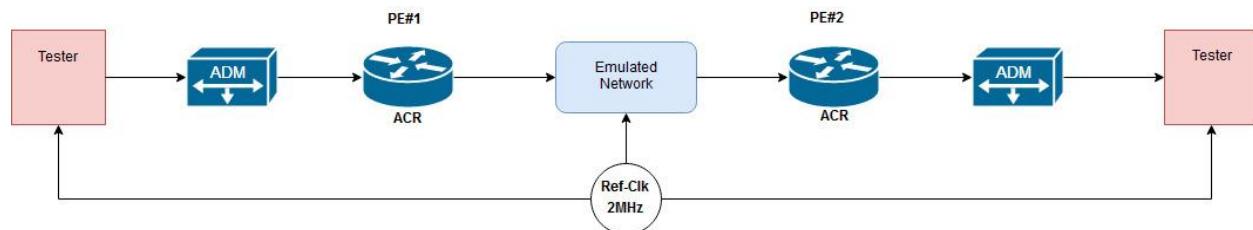
5.4.3 The sequence configuration

- Step#1: Configure data path on DUT with System/Loop/ACR/DCR clock
- Step#2: Configure HPX (ADM) with recovery clock from SONET
- Step#3: Start Jitter function on Tester
- Step#2: Refer standard above to measure Jitter.

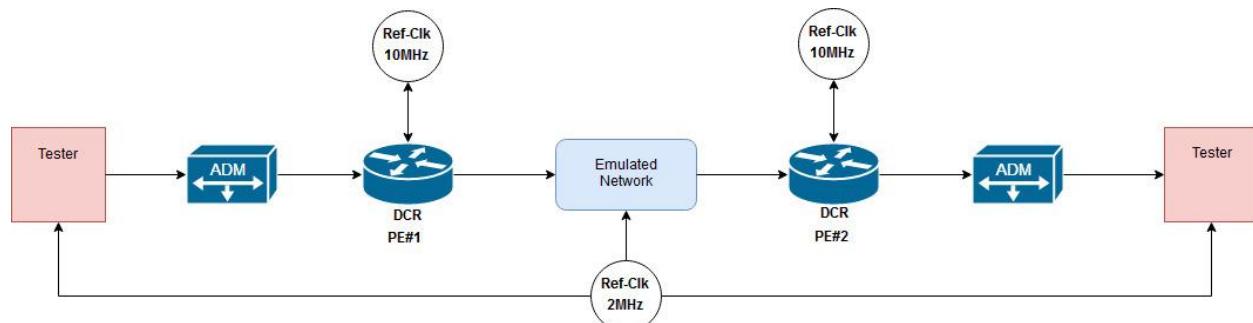
5.4.4 Measure test-case G.8261:

5.4.4.1 The testing model:

- Use ADM was used by HPX
- Tester: TB8000
- Ref-Clk 2MHz and 10Mhz: Acterna box
- ACR Mode:



- DCR Mode:



5.4.4.2 Test-cases for ACR mode:

5.4.4.2.1 Test-case #1:

- Step#1: Configure data path with ACR mode on DUT (only one channel)
- Step#2: Start Test-case #1 on ANUE Tester.
- Step#3: Waiting for ACR was locked, restart Tester to measure wander for Test-case #1
- Step#4: After Test-case#1 finished (check on ANUE), stop ANUE and save TIE data to compare with mask above.

5.4.4.2.2 Test-case #2, #3, #4, #5, #6, #7, #8:

- Refer steps in section 2.3.6.3.1 to measure Test-case #2, #3, #4, #5, #6, #7, #8.

5.4.4.3 Test-cases for DCR mode:

5.4.4.3.1 Test-case #9:

- Step#1: Configure data path with DCR mode on DUT (only one channel)
- Step#2: Start Test-case #9 on ANUE Tester
- Step#3: Waiting for DCR was locked, restart Tester to measure wander for Test-case #9
- Step#4: After Test-case #9 finished (Check on ANUE), stop ANUE and save TIE data to compare with mask above.

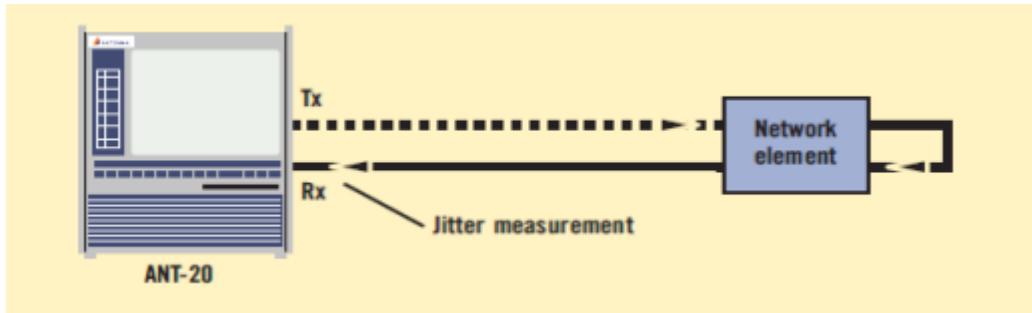
5.4.4.3.2 Test-case #10, #11:

- Refer steps in section 2.3.6.4.1 to measure Test-case #10, #11

6 Appendix

6.1 Arrive common test models:

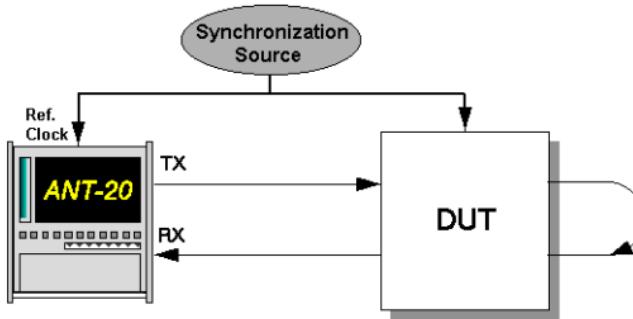
6.1.1 Jitter testing (include Jitter Transfer, Jitter Generate, Jitter Tolerance):



- Tester: ANT20 or JDSU → see [Appendix 6.2](#)
- Network Element: Cisco's Board. Use sample script as below
 - o E1/DS1 interface:
 - [\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\ds1_unframed.tcl](#)
 - [\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\e1_unframed.tcl](#)
 - o E3/DS3 interface:
 - [\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\ds3_unframed.tcl](#)
 - [\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\e3_unframed.tcl](#)
 - o SONET interface:
 - [\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\sonet_oc48_sts1_ds1_unframed.tcl](#)
 - [\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\sonet_oc48_sts1_e1_unframed.tcl](#)

6.1.2 Wander testing

6.1.2.1 Wander without PDV



- Tester: ANT20 or JDSU → see [Appendix 6.2](#)
- PRC box → see [Appendix 6.5](#)
- Network Element: Cisco's Board. Use sample script as below
 - E1/DS1 interface:
 - [\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\ds1_unframed_acr.tcl](#)
 - [\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\ds1_unframed_dcr.tcl](#)
 - [\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\e1_unframed_acr.tcl](#)
 - [\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\e1_unframed_dcr.tcl](#)
 - E3/DS3 interface:
 - [\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\ds3_unframed_acr.tcl](#)
 - [\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\ds3_unframed_dcr.tcl](#)
 - [\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\e3_unframed_acr.tcl](#)
 - [\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\e3_unframed_dcr.tcl](#)

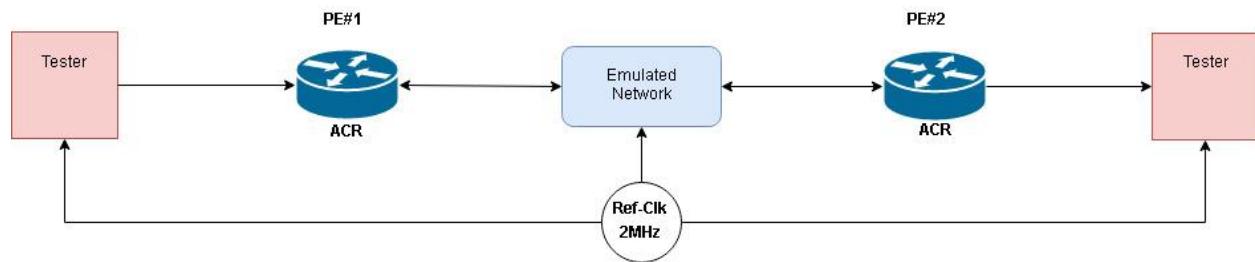
- SONET interface:

- \\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\sonet_oc48_sts1_ds1_unframed_acr.tcl
- \\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\sonet_oc48_sts1_ds1_unframed_dcr.tcl
- \\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\sonet_oc48_sts1_e1_unframed_acr.tcl
- \\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\sonet_oc48_sts1_e1_unframed_dcr.tcl

6.1.2.2 Wander with PDV (ITU-T G.8261)

6.1.2.2.1 ACR mode:

6.1.2.2.1.1 LIU Interface:

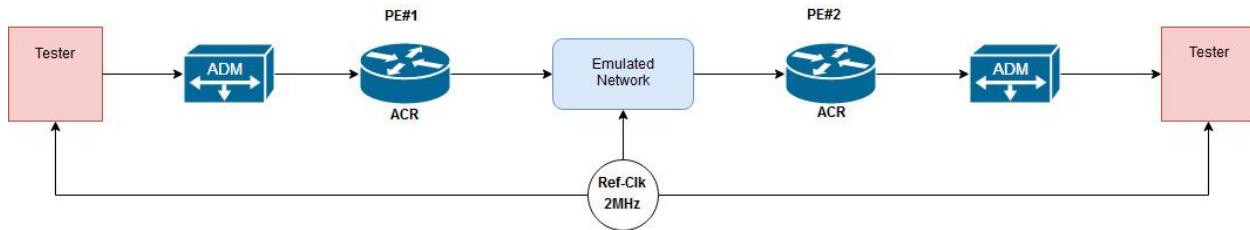


- Tester: ANT20 or JDSU → see [Appendix 6.2](#)
- Ref-Clk use PRC box → see [Appendix 6.5](#)
- Emulated Network: Calnex or Anue → see [Appendix 6.3](#) or [Appendix 6.4](#)
- PE#1 and PE#2: Cisco's Board. Use Cisco IOS → See the sample script as below

- E1/DS1 interface:

- \\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\IOS_ds1_unframed_acr.tcl
- \\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\IOS_e1_unframed_acr.tcl

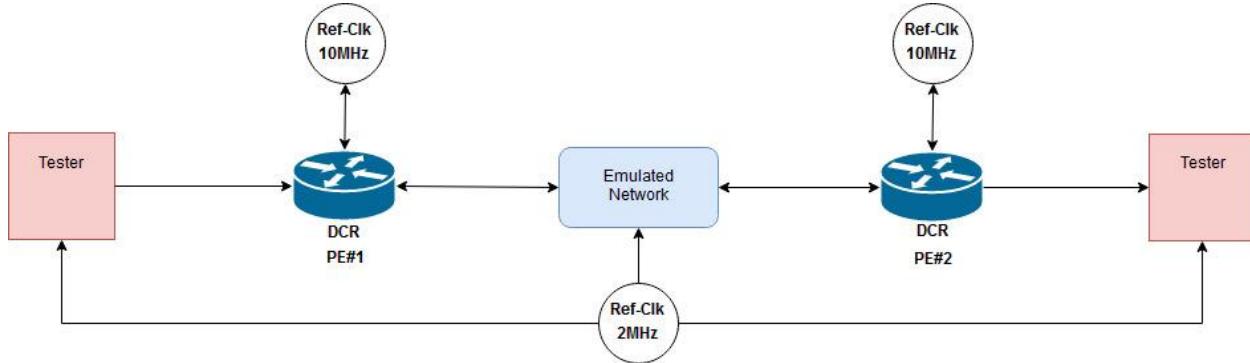
6.1.2.2.1.2 SONET/SDH interface:



- Tester: ANT20 or JDSU → see [Appendix 6.2](#)
- Ref-Clk use PRC box → see [Appendix 6.5](#)
- Emulated Network: Calnex or Anue → see [Appendix 6.3](#) or [Appendix 6.4](#)
- ADM use HPX box → see [Appendix 6.6](#)
- PE#1 and PE#2: Cisco's Board. Use Cisco IOS → See the sample script as below
 - o \\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\IOS_oc48_ds1_unframed_acr.tcl

6.1.2.2.2 DCR mode:

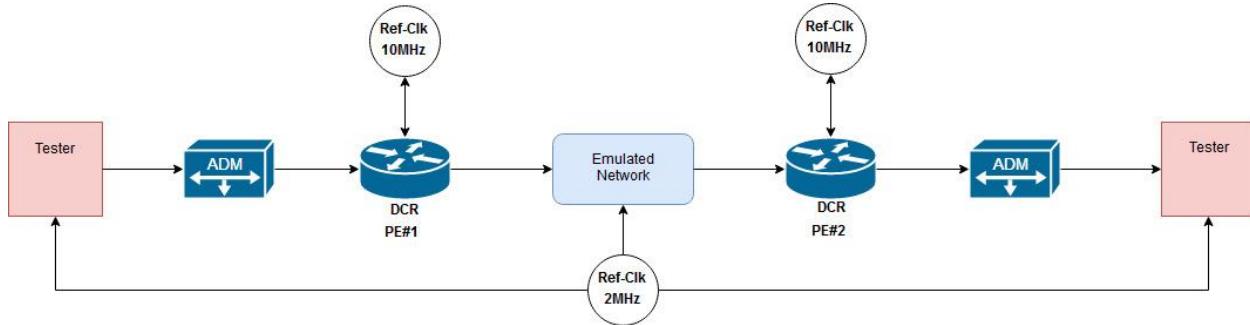
6.1.2.2.2.1 LIU interface:



- Tester: ANT20 or JDSU → see [Appendix 6.2](#)
- Ref-Clk use PRC box → see [Appendix 6.5](#)
- Emulated Network: Calnex or Anue → see [Appendix 6.3](#) or [Appendix 6.4](#)
- PE#1 and PE#2: Cisco's Board. Use Cisco IOS → See the sample script as below
 - o E1/DS1 interface:

- \\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\IOS_ds1_unframed_dcr.tcl
- \\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\IOS_e1_unframed_dcr.tcl

6.1.2.2.2 SONET/SDH interface:

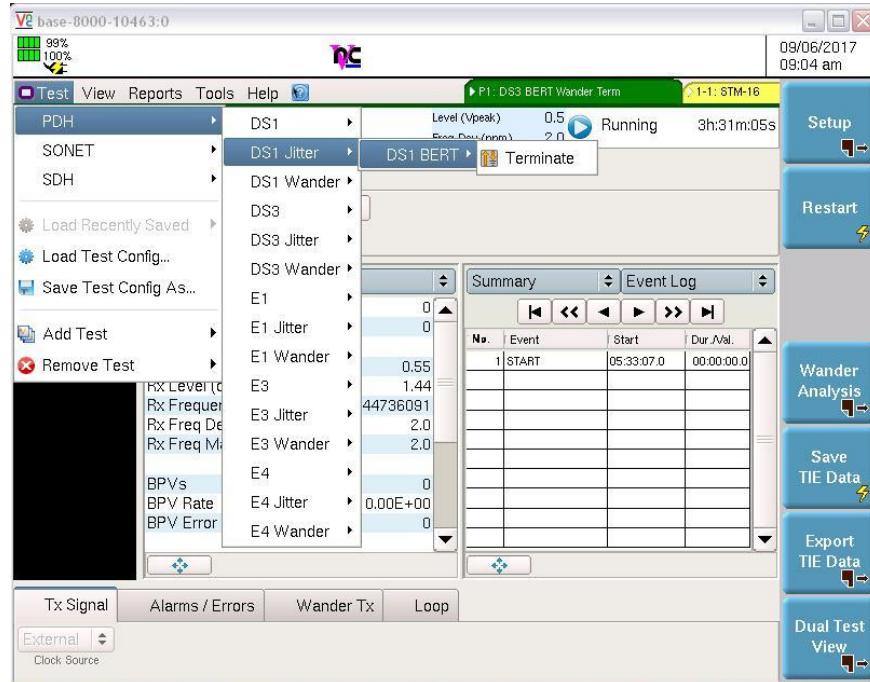


- Tester: ANT20 or JDSU → see [Appendix 6.2](#)
- Ref-Clk use PRC box → see [Appendix 6.5](#)
- Emulated Network: Calnex or Anue → see [Appendix 6.3](#) or [Appendix 6.4](#)
- ADM use HPX box → see [Appendix 6.6](#)
- PE#1 and PE#2: Cisco's Board. Use Cisco IOS → See the sample script as below
 - \\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\TIMING\tcl scripts\IOS_oc48_ds1_unframed_dcr.tcl

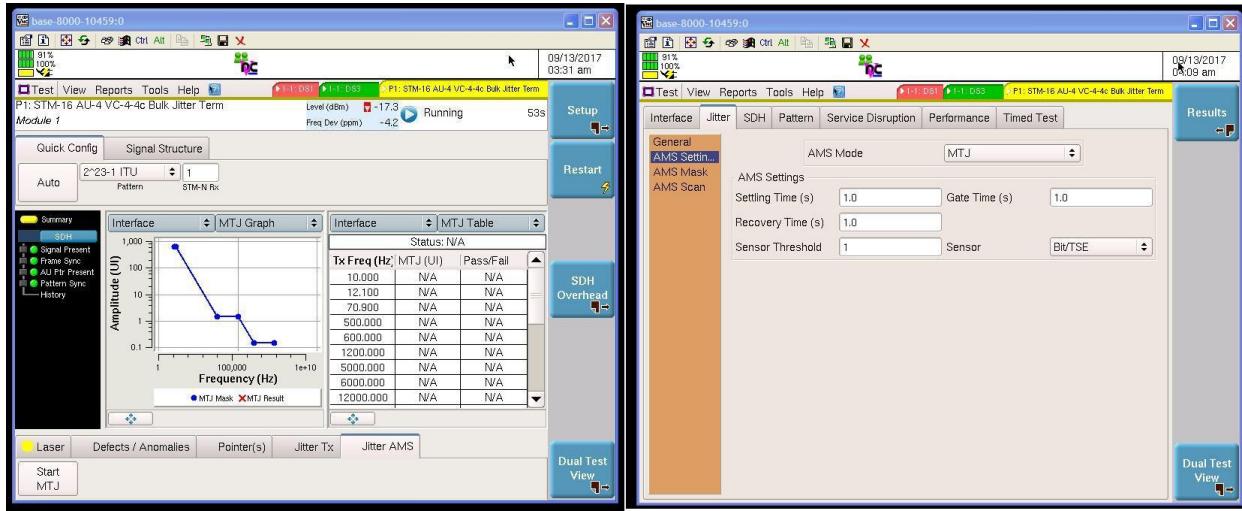
6.2 JDSU configuration:

Refer User Manual of TB8000

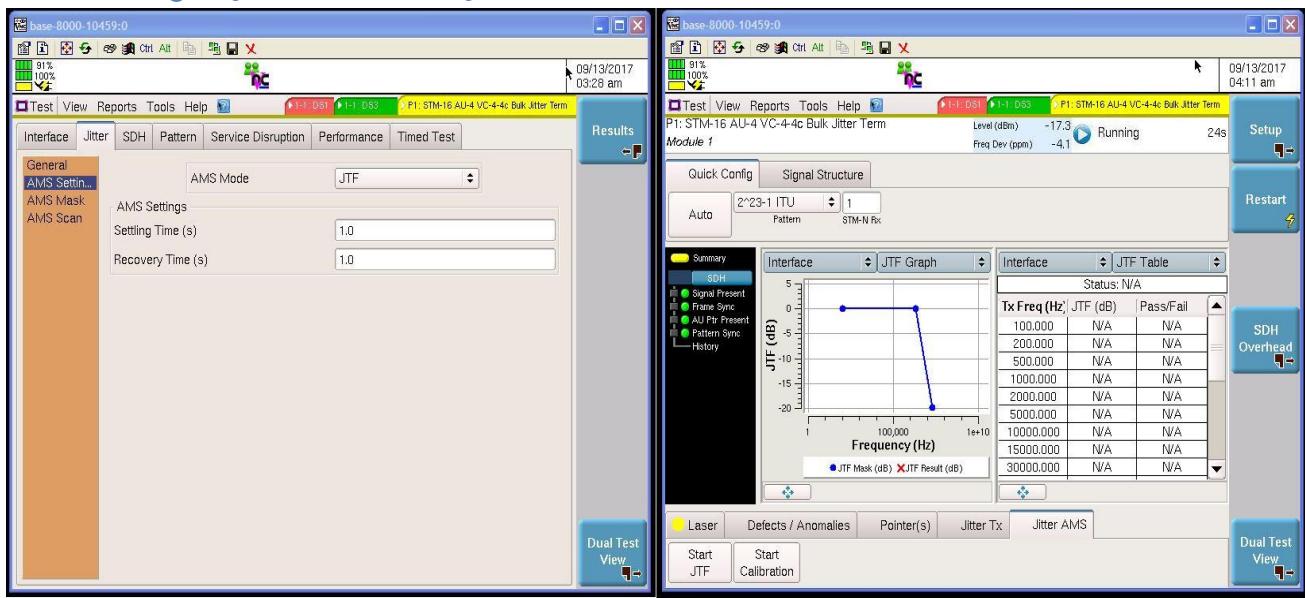
6.2.1 Configure Jitter function on JDSU



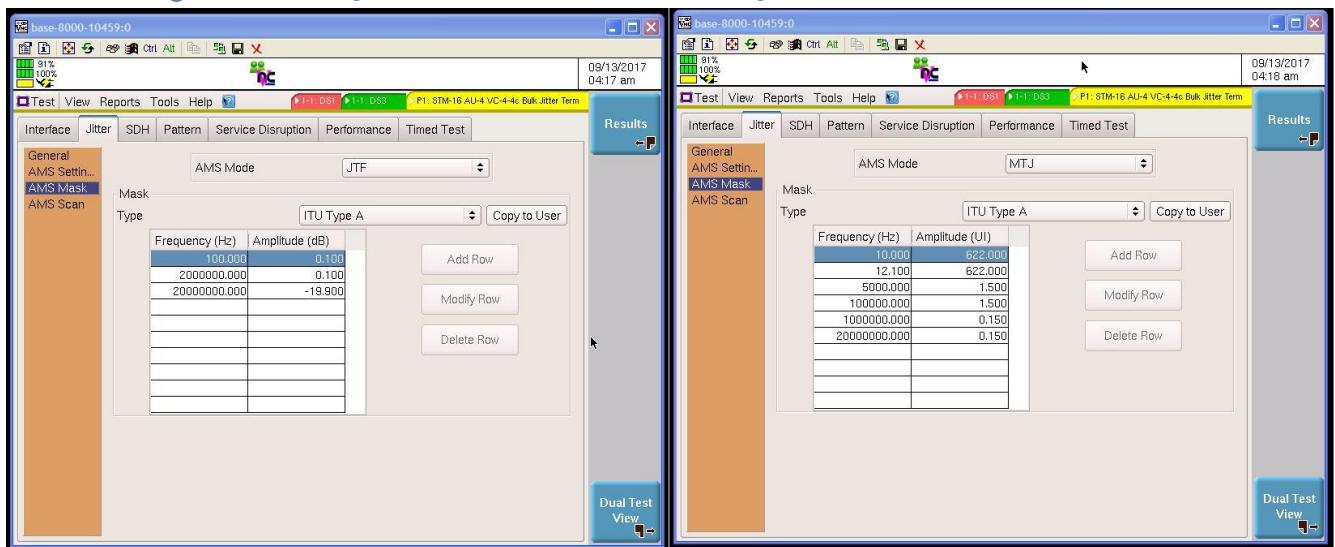
6.2.2 Configure Jitter Tolerance on JDSU



6.2.3 Configure Jitter Transfer on JDSU

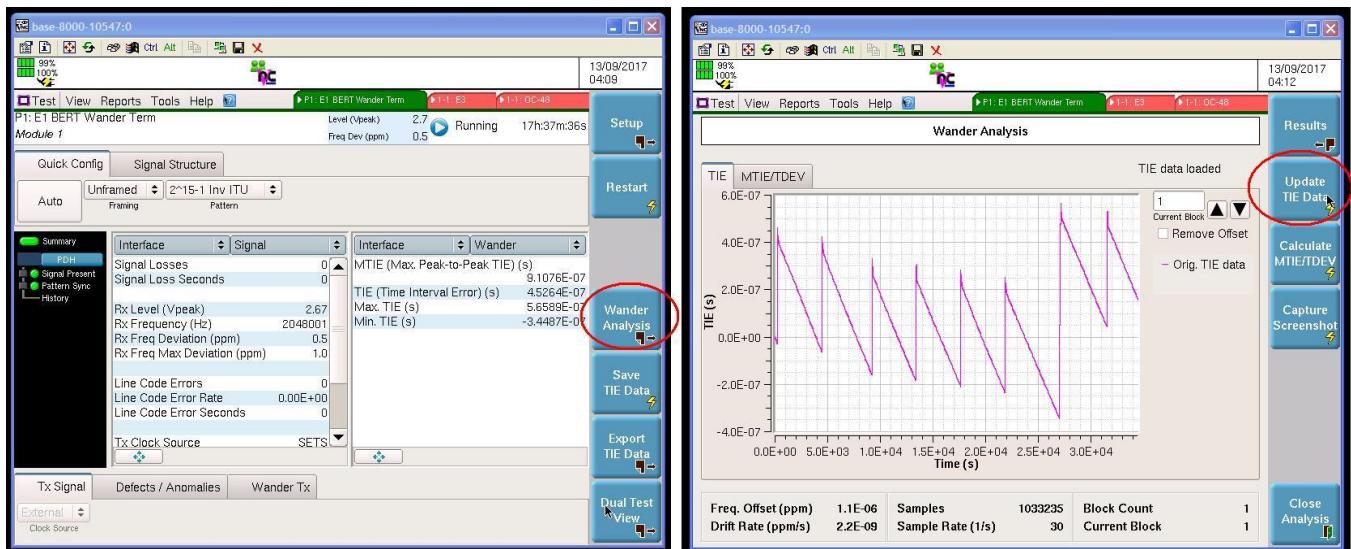
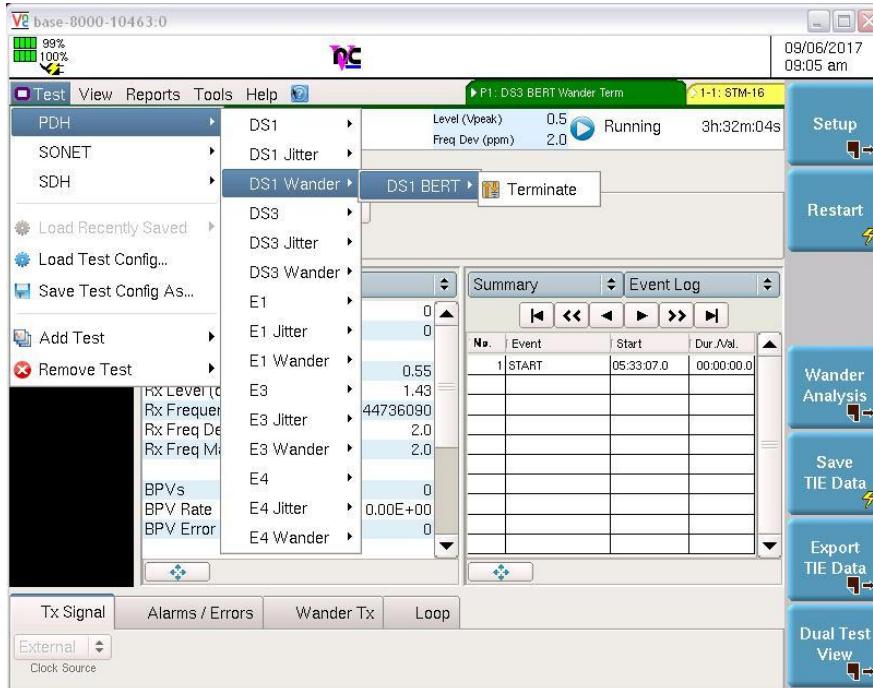


6.2.4 Configure Mask for Jitter Tolerance or Transfer on JDSU



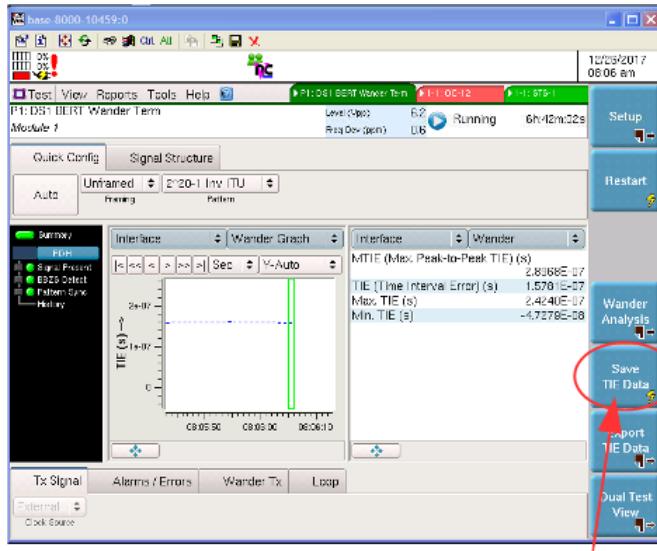
6.2.5 Configure Wander function on JDSU

6.2.5.1 Check TIE result on JDSU:



6.2.5.2 Save TIE result to analyze by Apps:

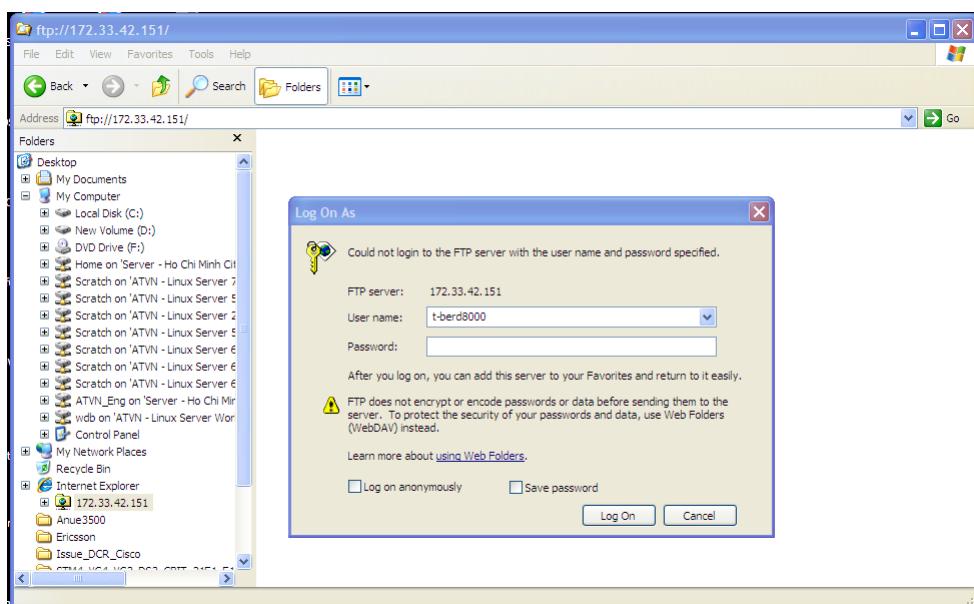
After save TIE result, please see [Appendix 6.7](#) to how to analyze TIE and MTIE



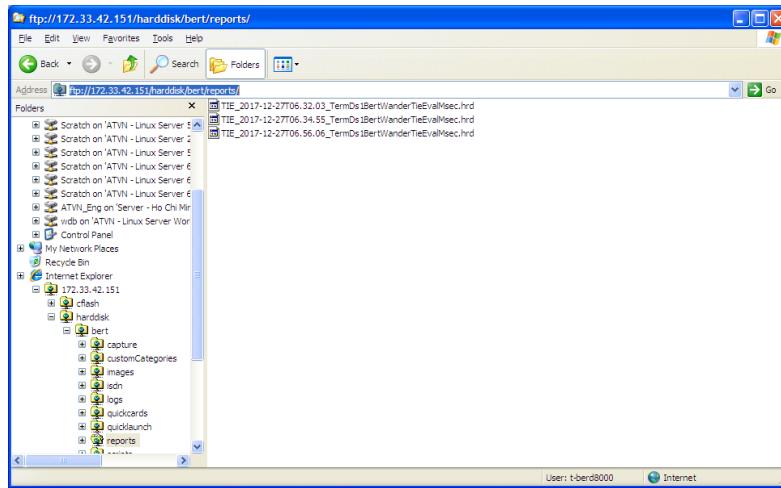
Save TIE result

6.2.6 How to get TIE data from JDSU

- FTP to JDSU (ex:172.33.42.151)
- User name: t-berd8000
- Password: acterna

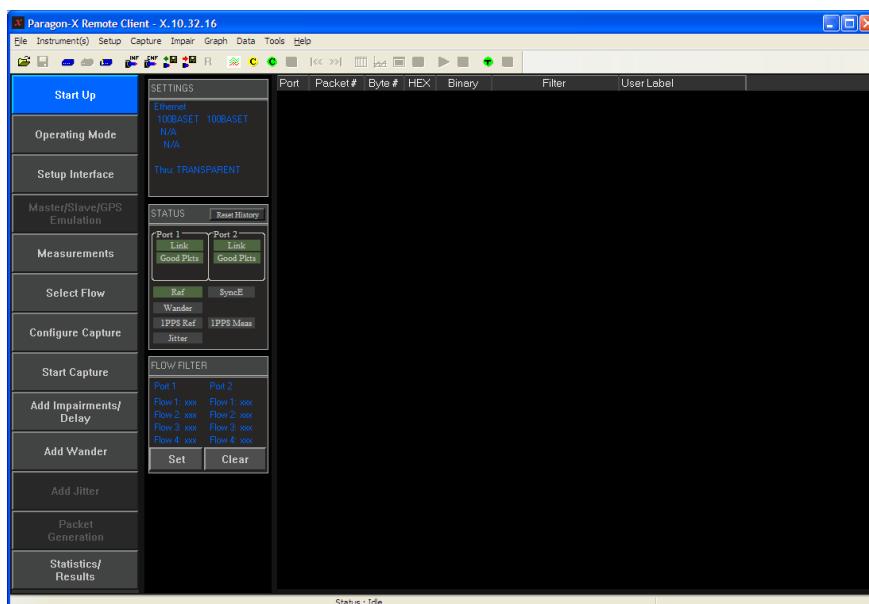


- Get TIE data from folder: <ftp://172.33.42.151/harddisk/bert/reports/>



6.3 Calnex configuration:

- Request IT install Paragon-X on your desktop
- Get profile (test-cases) from folder: \\it-ref\All_Ref\ATVN_Ref_CD\JDSU\ParagonX\Profile\CES
- IP address of Calnex: **172.33.42.93**
- To setup Calnex → Refer to <\\wdb\wdb\projects\wander\Documents\Paragon-X Getting Started Guide.pdf>
- This is interface of Calnex on destop

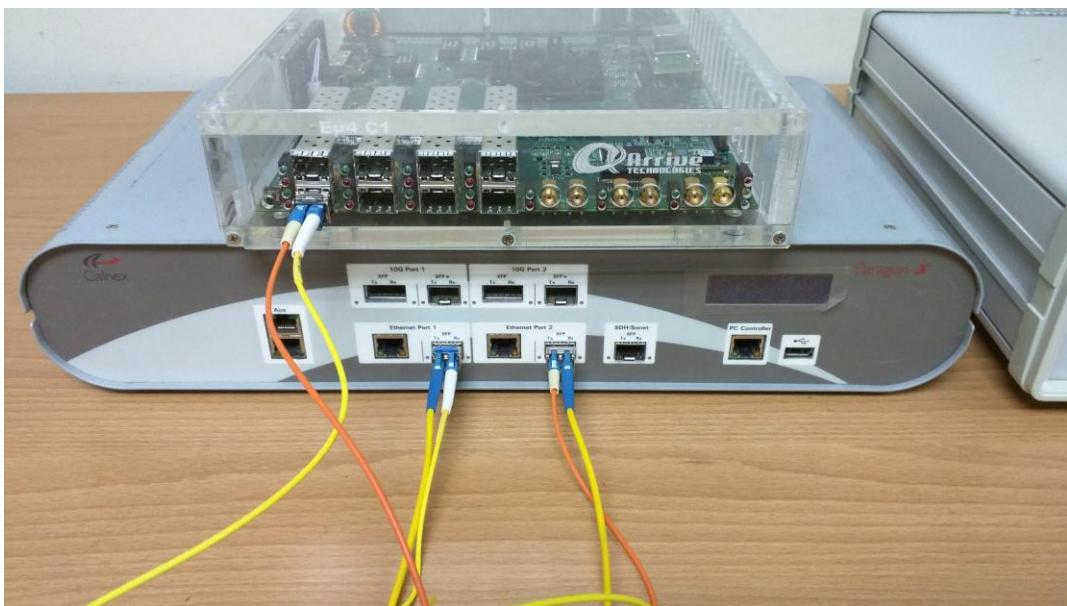


6.3.1 Connection Calnex Tester with PRC



6.3.2 Connection Calnex Tester with Board

6.3.2.1 EP6C1 Board

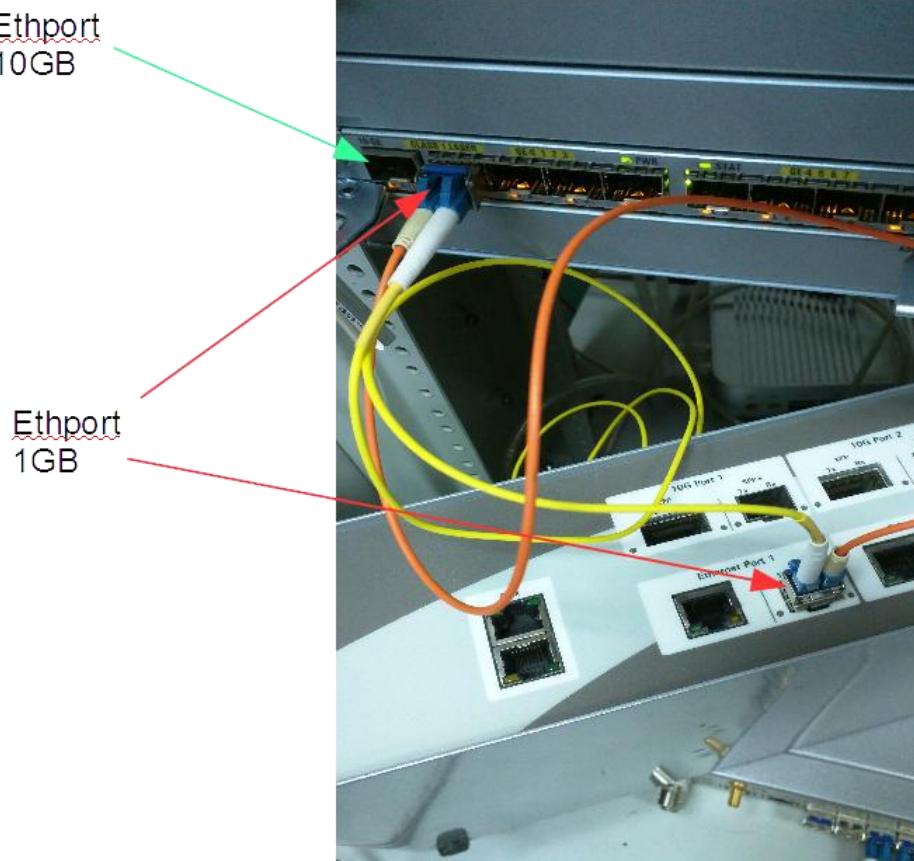




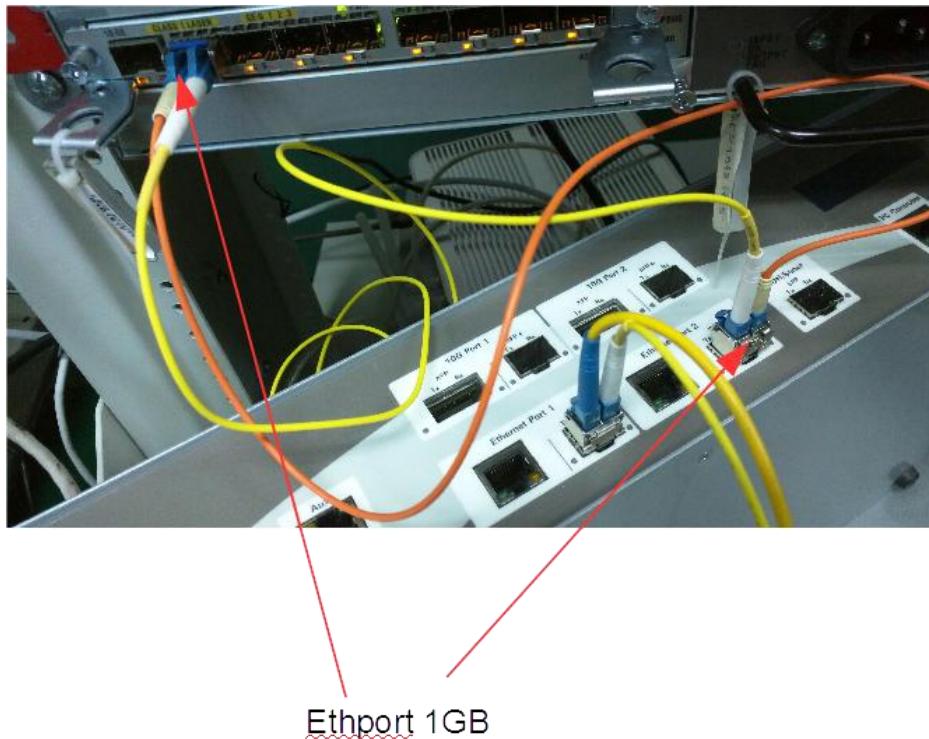


6.3.2.2 Cisco's Board

6.3.2.2.1 Board#1



6.3.2.2Board#2



6.4 ANUE configuration:

Welcome to the Anue 3500 Control Panel.

The Anue 3500 is an intuitive test-case-driven solution for validating synchronization performance and Carrier Ethernet functions found in next generation Ethernet based mobile backhaul networks. With the Anue 3500 you can leverage test and development engineers of almost any skill level to quickly verify compliance to international standards-based requirements with real-time graphed analysis and automatic pass/fail results. The Anue 3500 provides real-world testing for a range of technologies including Synchronous Ethernet, IEEE 1588v2/PTP, SAToP/CESoPSN, MPLS and Ethernet OAM.

Contact Information

Visit [our support page](#) for support and contact information. For more information about the full assortment of Anue's products, please visit [AnueSystems.com](#).

Launching the Anue 3500 Control Panel

Click the button below to launch the Control Panel. If this is the first time you have launched the application, java-based files will be automatically downloaded to your computer. Use the default user name (admin) and default password (admin) to sign on to the system the first time.

Installing the Anue 3500 Tcl Command Shell and Scripting Package

You may install the Tcl Package by downloading and unpacking [this ZIP file](#).

Your computer does not appear to have Java Web Start installed or you might be using an unsupported browser. To try to launch anyway, click [here](#). To download the necessary Java files, click [here](#).

Front Panel LCD Display

1 Anue 3500
Status: Normal

Server software version 1.2.0-56494-20120913-122428 ©2011-2012 Anue Systems

6.4.1 Connection Anue with PRC

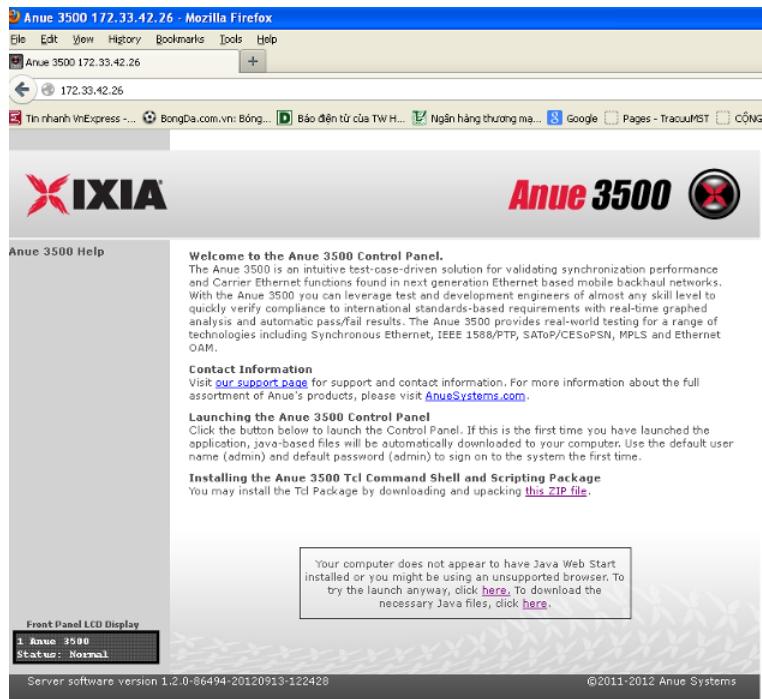
Same as Calnex (see section [6.3.2.1](#))

6.4.2 Connection Anue with Board

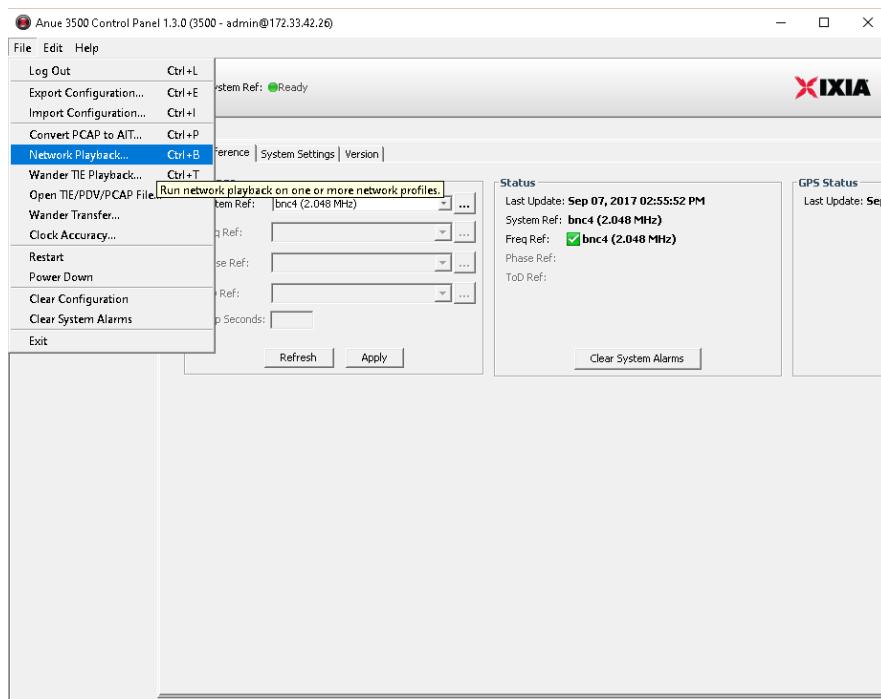
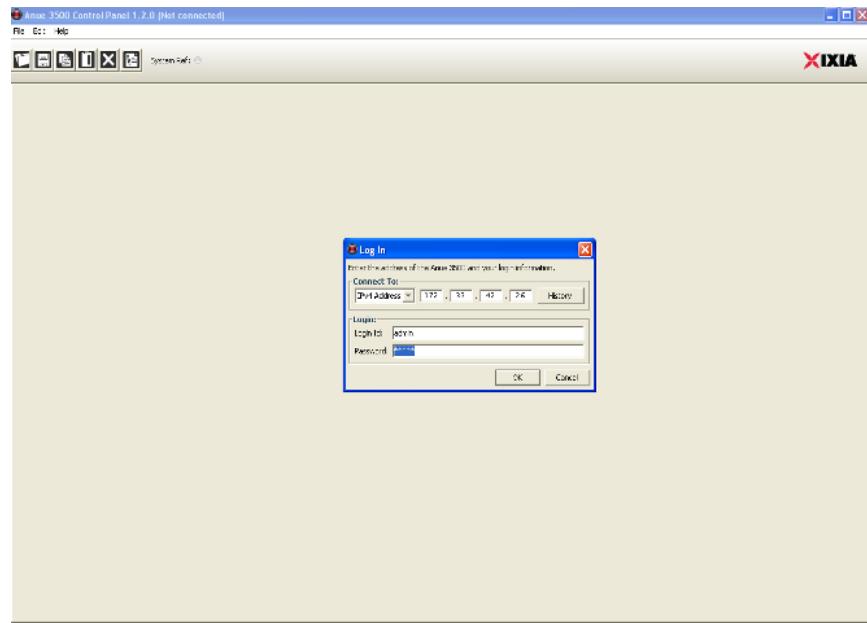
Same as Calnex (see section [6.3.2.2](#))

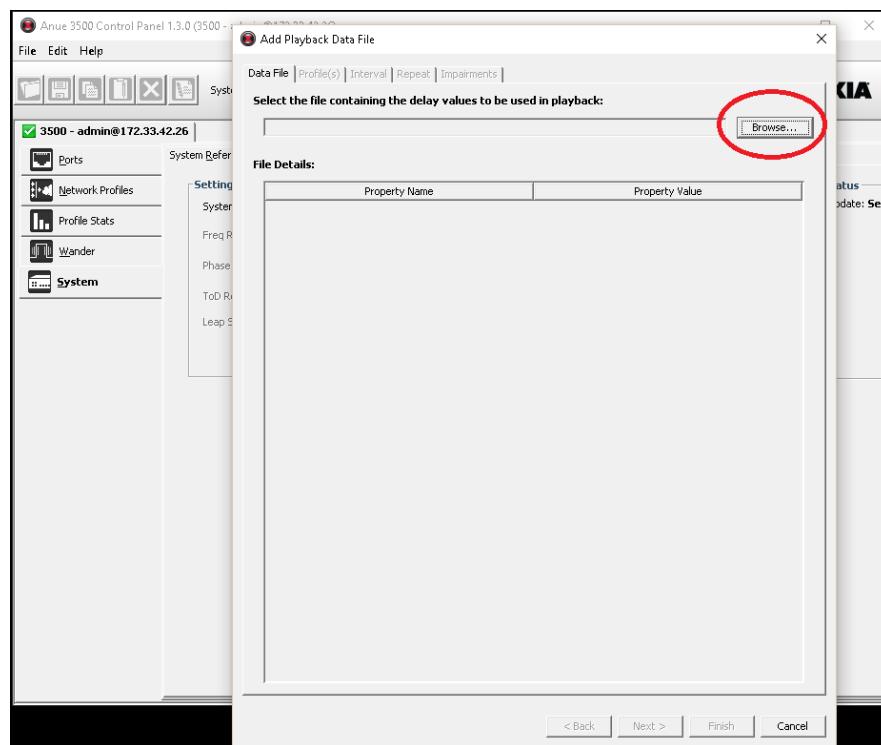
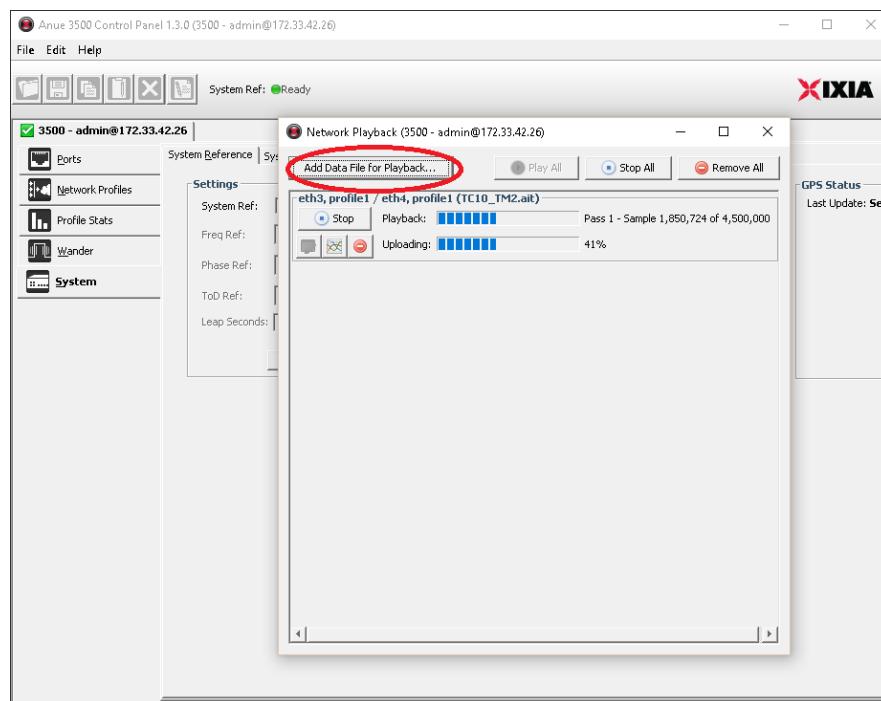
6.4.3 Start test-case on ANUE

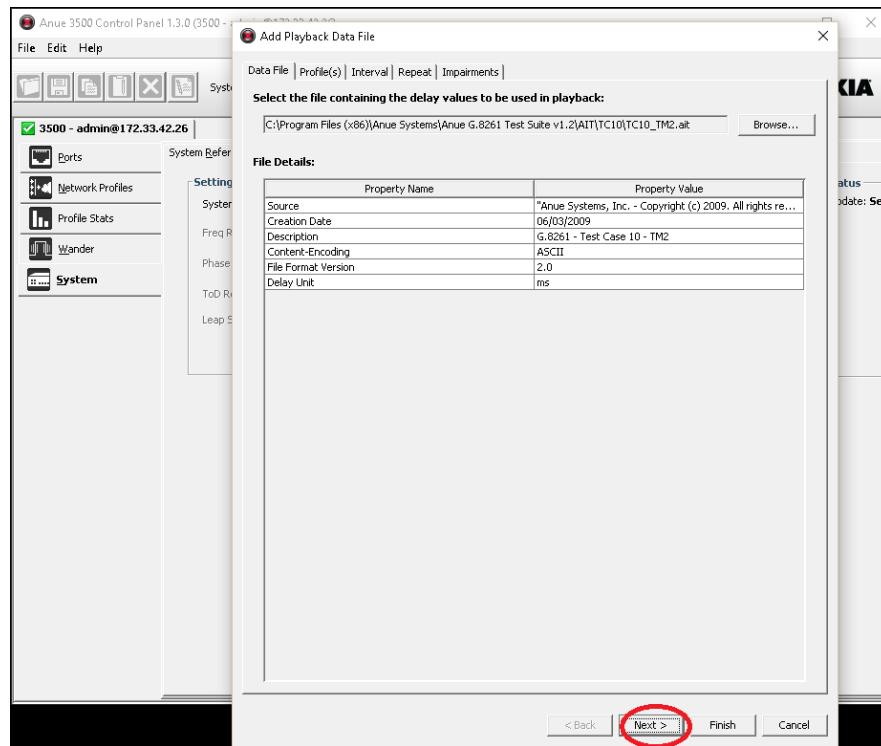
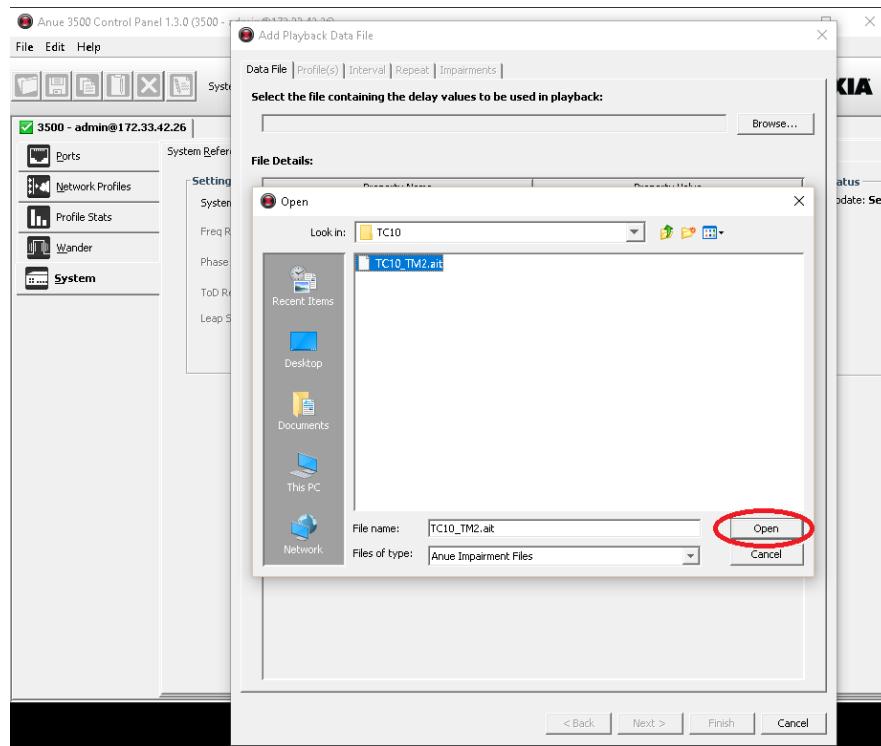
- Get profile (test-cases) from folder: \\IT-REF\All_Ref\ATVN_Ref_CD\Anue 3500 System\ITU-G8261.TestSuite.v1.2_Testcase\

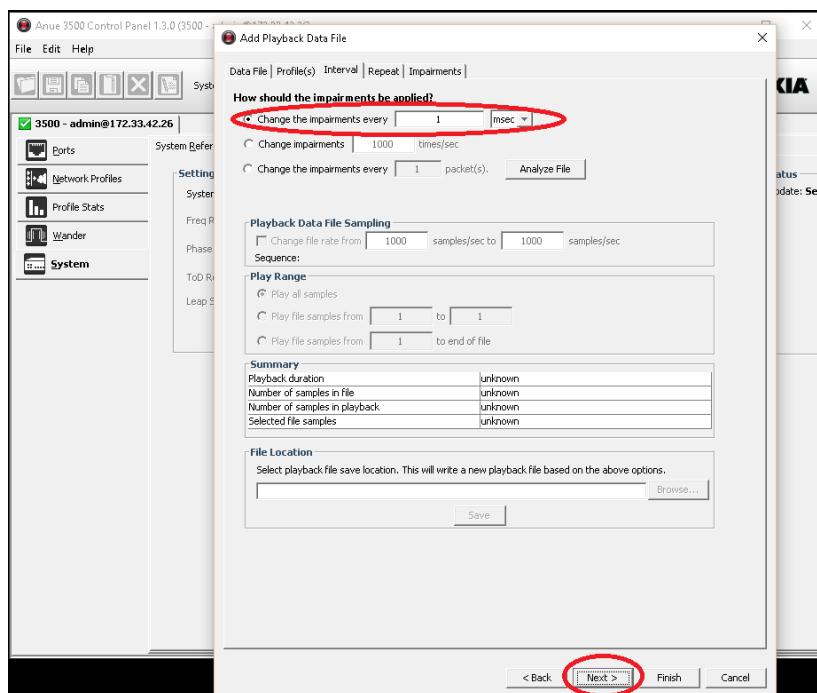
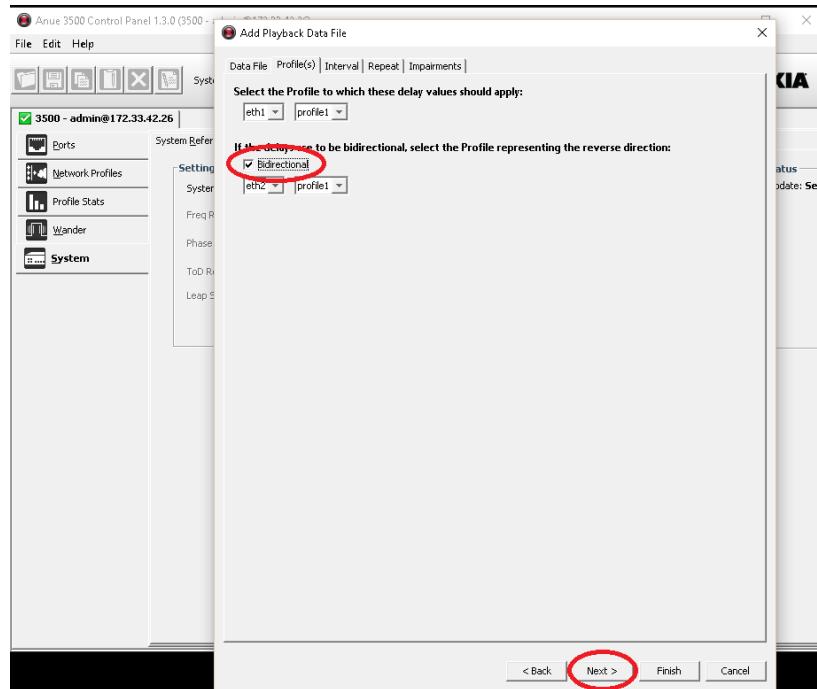


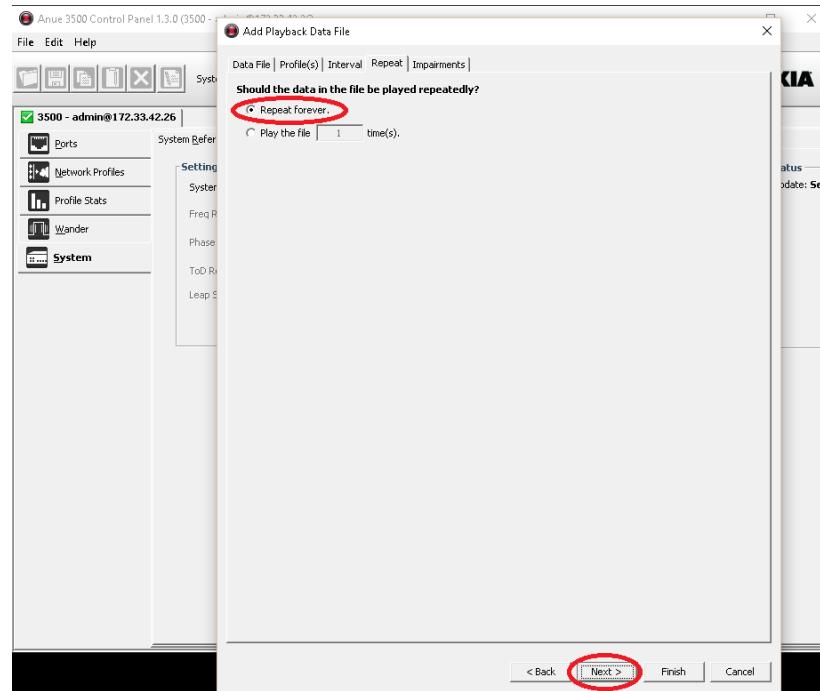
- Login: admin
- Password: admin



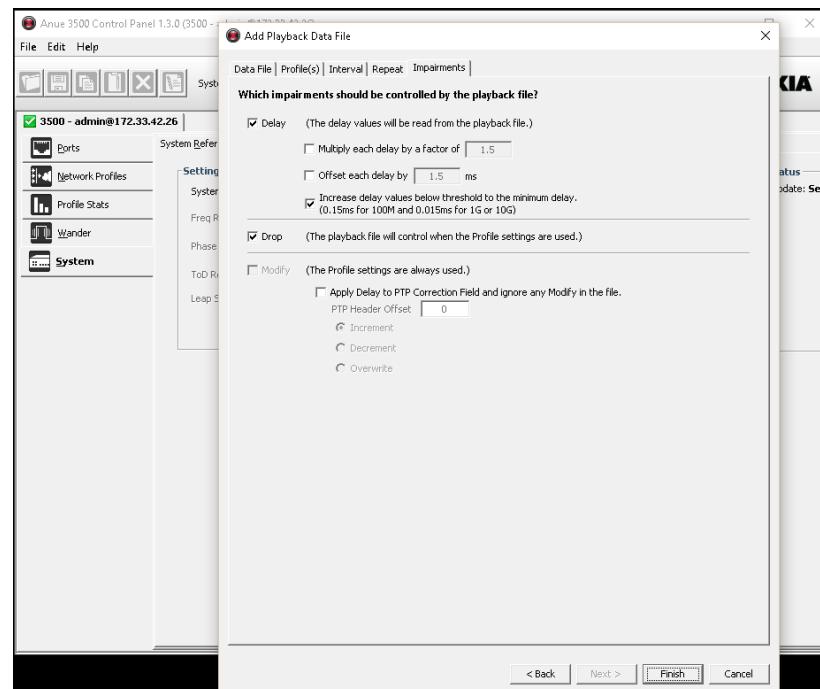


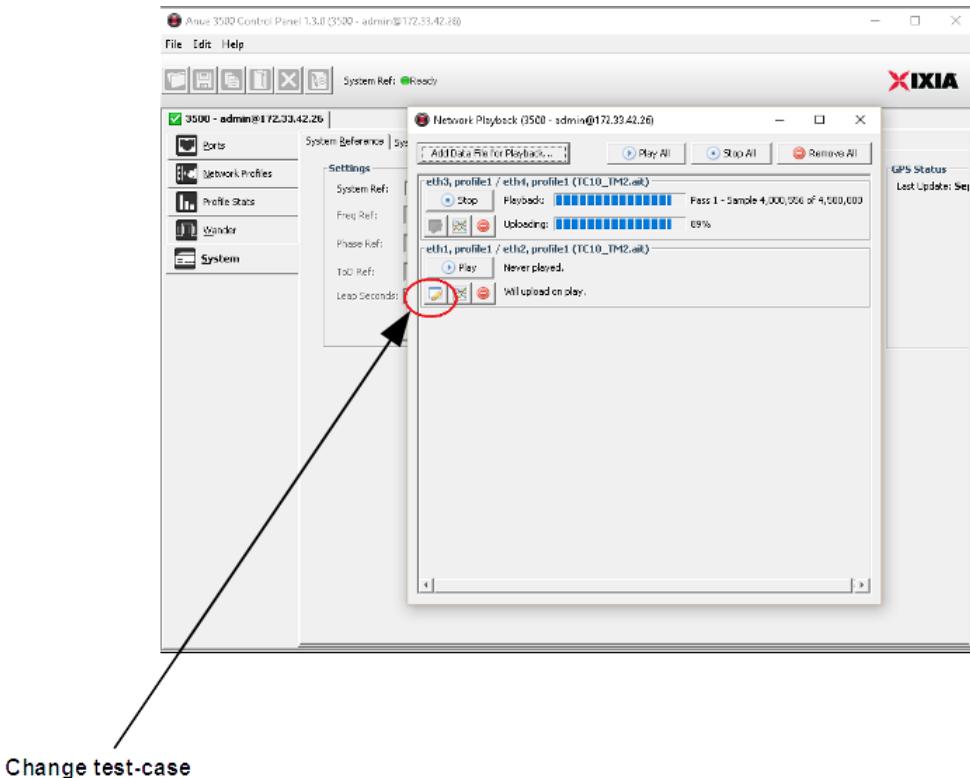






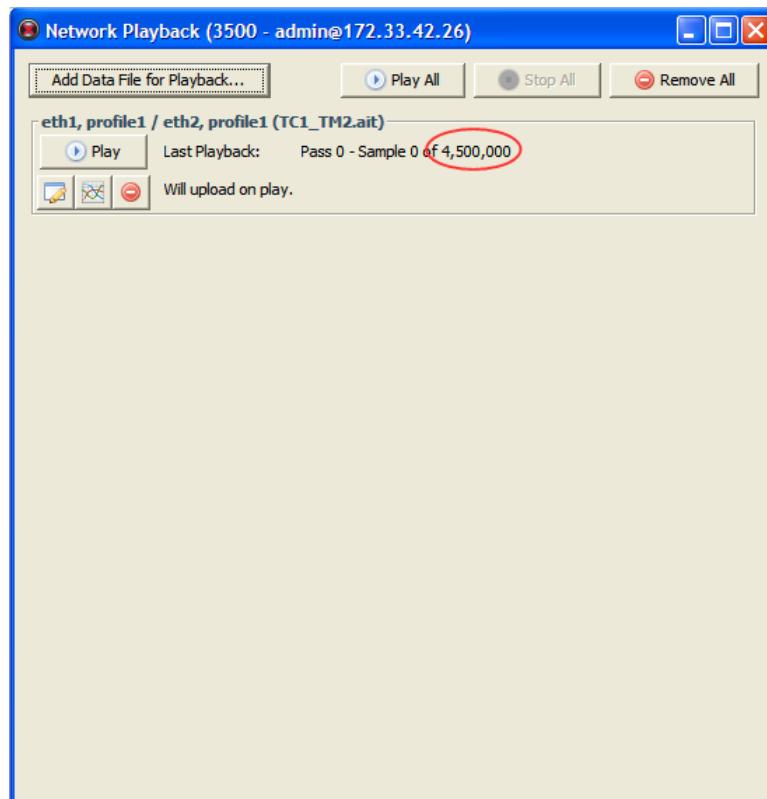
- Repeate forever → run many times
- Play the file ... → choose number of times to run test-case (ex: 1 times → will auto finish)





Change test-case

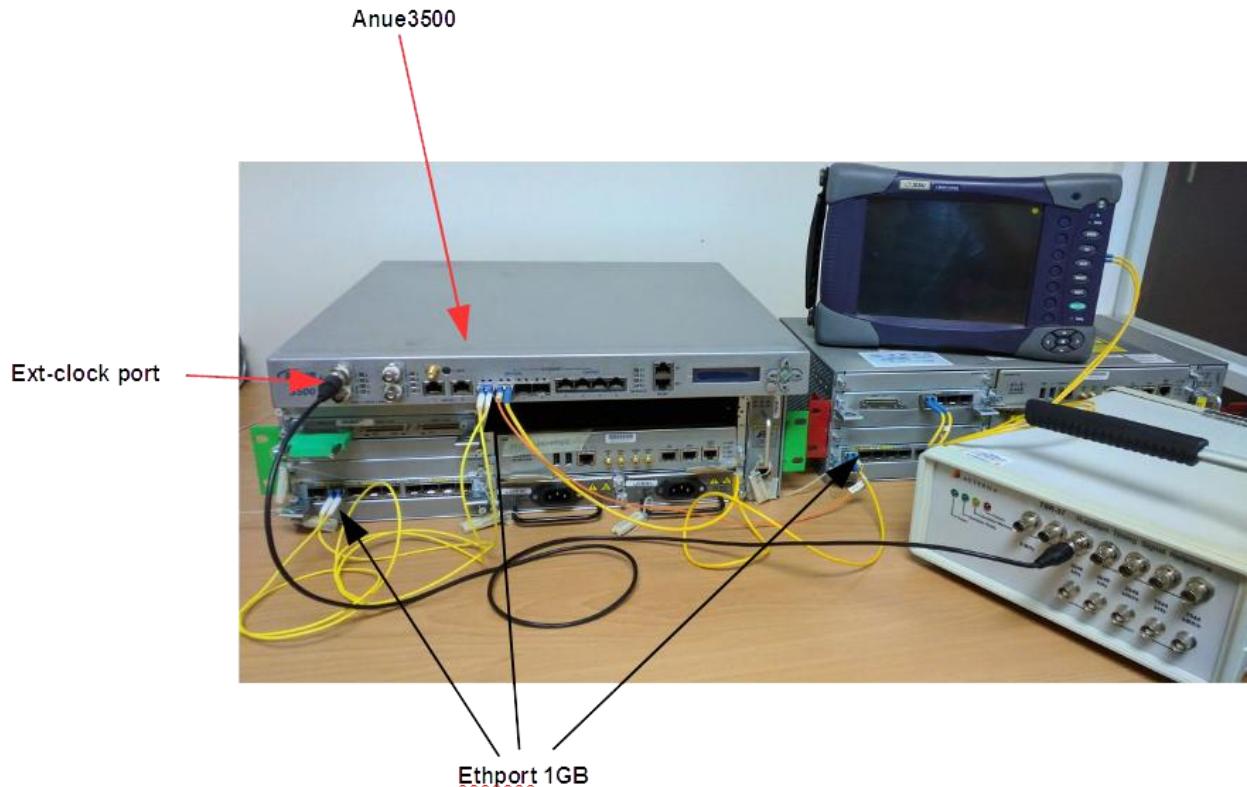
- Time to finish test-case



6.4.4 Test-cases on ANUE

Refer to <\\wdb\\wdb\\projects\\wander\\Documents\\ Tech Note - G8261 - Delay Plots v1.2.pdf>

- TC9_TM2
- TC10_TM2
- TC11_TM2



6.5 PRC box:



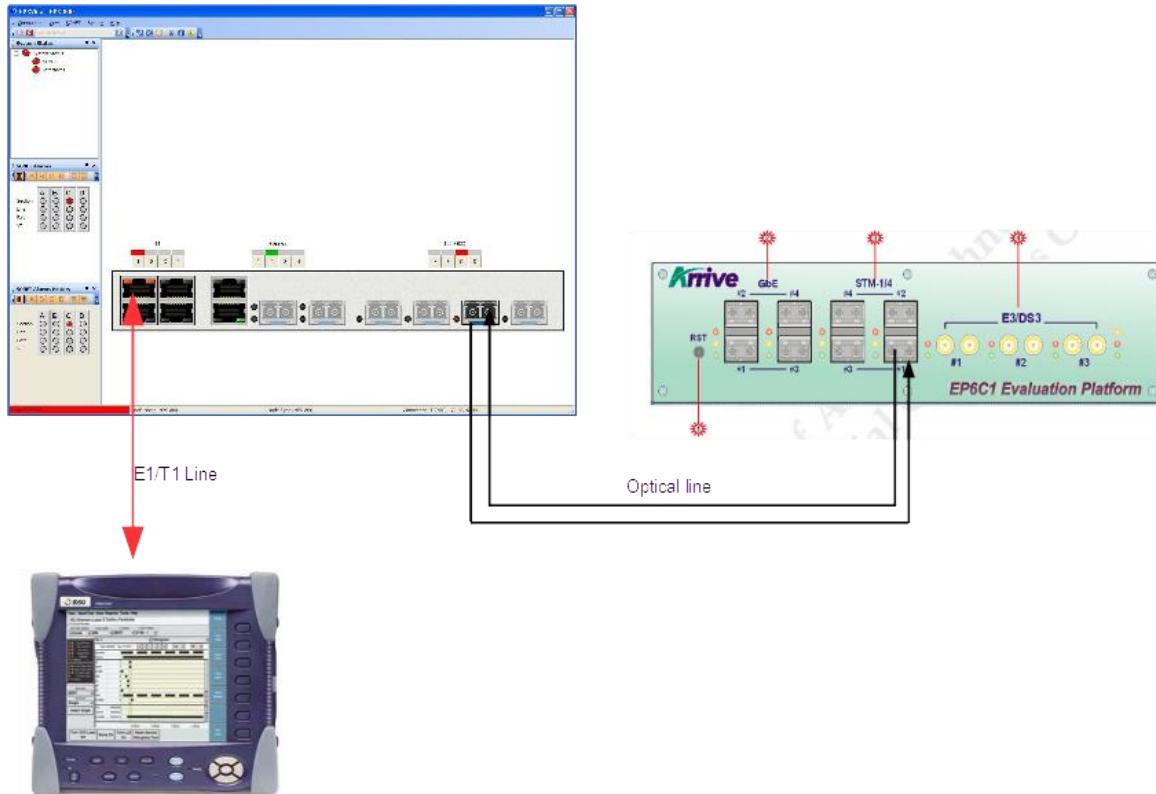
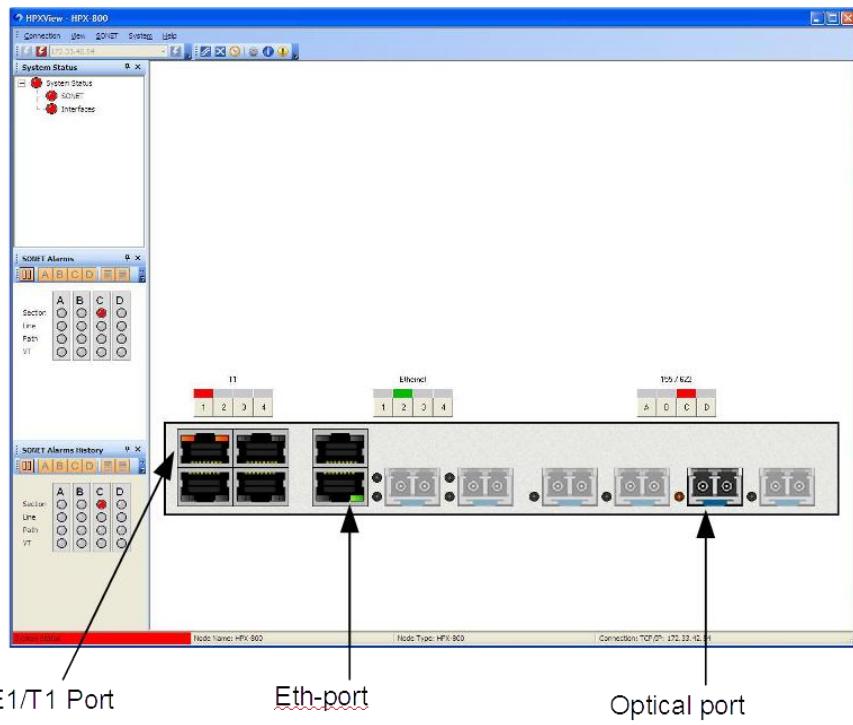
6.6 ADM Configuration

6.6.1 HPX box

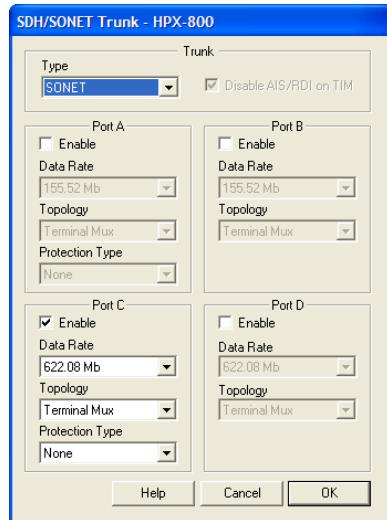
6.6.1.1 Telnet and basic setting:

- IP address: 172.33.42.54
- User: admin
- Password: none
- E1/T1 port number: 1

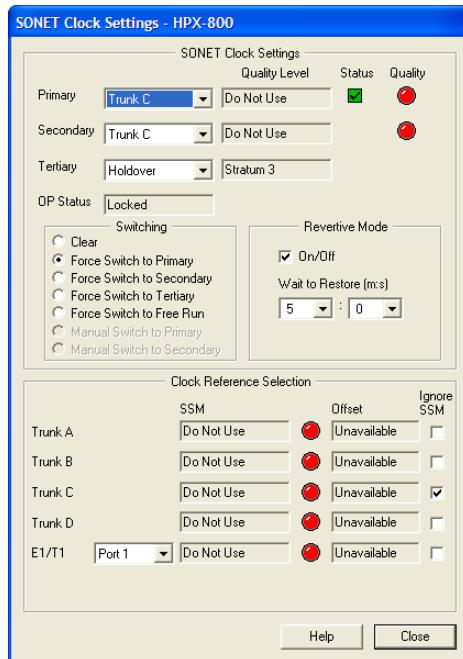
- Ethernet port number: 2
- Optical port number: C



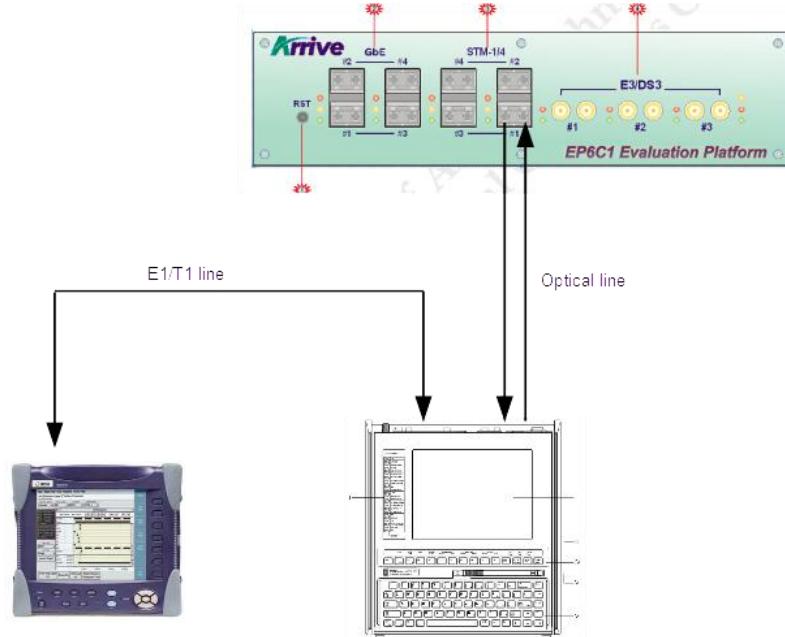
6.6.1.2 Trunk setting:



6.6.1.3 Clock setting

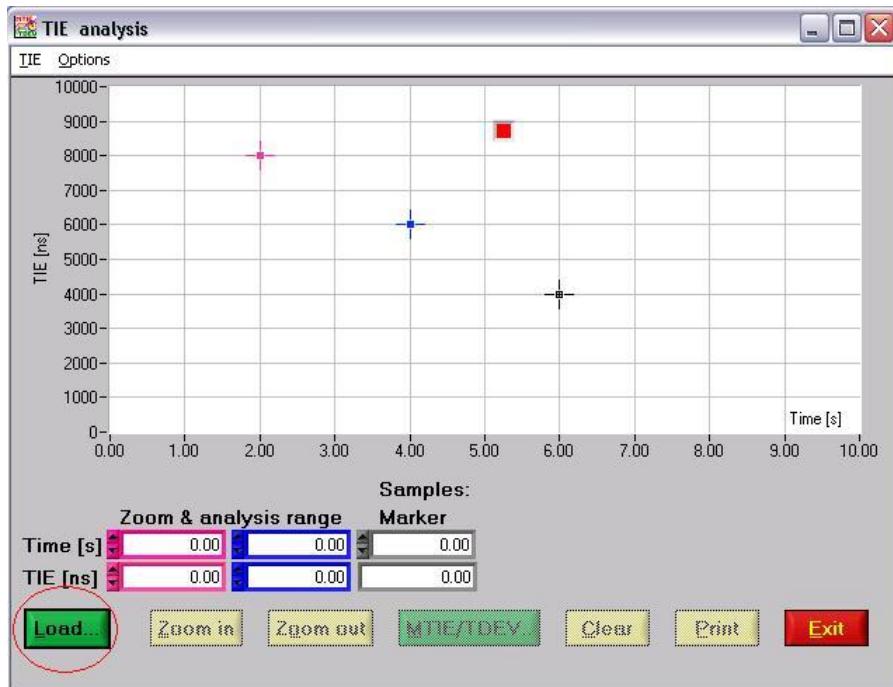


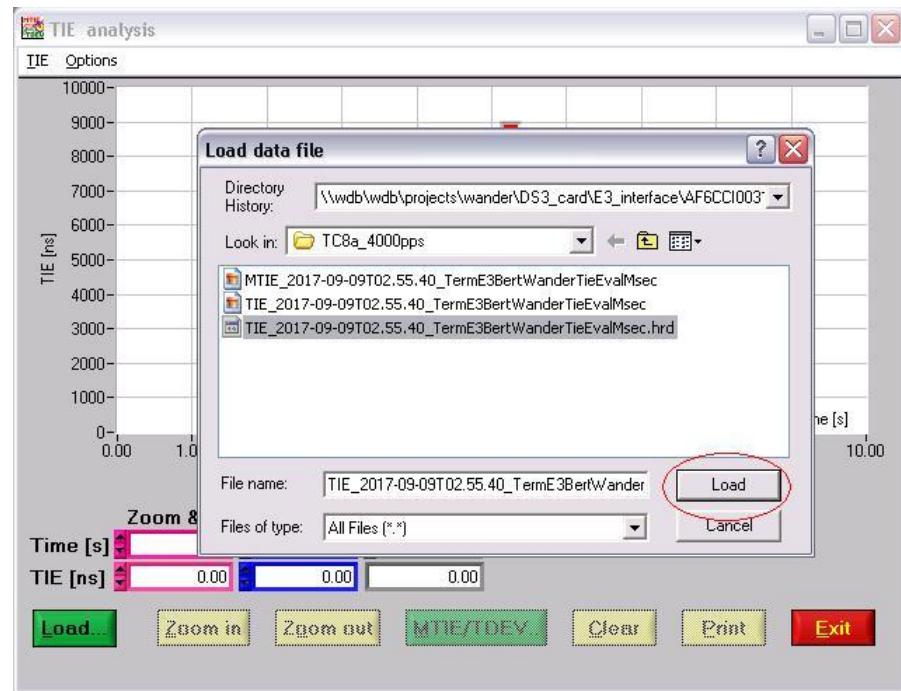
6.6.2 ANT20 configured as ADM



6.7 Get result and compare with Mask:

6.7.1 Load TIE result: Use Analysis TIE – MTIE – TDEV, select result to load



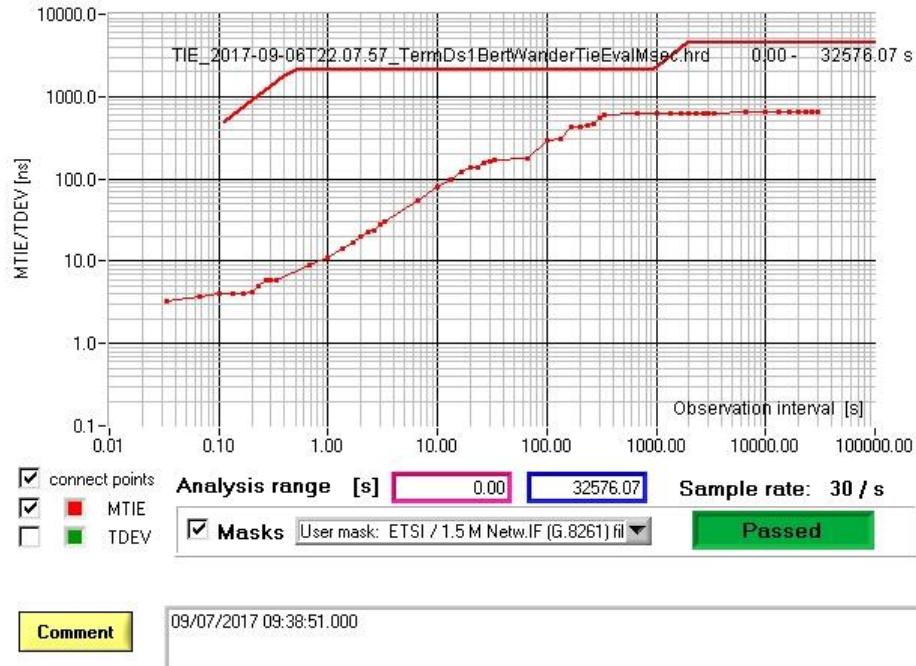


6.7.2 Load MTIE result: Select MTIE/TDEV tab and choose mark to compare

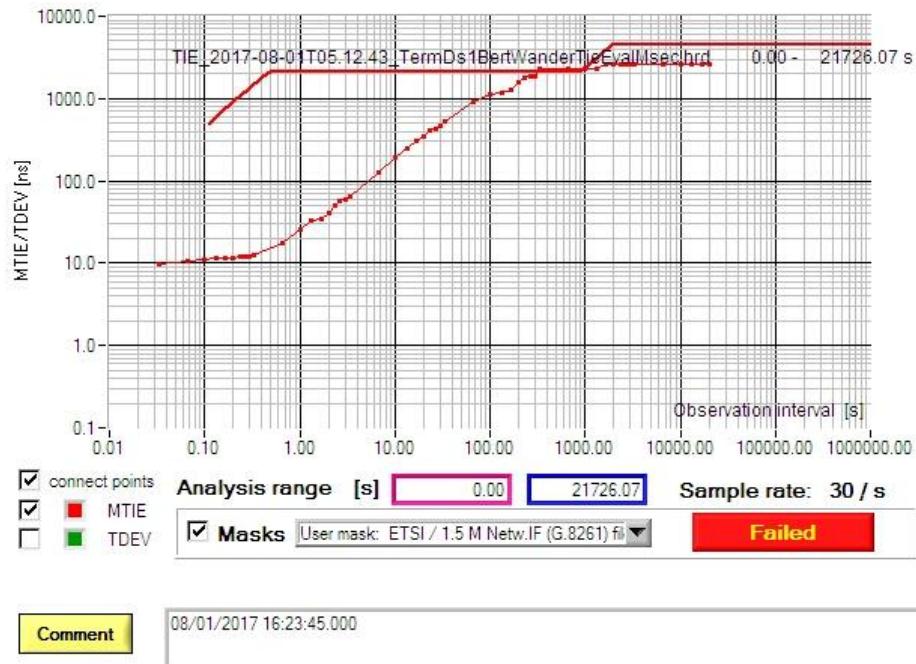


6.7.3 Passed/Failed Cases

6.7.3.1 Passes Case:



6.7.3.2 Failed Case:



6.7.4 Create timing mask:

- Use Notepad to create new mask
- Read standards about timing in the sections above
- The following picture is mask for G.8261-DS1

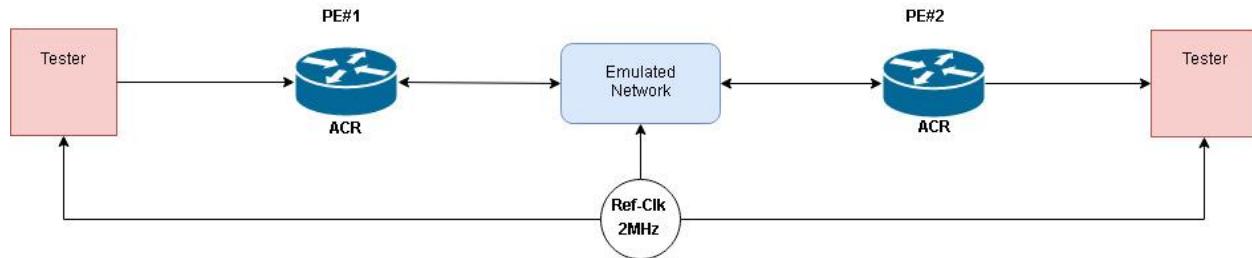
```
#      MTIE  0 = no Val.          TDEV  0 = no Val.
#      x[s]  y[ns]              x[s]  y[ns]
0.11,  495,                  0.1,   0
0.15,  675,                  0.1,   0
0.2,   900,                  0.2,   0
0.3,  1350,                  0.3,   0
0.4,  1800,                  0.5,   0
0.5,  2100,                  0.8,   0
1,    2100,                  1,    0
2,    2100,                  2,    0
3,    2100,                  3,    0
5,    2100,                  5,    0
8,    2100,                  8,    0
10,   2100,                 10,   0
20,   2100,                 20,   0
30,   2100,                 30,   0
32,   2100,                 40,   0
50,   2100,                 50,   0
64,   2100,                 80,   0
100,  2100,                100,   0
200,  2100,                200,   0
300,  2100,                300,   0
500,  2100,                500,   0
900,  2100,                800,   0
1000, 2330,                1000,  0
```

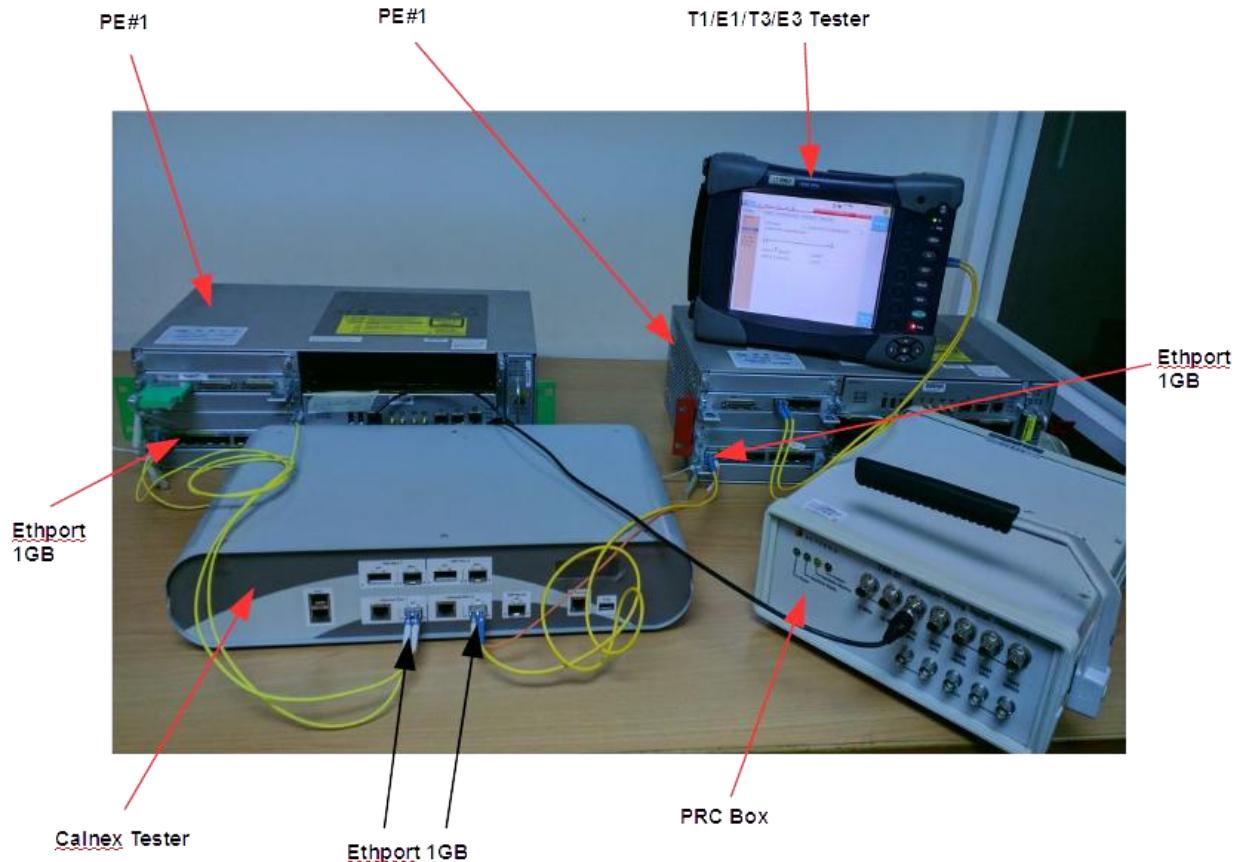
6.8 Some notice:

- Connect Tester and Cisco's board to patch panel → please check document of Cisco → <\\dv-hvminh\Share2Write\Design Validataion - Sub-Dept\AUDIT-GUIDELINE-DOCUMENT\Cisco>
- Change Tx frequency (ppm) → data did not hit
- In worst case, we need to await about 15 minutes after re-load test-case of G.8261.

6.9 The sample model:

6.9.1 Model Testing





6.9.2 Locked state:

- ACR was holdover

```
Router#show recovered-clock
Recovered clock status for subslot 0/4
-----
Clock      Type       Mode        CEM      Status     Frequency Offset(ppb)  Circuit-No
0          T1         ADAPTIVE    0        HOLDOVER   n/a                  0 (Port)      NA
Priority
```

- ACR was locked

```
Router# show recovered-clock

Recovered clock status for subslot 0/4
-----
Clock    Type      Mode       CEM     Status      Frequency Offset(ppb) Circuit-No
0        DS1       ADAPTIVE   0        ACQUIRED   n/a          0 (Port)
```

- DCR was holdover:

```
Router#show recovered-clock
Recovered clock status for subslot 0/4
-----
Clock      Type       Mode        CEM      Status      Frequency Offset(ppb)  Circuit-No
0          T1         DIFFERENTIAL 0        HOLDOVER    n/a                      0 (Port)     NA

Router#
```

- DCR was locked:

```
Router# show recovered-clock
Recovered clock status for subslot 0/4
-----
Clock      Type       Mode        CEM      Status      Frequency Offset(ppb)  Circuit-No
0          DS1        DIFFERENTIAL 0        ACQUIRED   n/a                      0 (Port)
```

6.10 Network jitter recommendations for network interface:

Network Interface	Standard	Bit Rate	Jitter Limits	
			Wide-Band (UI)	High-Band (UI)
SDH Transport	ITU-T G.825	STM-1e	1.5	0.075
		STM-1	1.5	0.15
		STM-4	1.5	0.15
		STM-16	1.5	0.15
		STM-64	1.5	0.15
SONET Transport	Telcordia GR-253	OC-1	1.5	0.15
		OC-3	1.5	0.15
		OC-12	1.5	0.15
		OC-48	1.5	0.15
		OC-192	1.5	0.15
PDH Transport	ITU-T G.823	2048 Kbps	1.5	0.2
		8448 Kbps	1.5	0.2
		34368 Kbps	1.5	0.15
		139264 Kbps	1.5	0.075
	ITU-T G.824 Telcordia GR-499	1544 Kbps	5	0.1
		6312 Kbps	3	0.1
		44736 Kbps	5	0.1
OTN Transport	ITU-T G.8251	OTU1	1.5	0.15
		OTU2	1.5	0.15
		OTU3	6	0.15
Synchronization	ITU-T G.823 ETSI 300 462-3-1	2048 Kbps PRC	0.05	N/A
		2048 Kbps SSU	0.05	N/A
		2048 Kbps SEC	0.5	0.2
		2048 Kbps PDH	1.5	0.2