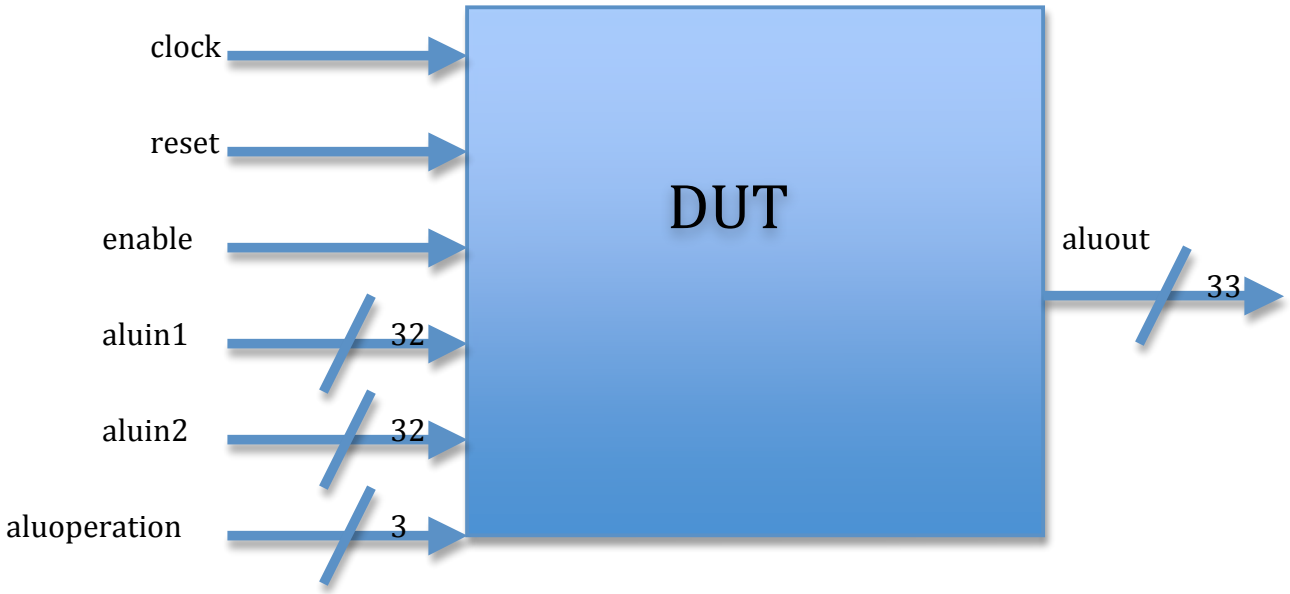
Specification for Design Under Test (DUT) for Lab #1



The Device Under Test for the first lab is a very simplistic ALU block. There are six inputs and one output as seen above.

Signal	Description
clock	Incoming clock signal
reset	Active High. Reset the DUT. Aluout should go to zero on reset and hold until new calculation is performed.
enable	Active High signal. When high, the operation on aluin1, aluin2, and aluoperation is performed and appears on aluout the next clock cycle.
aluin1	First Operand
aluin2	Second Operand
aluoperation	Type of operation to be performed
aluout	The result of the calculation

*Note, the aluopselect input is not used in this lab and does not influence the operation of the DUT.

aluoperation	Operation	Description
8'b001	ADD	aluin1 + aluin2
8'b010	SUB	aluin1 - aluin2
8'b011	NOT	{1'b0, ~{aluin2}}
8'b100	AND	{1'b0, {aluin1 & aluin2}}
8'b101	OR	{1'b0, {aluin1 | aluin2}}
8'b110	XOR	{1'b0, {aluin1 ^ aluin2}}