Chapter 1
Introduction to CMOS VLSI Design

Course Topics

- Introduction to CMOS circuits
- MOS transistor theory, processing technology

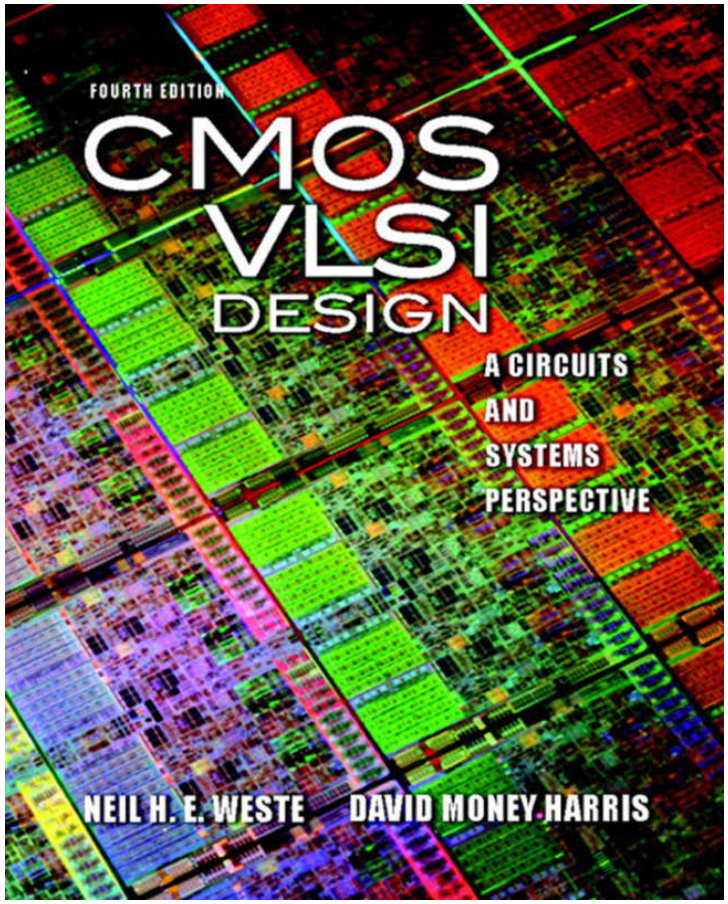
lí thuyết công nghệ xử lí

- CMOS circuit and logic design
- System design methods
- CAD algorithms for backend design

phần mềm máy tính hỗ trợ thiết kế

Course materials

- Textbook
  - Weste and Harris. *CMOS VLSI Design (4rd edition)*
  - *D. Hodges, H. G. Jackson, R.A. Saleh, Analysis and design of Digital integrated circuits*



sự tích hợp ở mức độ rất là cao, trong 1 diện tích tiết diện bán dẫn, có số lượng tích hợp rất lớn số transistor trên đó, vd như hiện nay trên 1 cm^2 con chip có thể tích hợp vài chục triệu hoặc hơn nữa số transistor trên diện tích 1 cm^2 như thế, sau này có thể cao hơn nhiều

Introduction

xử lí nhanh hơn, giá thành rẻ hơn, công suất tiêu thụ thấp hơn so với transistor BJT và các loại khác, do đó cho phép số lượng tích hợp rất lớn trên 1 đơn vị diện tích bán dẫn

- Integrated circuits: many transistors on one chip.
- *Very Large Scale Integration* (VLSI): very many
- *Complementary Metal Oxide Semiconductor*
  - Fast, cheap, low power transistors

chất bán dẫn oxit kim loại bổ sung

- Introduction: How to build your own simple CMOS chip
  - CMOS transistors
  - Building logic gates from transistors
  - Transistor layout and fabrication chế tạo
- Rest of the course: How to build a good CMOS chip

A Brief History

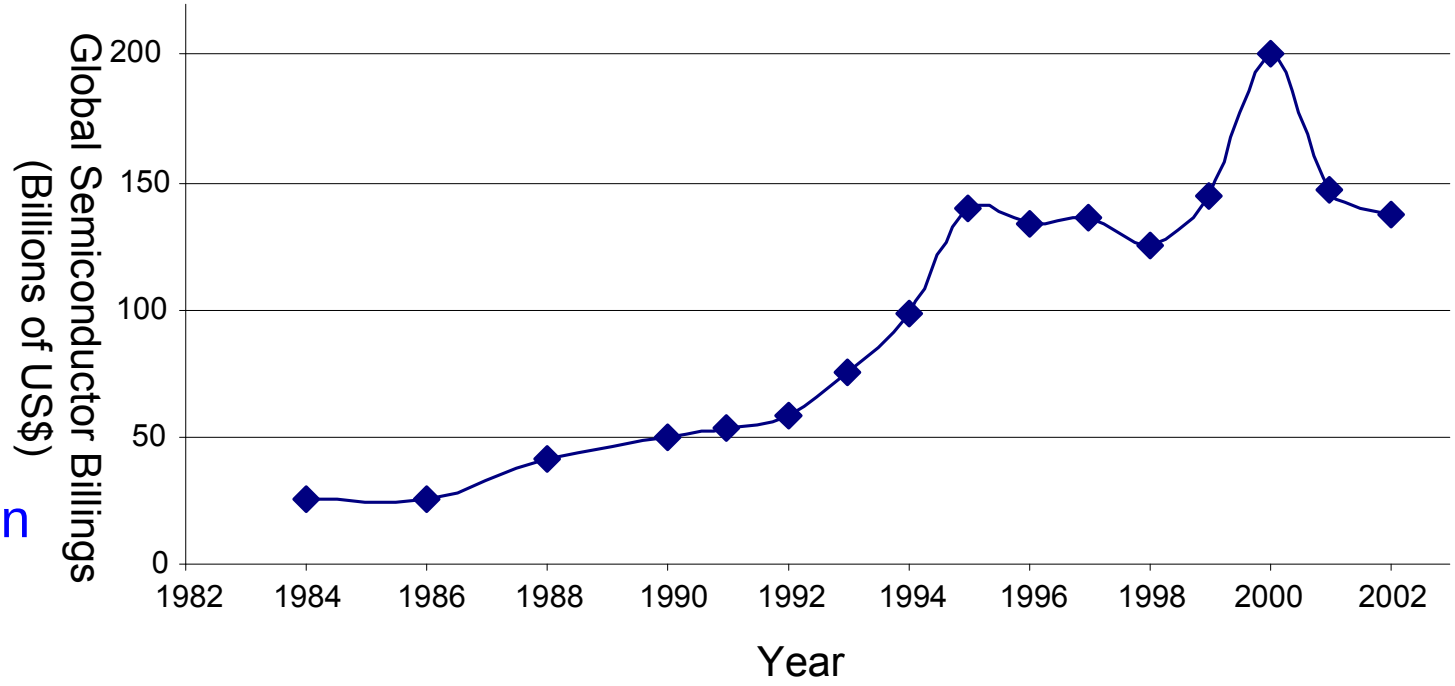
- 1958: First integrated circuit
  - Flip-flop using two transistors
  - Built by Jack Kilby at Texas Instruments
- 2003
  - Intel Pentium 4 μprocessor (55 million transistors)
  - 512 Mbit DRAM (> 0.5 billion transistors)
- 53% compound annual growth rate over 45 years
  - No other technology has grown so fast so long
- Driven by miniaturization of transistors
  - Smaller is cheaper, faster, lower in power!
  - Revolutionary effects on society

hợp chất, kép

Được thúc đẩy bởi sự thu nhỏ

Annual Sales

- 10^{18} transistors manufactured in 2003
  - 100 million for every human on the planet

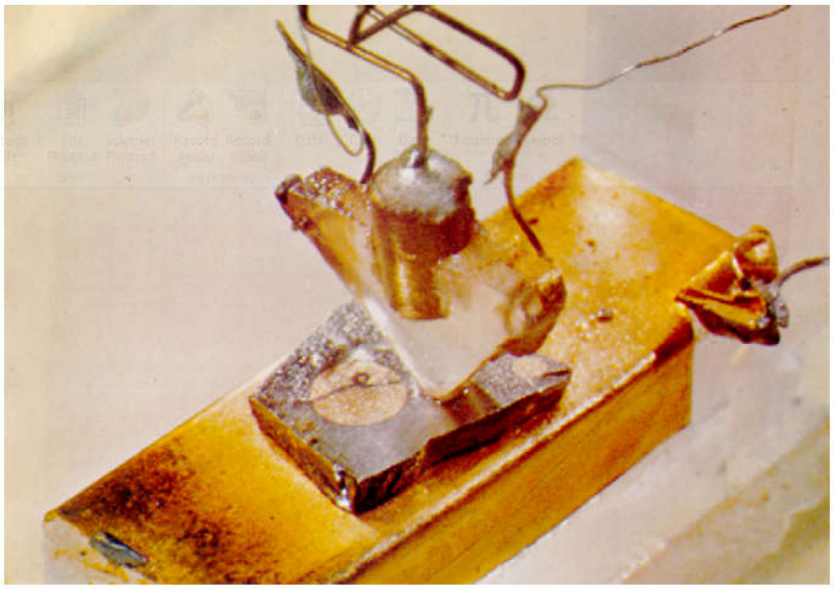


hóa đơn

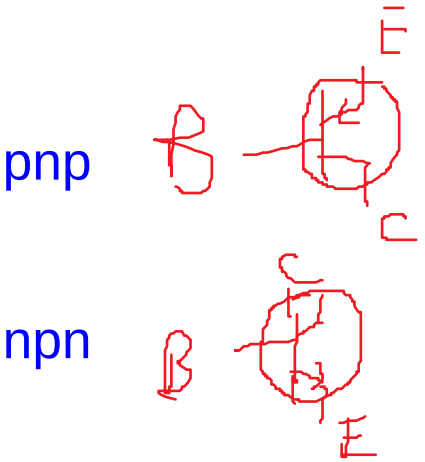
Invention of the Transistor

Ống chân không

- Vacuum tubes ruled in first half of 20th century
  Large, expensive, power-hungry, unreliable
- 1947: first point contact transistor
  - John Bardeen and Walter
  - Read *Crystal Fire*
    by Riordan, Hoddeson



Transistor Types



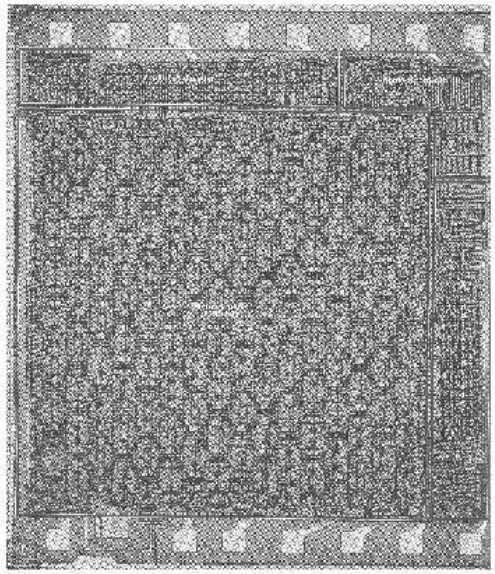
lưỡng cực

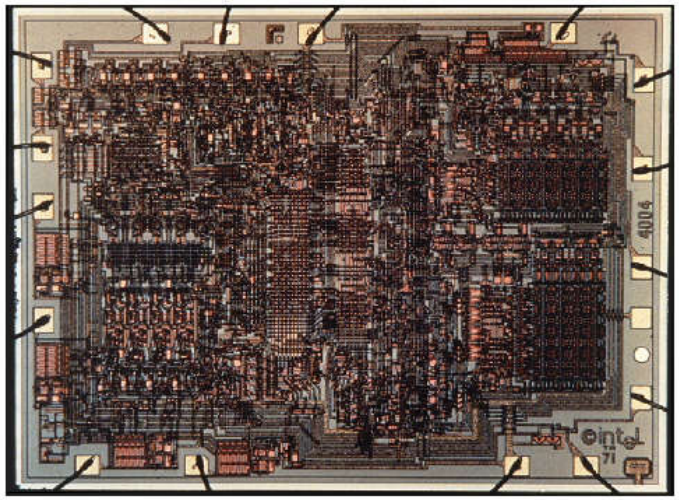
- Bipolar transistors
  - npn or pnp silicon structure
  - Small current into very thin base layer controls large currents between emitter and collector
  - Base currents limit integration density
- Metal Oxide Semiconductor Field Effect Transistors
  - nMOS and pMOS MOSFETS
  - Voltage applied to insulated gate controls current between source and drain
  - Low power allows very high integration

cách điện

MOS Integrated Circuits

- 1970's processes usually had only nMOS transistors
  - Ine





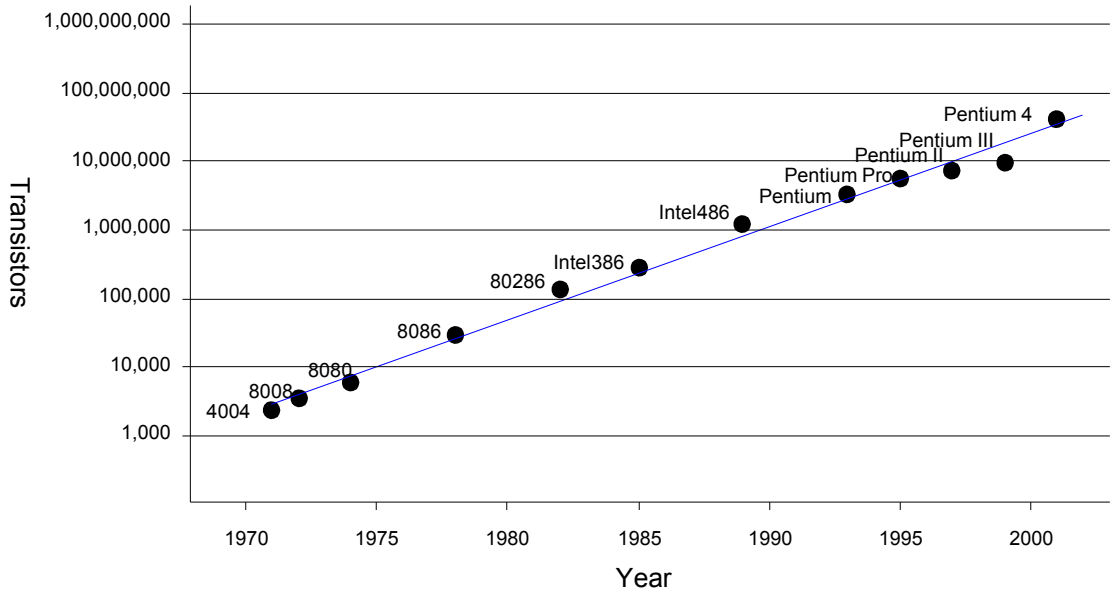
Intel 1101 256-bit SRAM Intel 4004 4-bit μProc

- 1980s-present: CMOS processes for low idle power

Moore's Law

- 1965: Gordon Moore plotted transistor on each chip
  - Fit straight line on semilog scale
  - Transistor counts have doubled every 26 months

tuyến tính



Integration Levels

SSI: 10 gates

MSI: 1000 gates

LSI: 10,000 gates

VLSI: > 10k gates

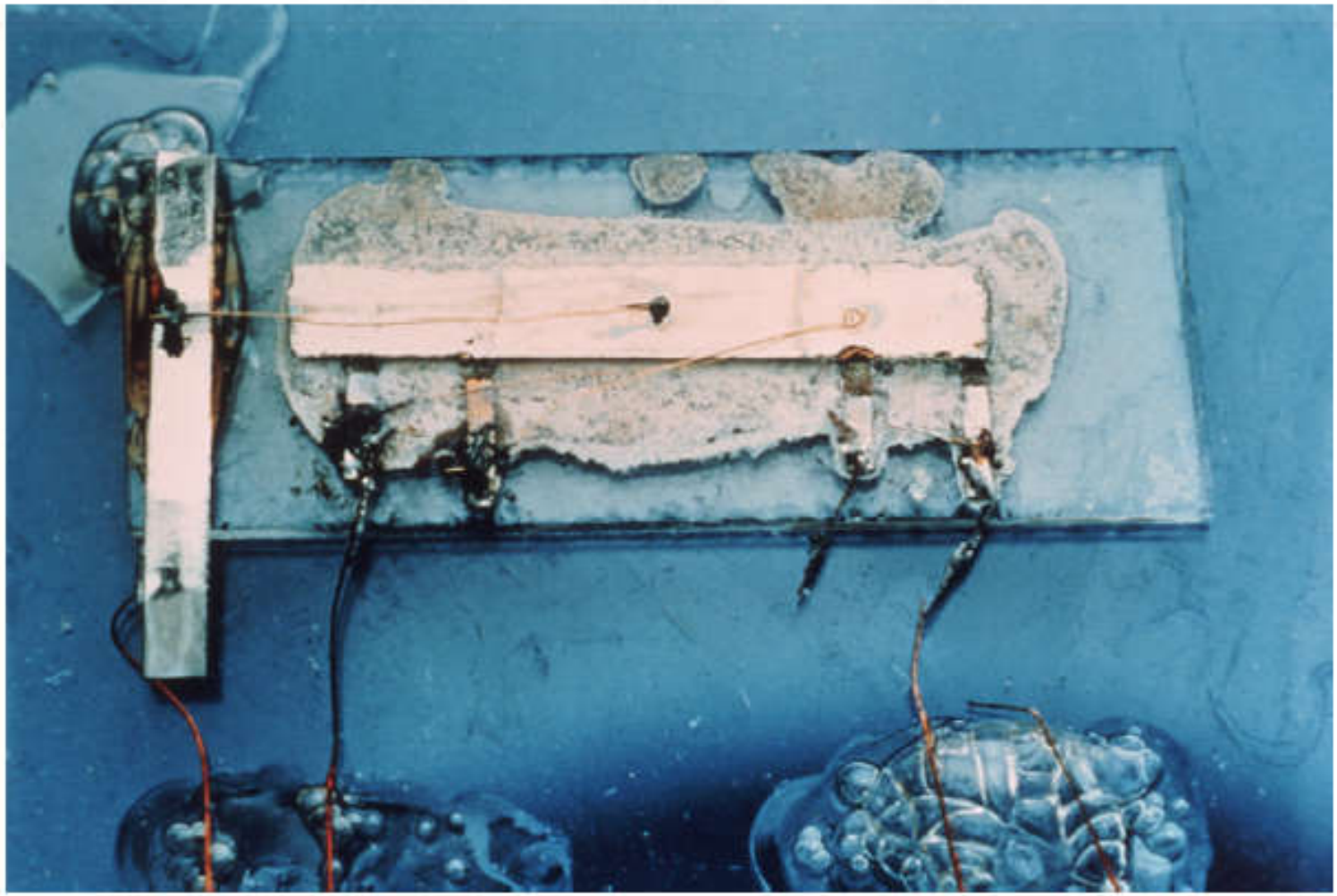
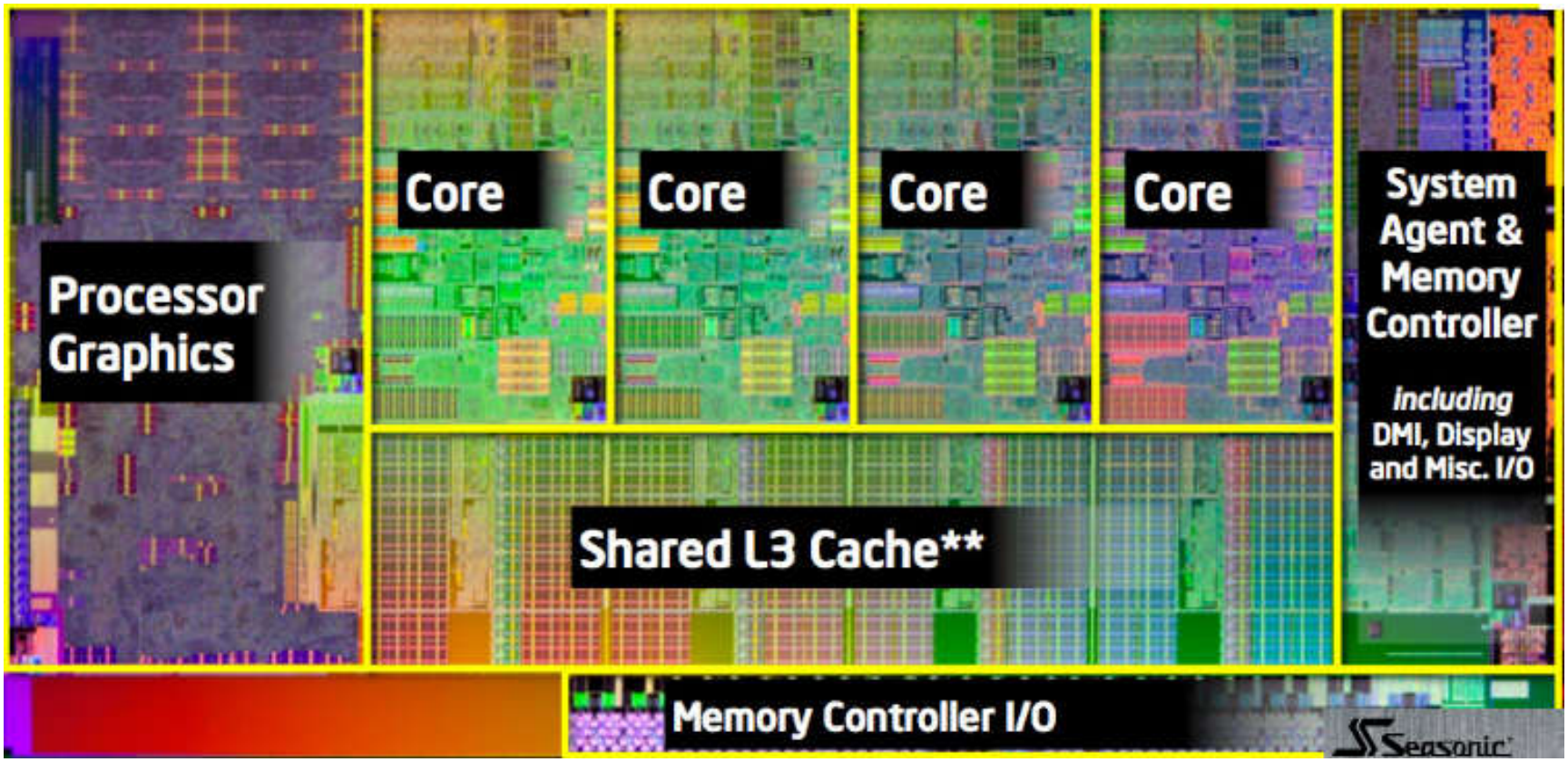


Fig. 5. The first integrated germanium circuit built by J. Kilby at Texas Instruments in 1958.

Ge


Processor Graphics
Core
Core
Core
Core
System Agent & Memory Controller
including DMI, Display and Misc. I/O
Shared L3 Cache**
Memory Controller I/O
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microarchitecture

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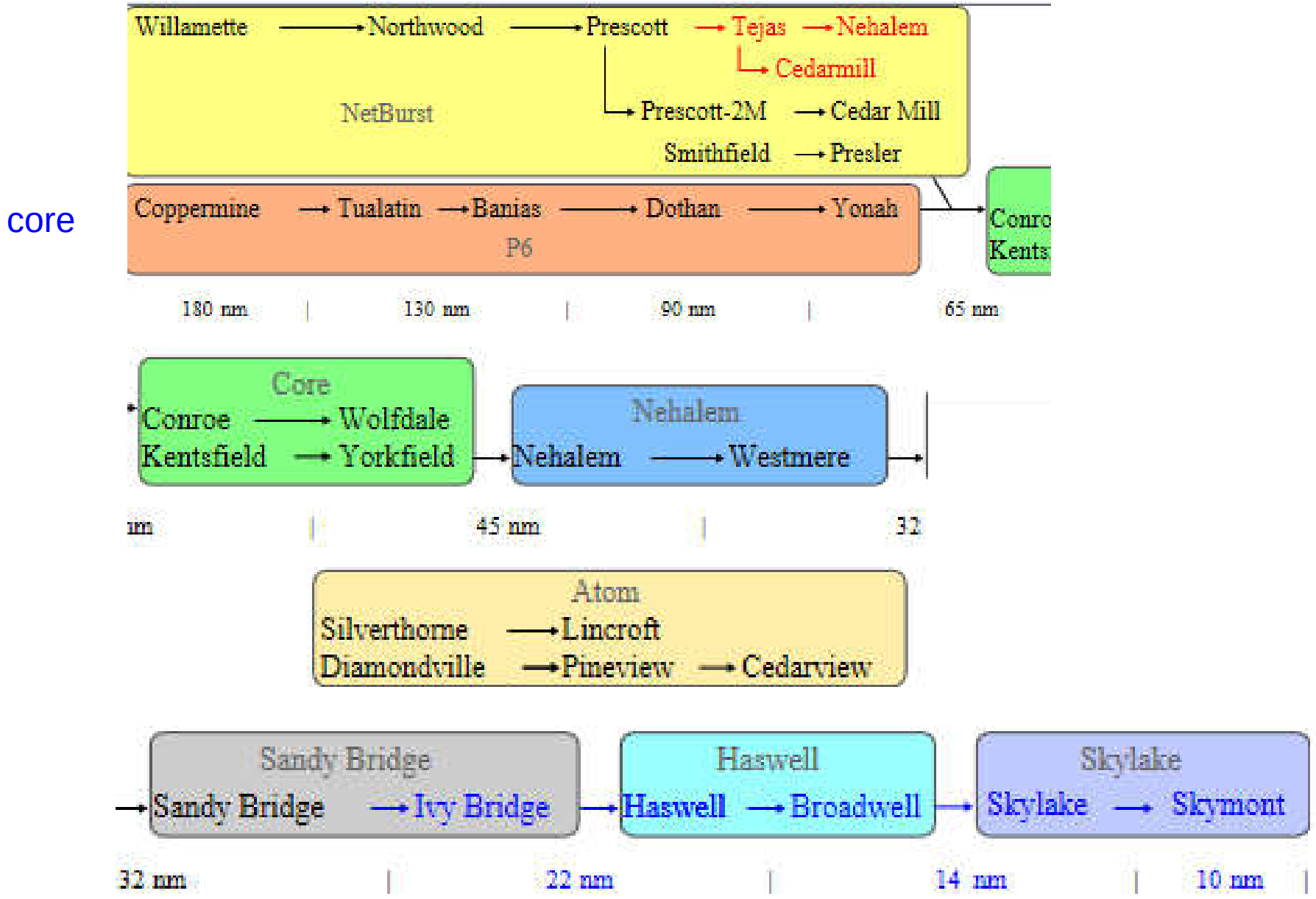
core

core

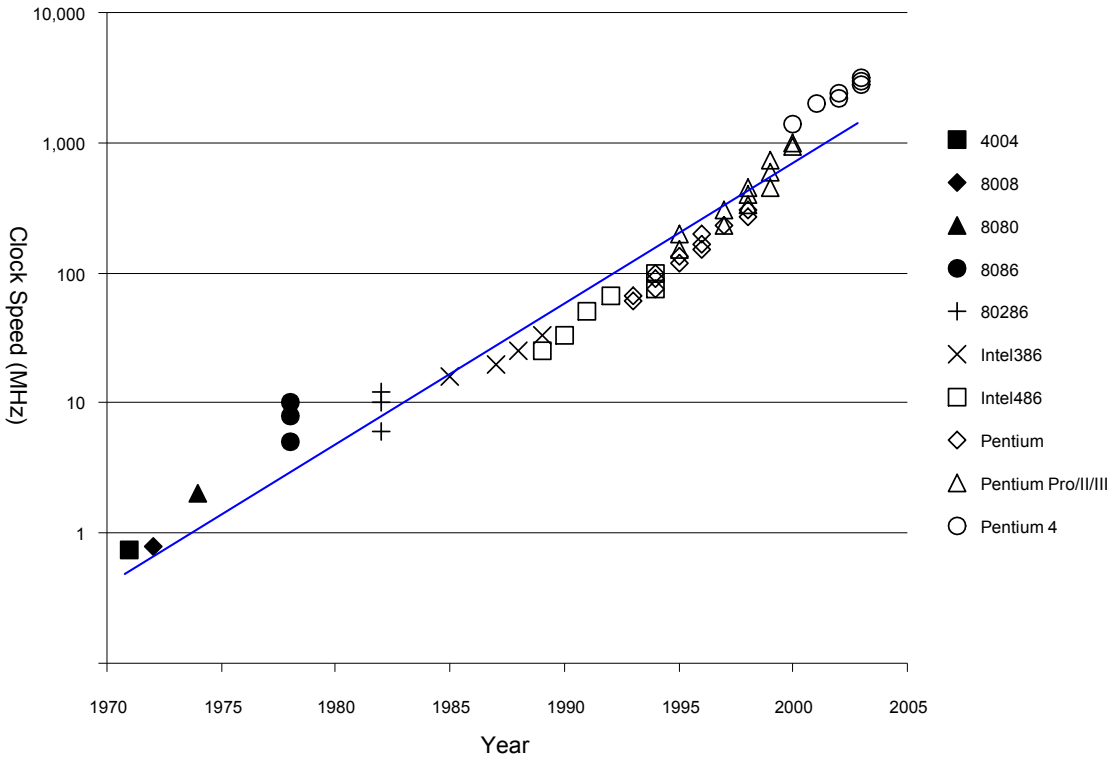


hệ lụy

Corollaries

theo hàm mũ

- Many other factors grow exponentially
  - Ex: clock frequency, processor performance



silicon là 1 nguyên tố nhóm IV của bảng hệ thống tuần hoàn, đặc trưng của nó có 4 cái electron hóa trị, vì vậy sẽ có liên kết bền vững với 4 cái nguyên tử si xung quanh nó để tạo trạng thái bền vững

Silicon Lattice

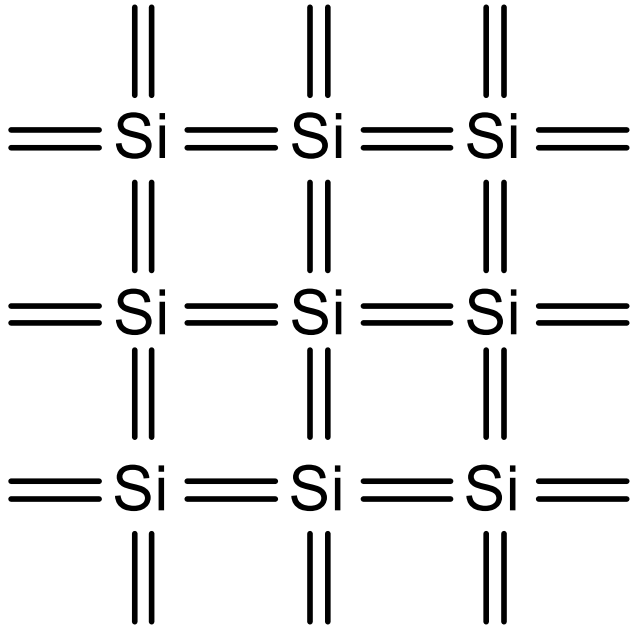
mạng tinh thể

cơ chất

- Transistors are built on a silicon substrate
- Silicon is a Group IV material

Hình thành mạng tinh thể với các liên kết tới bốn nguyên tử xung quanh

- Forms crystal lattice with bonds to four neighbors



nếu pha tạp chất thuộc nhóm V (vd Arsenic) vào khối silic nguyên chất, chúng ta sẽ có bán dẫn loại n, nếu pha tạp chất là Bor (thuộc nhóm III bảng hệ thống tuần hoàn) thì chúng ta có bán dẫn loại p

Dopants

tạp chất

Bor có 3 electron tự do, liên kết với các Silic thì thiếu mất 1 electron, vì vậy ta gọi nó là lỗ trống, tạo thành bán dẫn loại p

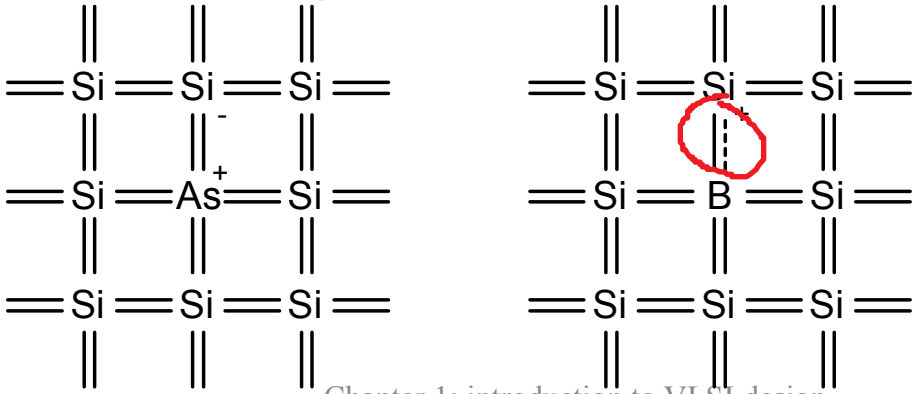
- Silicon is a semiconductor

Silicon tinh khiết không có hạt tải điện tự do và dẫn điện kém

- Pure silicon has no free carriers and conducts poorly

độ dẫn nhiệt

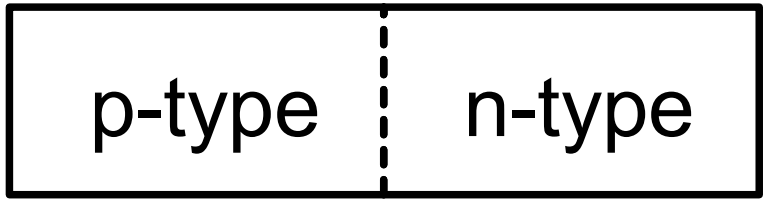
- Adding dopants increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)



chuyển tiếp p-n

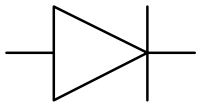
p-n Junctions

- A junction between p-type and n-type semiconductor forms a diode.
- Current flows only in one direction



ứng dụng dễ thấy nhất là ghép bán dẫn loại p và loại n thì sẽ có 1 cái diode, 1 bên là anode và 1 bên là cathode, sẽ cho dòng điện dẫn theo 1 chiều nhất định

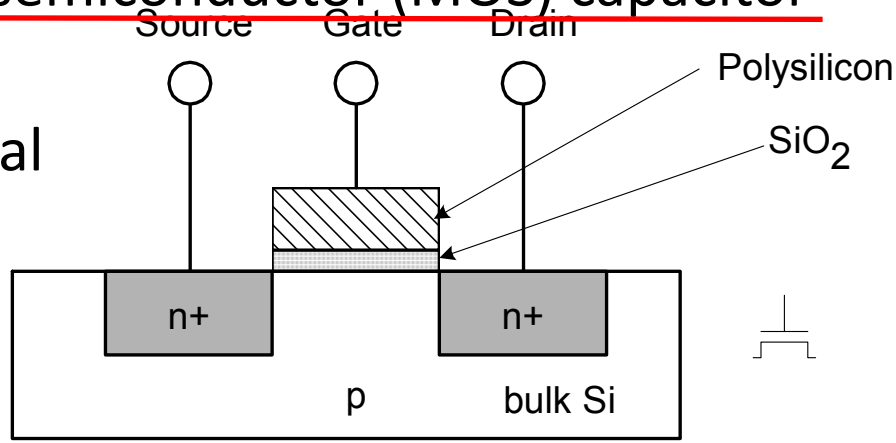
anode cathode



nMOS Transistor

1 transistor nMOS gồm 4 cực

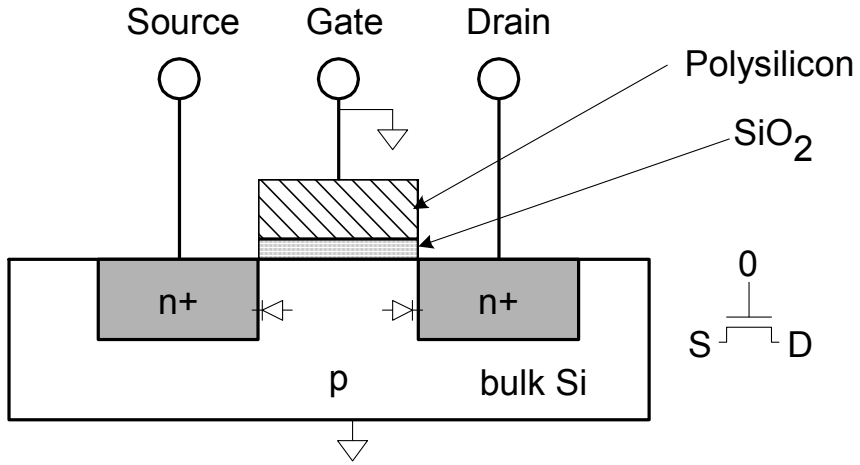
- Four terminals: gate, source, drain, body (máng, đế)
- Gate – oxide – body stack looks like a capacitor (tụ điện)
  - Gate and body are conductors
  - SiO_2 (oxide) is a very good insulator (chất cách điện)
  - Called metal – oxide – semiconductor (MOS) capacitor
  - Even though gate is no longer made of metal



đế của nó là bán dẫn loại p, trên đó ngta tạo ra 2 miếng bán dẫn loại n 2 bên, 1 cái cực source, 1 cái cực drain. n+ có nghĩa là bán dẫn loại n mà ngta bổ sung, tăng cường những cái tạp chất. ở giữa ngta tạo thành 1 lớp oxide (SiO2), là 1 lớp cách điện. Trên đó ngta làm 1 cái điện cực bằng polysilicon hoặc là metal kim loại, kết nối tạo thành cổng gate. => transistor nMOS hoàn chỉnh

nMOS Operation

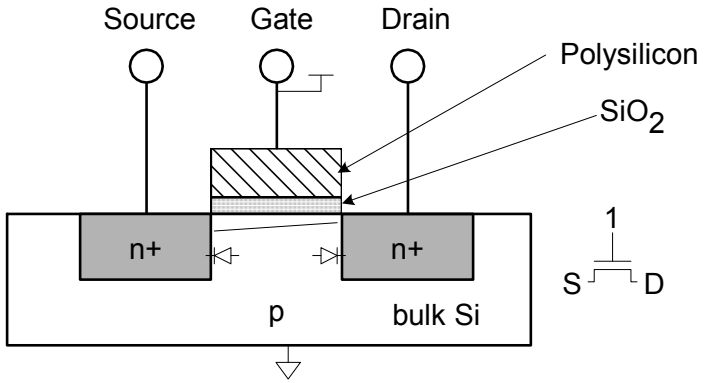
- Body is commonly tied to ground (0 V)
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF



nMOS Operation Cont.

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON

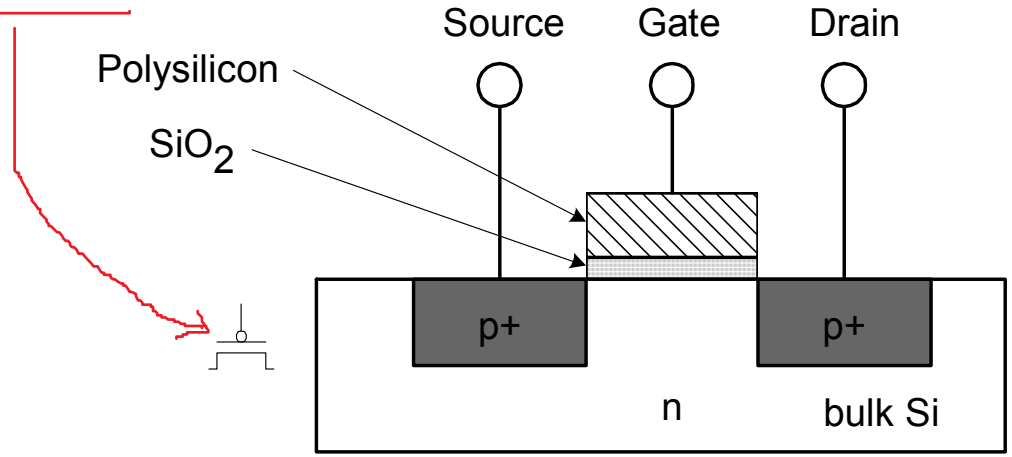
đảo ngược



pMOS Transistor

pha tạp chất đảo ngược

- Similar, but doping and voltages reversed
  - Body tied to high voltage (V_{DD})
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior



transistor pMOS cũng có cực g, s, d và body. Để trên 1 cái đế bán dẫn loại n, 2 khối bán dẫn tương ứng sẽ là bán dẫn loại p. p+ có nghĩa là ho cho nhiều tạp chất. Trên đó sẽ có 1 lớp SiO2 oxide và 1 cái điện cực polysilicon hoặc metal kim loại, tạo thành cái cổng gate

Power Supply Voltage

- GND = 0 V
- In 1980's, V_{DD} = 5V
- V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny transistors
  - Lower V_{DD} saves power
- V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, …

sau này để giảm công suất tiêu thụ cho transistor, ngta tìm cách giảm nguồn Vdd xuống, việc giảm điện áp cung cấp sẽ giảm rất hiệu quả công suất tiêu thụ của transistor, giảm tổng công suất tiêu thụ của toàn bộ cái vi mạch của mình

nhỏ bé

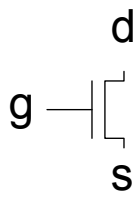
IMPORTANT

Transistors as Switches

transistor MOS có vùng hoạt động rất rộng, nhưng đối với thiết kế IC số, chúng ta chỉ quan tâm đến cái khoảng mà trong đó transistor hoạt động như 1 cái switch, tương đương là on hay off

- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain

nMOS

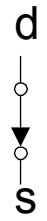


g = 0

hở mạch
vì ko có
sự di chuyển
của các electron,
ko có dòng điện

OFF

g = 1

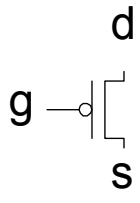


ON

có electron di
chuyển giữa s và
d, nên có dòng
chạy từ d xuống
s, tương đương
sẽ nối mạch ON

ngược lại

pMOS



g = 0

đóng mạch, có 1 cái
dòng điện đổ xuống

ON

g = 1

OFF

hở mạch OFF

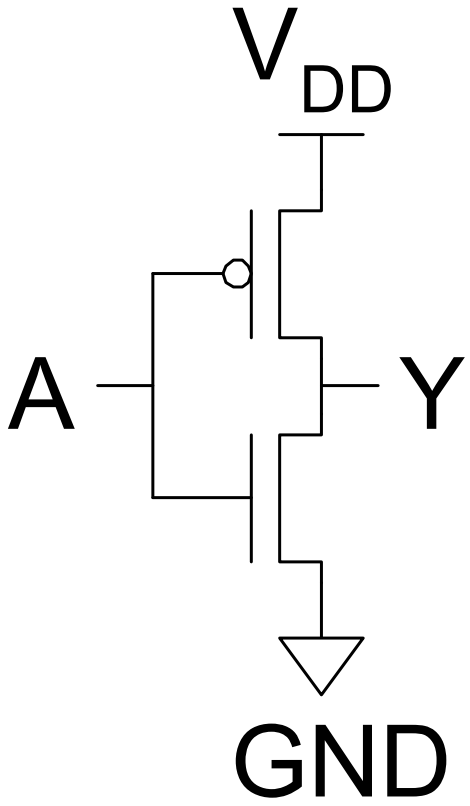
hiệu điện thế đưa
vào cực g với mức logic tương ứng

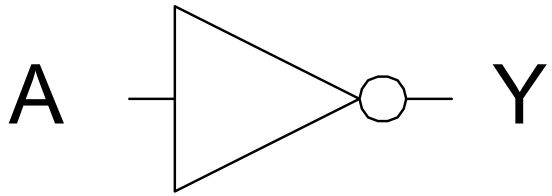
CMOS Inverter

đảo

ghép nối 2 cái transistor liên hợp như hình, nMOS ở dưới, pMOS ở trên, ngõ vào A sẽ điều khiển chân gate của 2 transistor này. ngõ ra Y sẽ ngõ ra của cổng inverter chúng ta thiết kế

A	Y
0	
1	



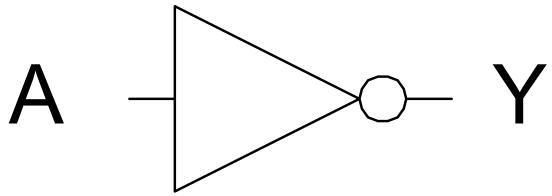


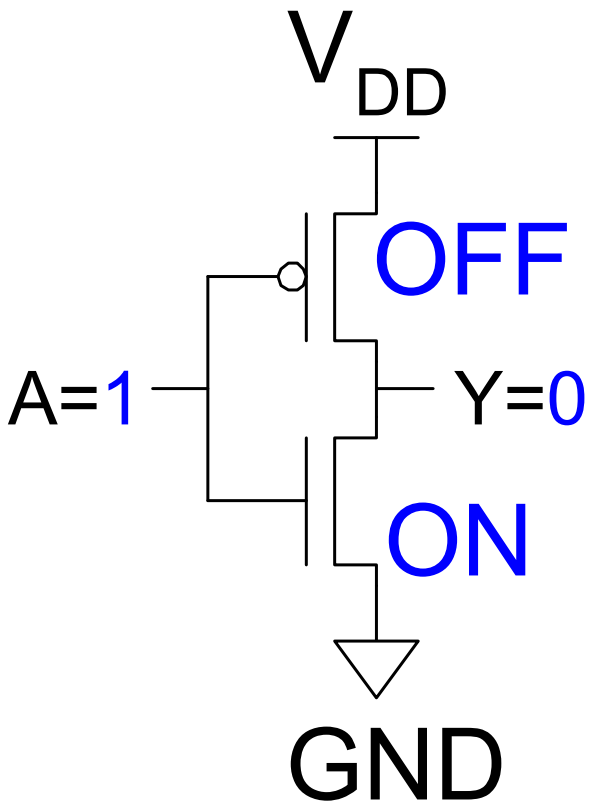
kí hiệu điện

A = 1, chân g của cái pMOS ở trên và chân g của nMOS ở dưới đều = 1, đối với nMOS, chân g bằng 1 thì transistor dẫn ON, coi như nối mạch. Ngược lại vs pMOS thì hở mạch OFF => Y nối xuống GND => Y=0

CMOS Inverter

A	Y
0	
1	**0**

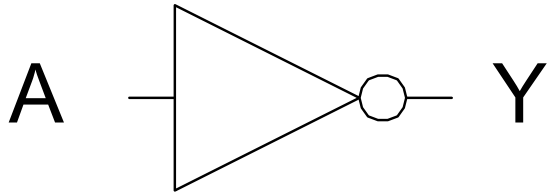


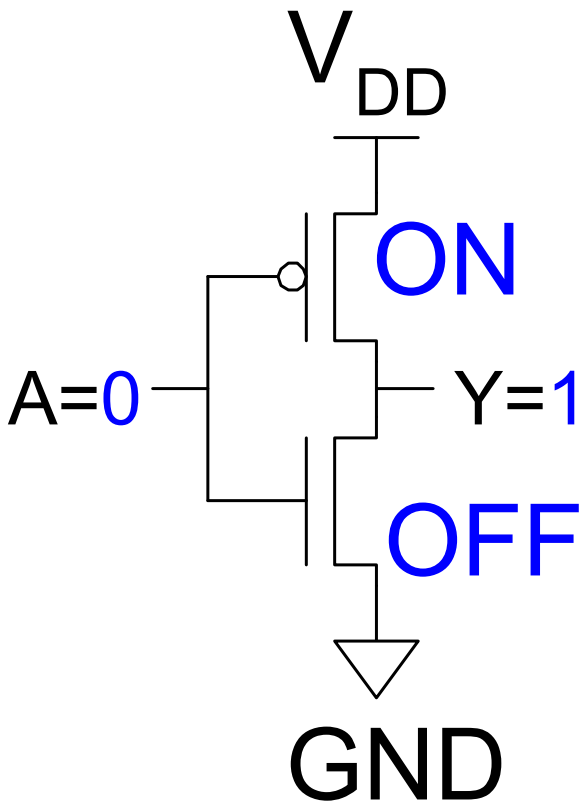


A=0, g dưới =0, suy ra OFF hở mạch, có nghĩa là cắt ra, ngược lại ở trên là ON, Y sẽ nối lên nguồn => Y=1

CMOS Inverter

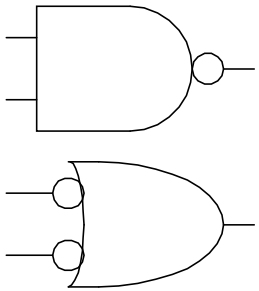
A	Y
0	**1**
1	0

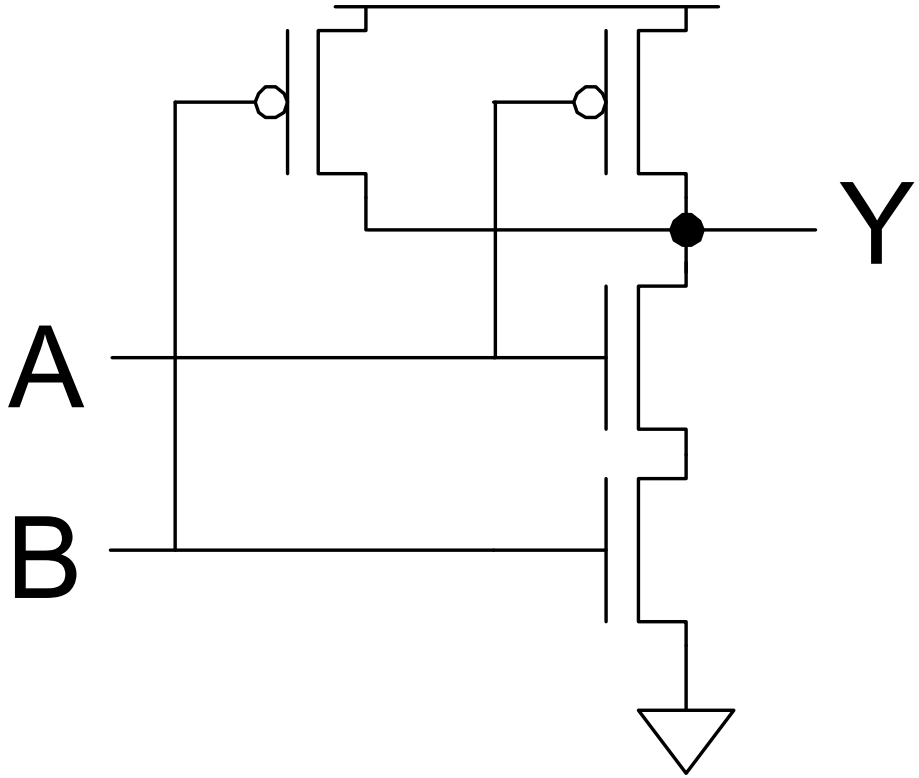




CMOS NAND Gate

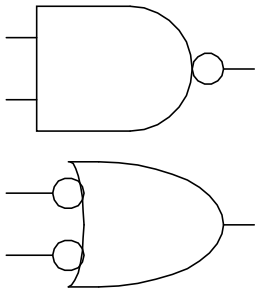
A	B	Y
0	0	
0	1	
1	0	
1	1	

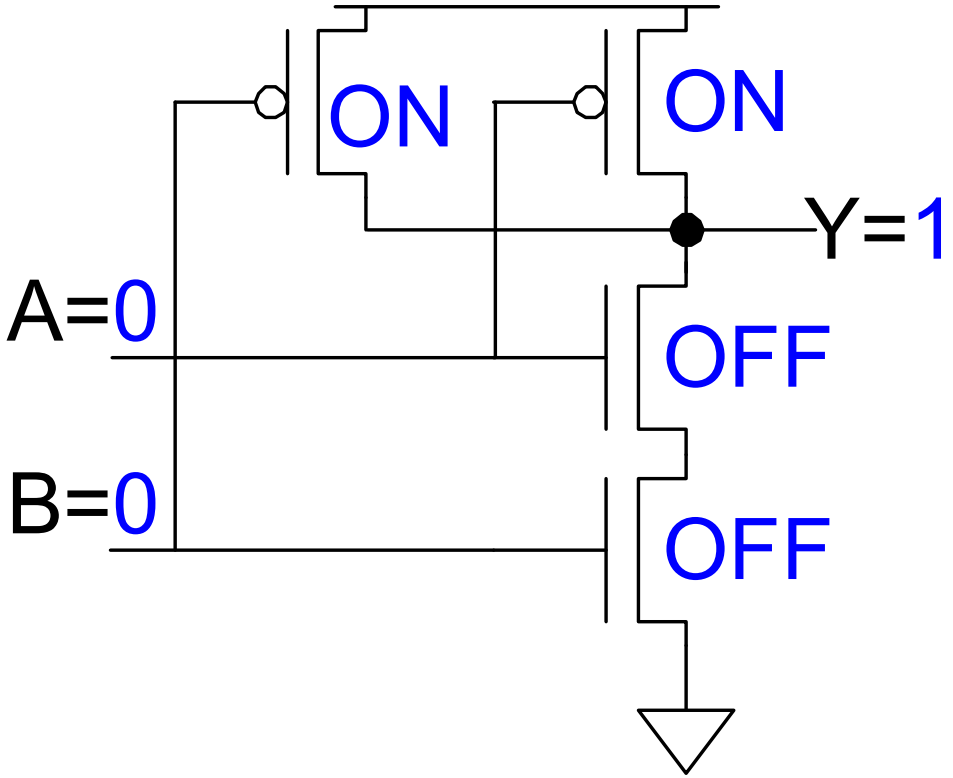




CMOS NAND Gate

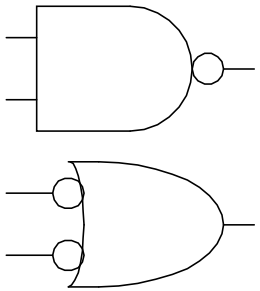
A	B	Y
0	**0**	**1**
0	1	
1	0	
1	1	

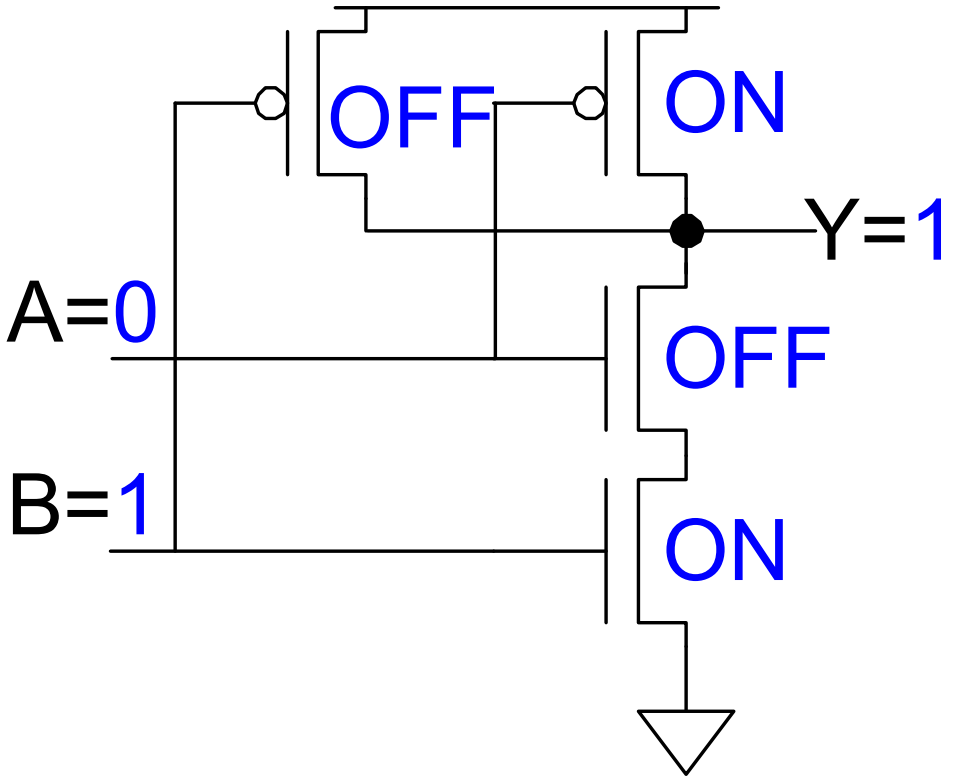




CMOS NAND Gate

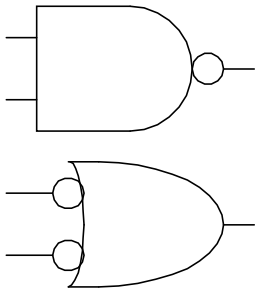
A	B	Y
0	0	1
0	**1**	**1**
1	0	
1	1	

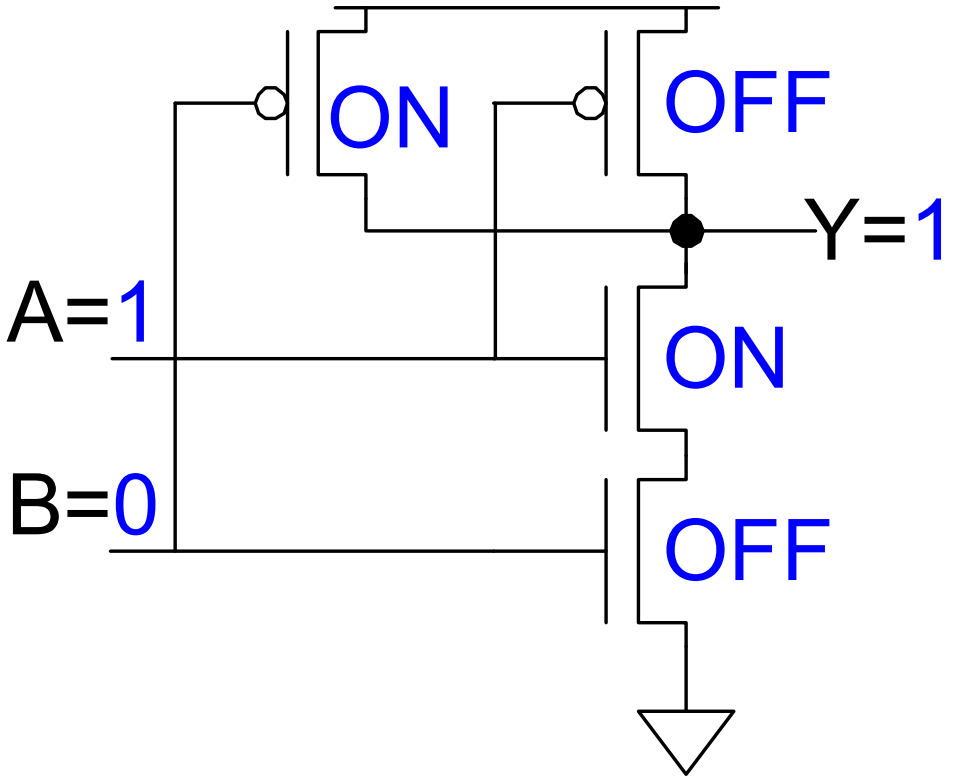




CMOS NAND Gate

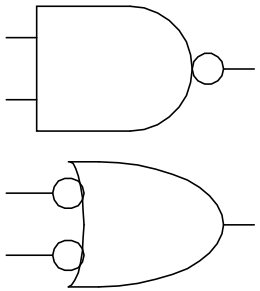
A	B	Y
0	0	1
0	1	1
1	**0**	**1**
1	1	

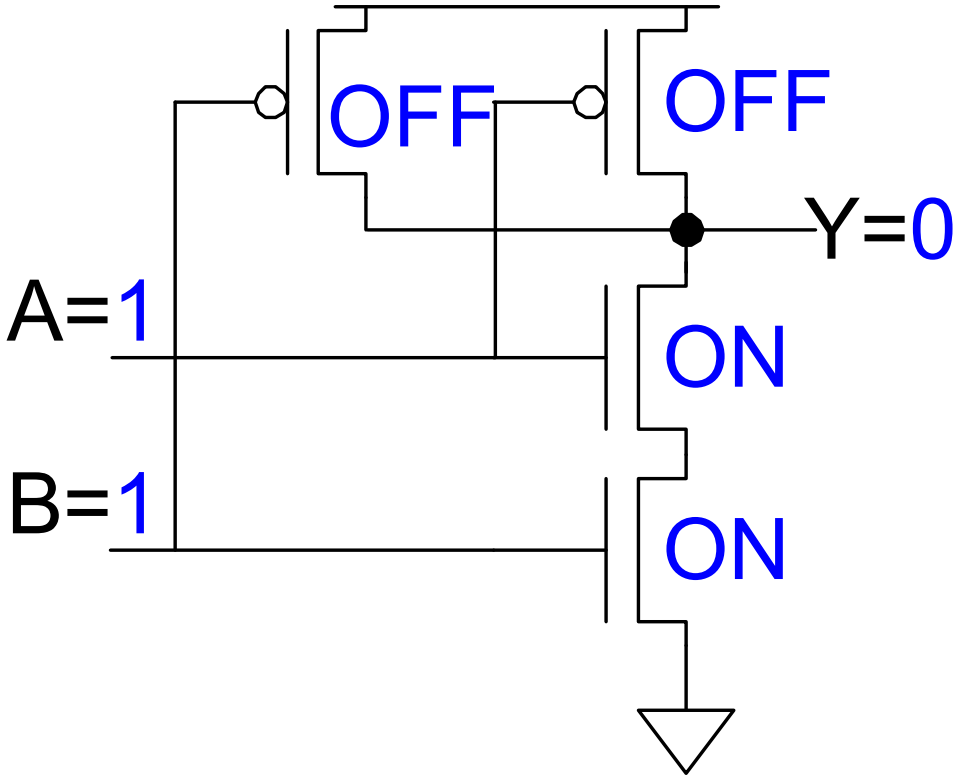




CMOS NAND Gate

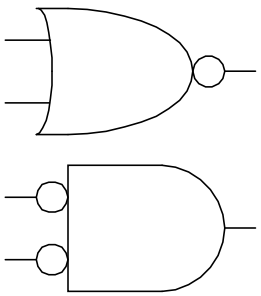
A	B	Y
0	0	1
0	1	1
1	0	1
1	**1**	**0**

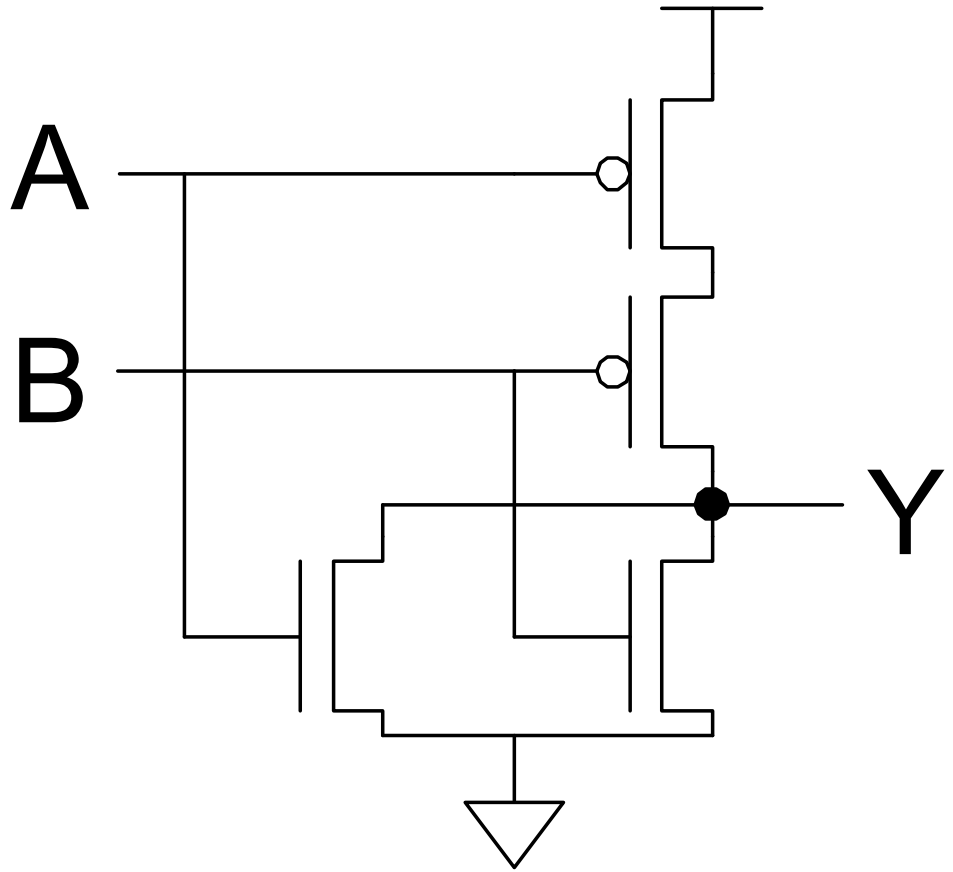




CMOS NOR Gate

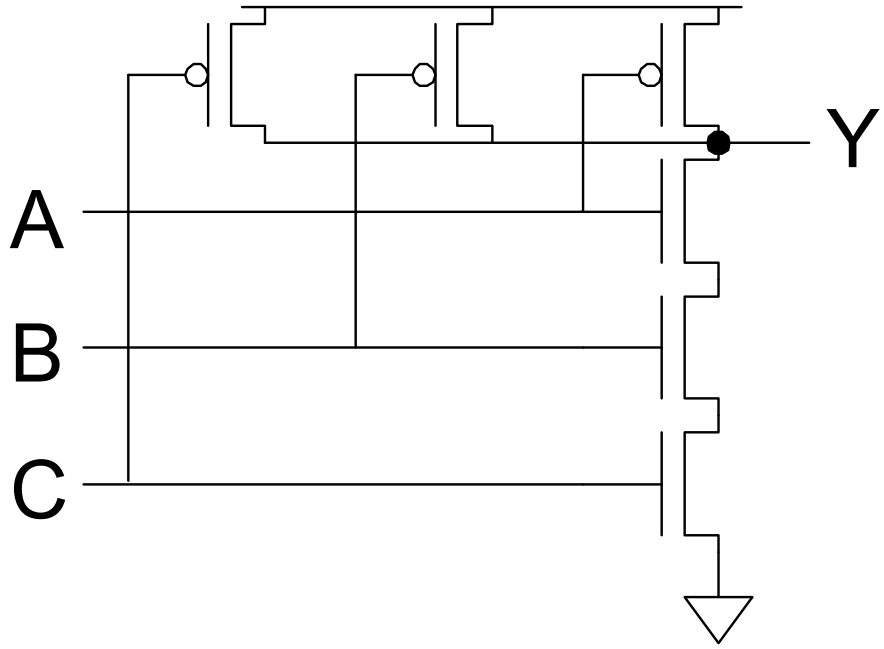
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0





3-input NAND Gate

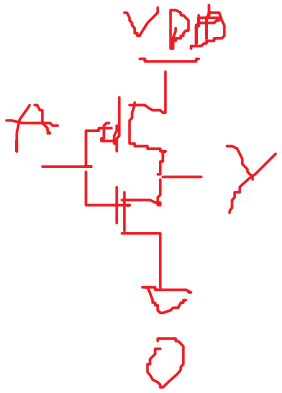
- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0



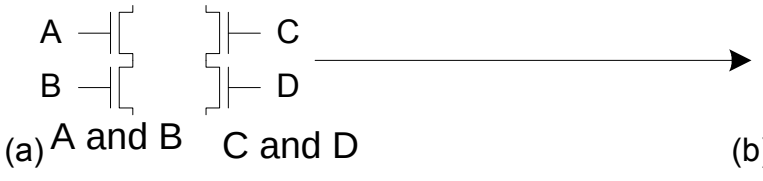
Compound Gates

- *Compound gates* can do any inverting function
- Ex:

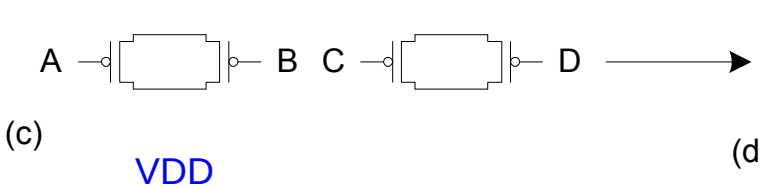
$$Y = \overline{A \cdot B + C \cdot D}$$ (AND-AND-OR-INVERT, AOI22)



inverter

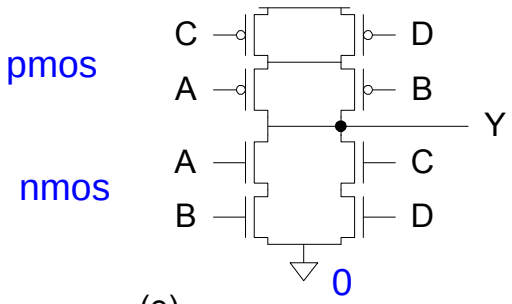


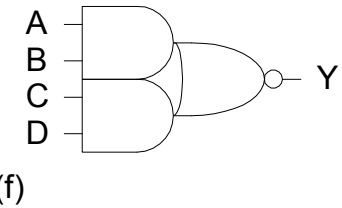
1, nmos
AND: serial
OR: parallel



2. DeMorgan's Law

3. pmos
AND: parallel
OR: serial



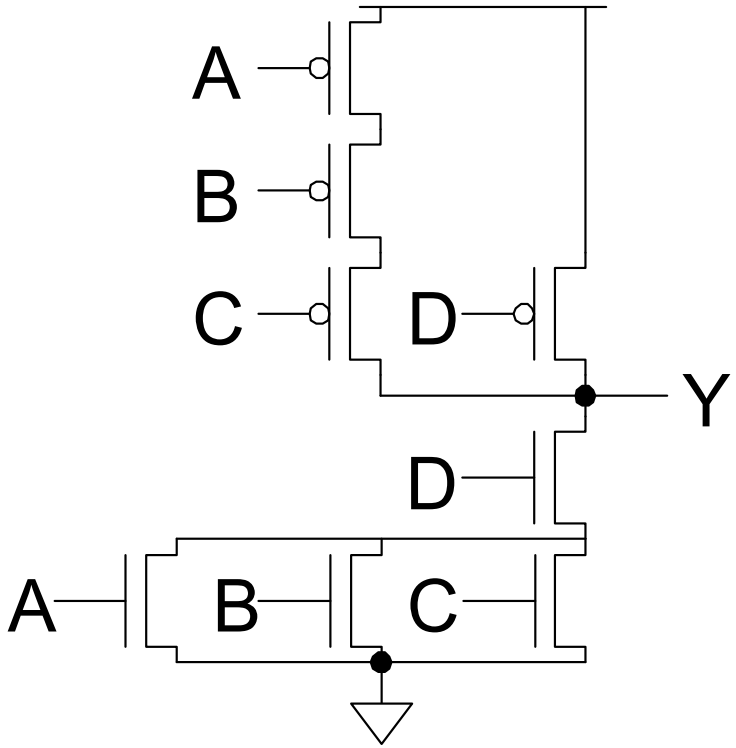


Y = Not(AB or CD)

Example: O3AI

or 3input and invert

- $Y = \overline{(A + B + C) \cdot D}$



Pass transistors and transmission gate

- An nMOS transistor is an almost perfect switch when passing a 0 and thus we say it passes a *strong* 0. However, the nMOS transistor is imperfect at passing a 1. We say it passes a *degraded* or *weak* 1
- A pMOS transistor again has the opposite behavior, passing strong 1s but degraded 0s
- When an nMOS or pMOS is used alone as an imperfect switch, we sometimes call it a *pass transistor*

Pass transistors and transmission gate

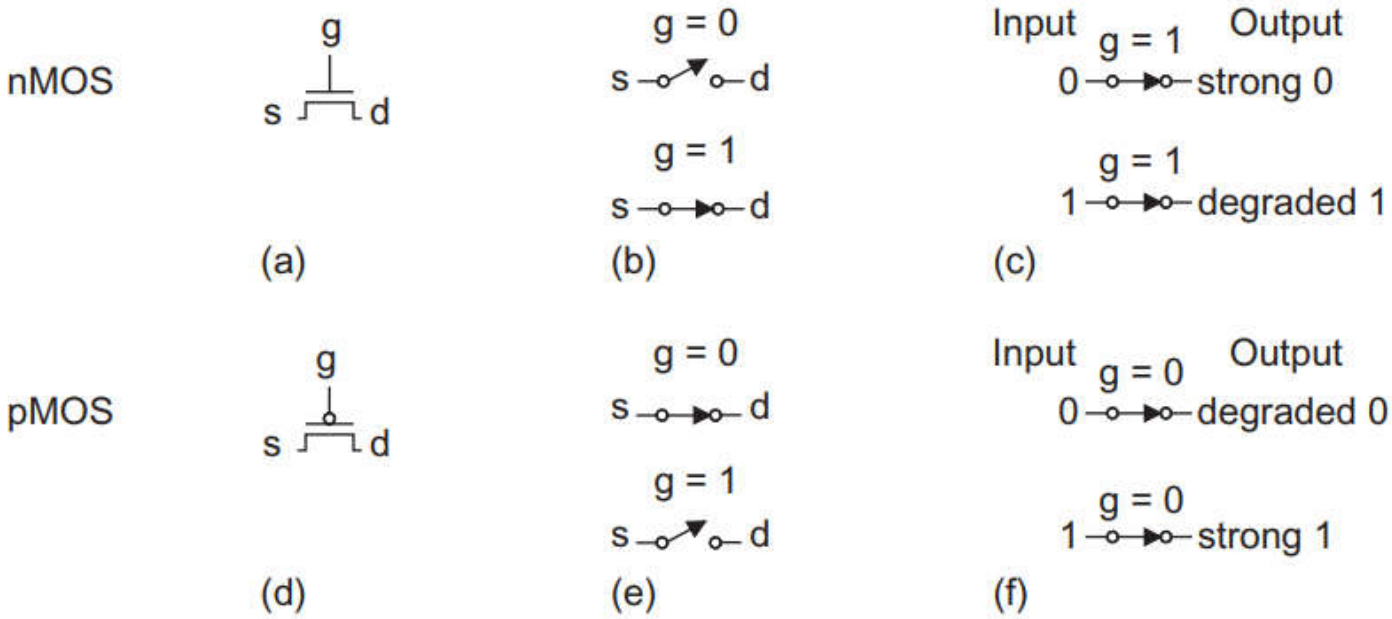


FIGURE 1.20 Pass transistor strong and degraded outputs

Pass transistors and transmission gate

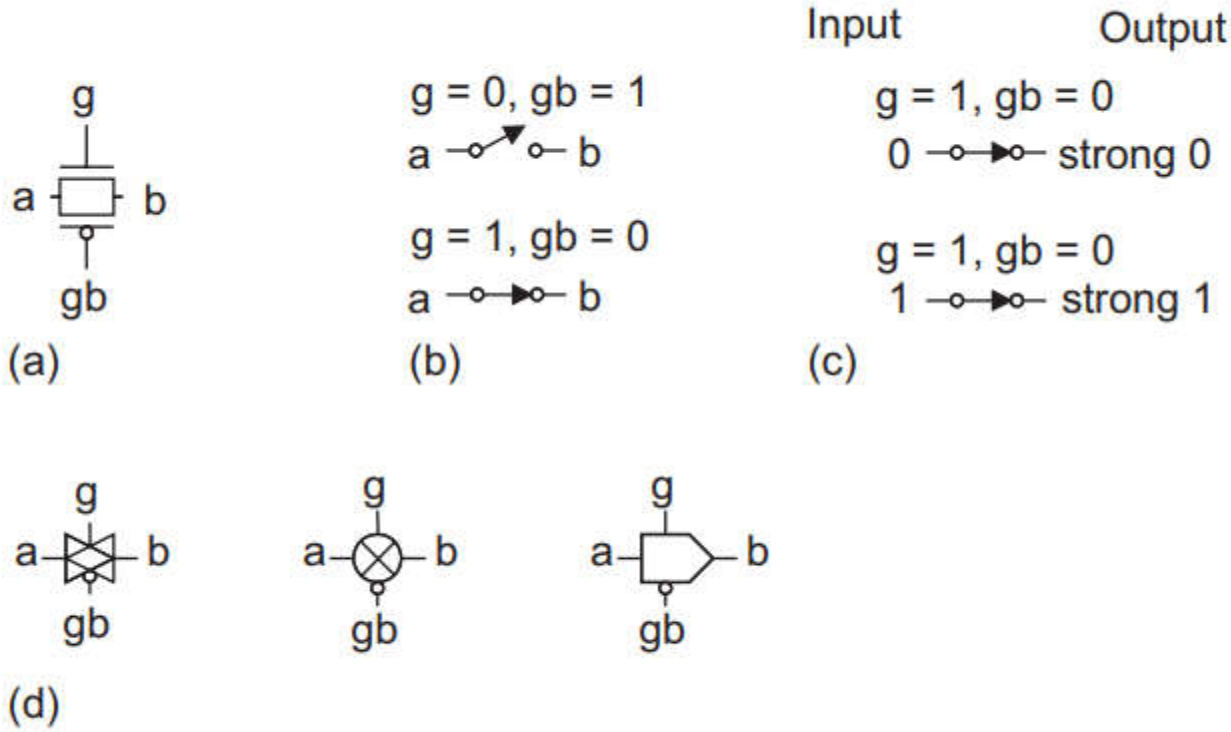


FIGURE 1.21 Transmission gate

CMOS Fabrication

đĩa bán dẫn

- CMOS transistors are fabricated on silicon wafer

Quy trình in thạch bản tương tự như in ấn

- Lithography process similar to printing press

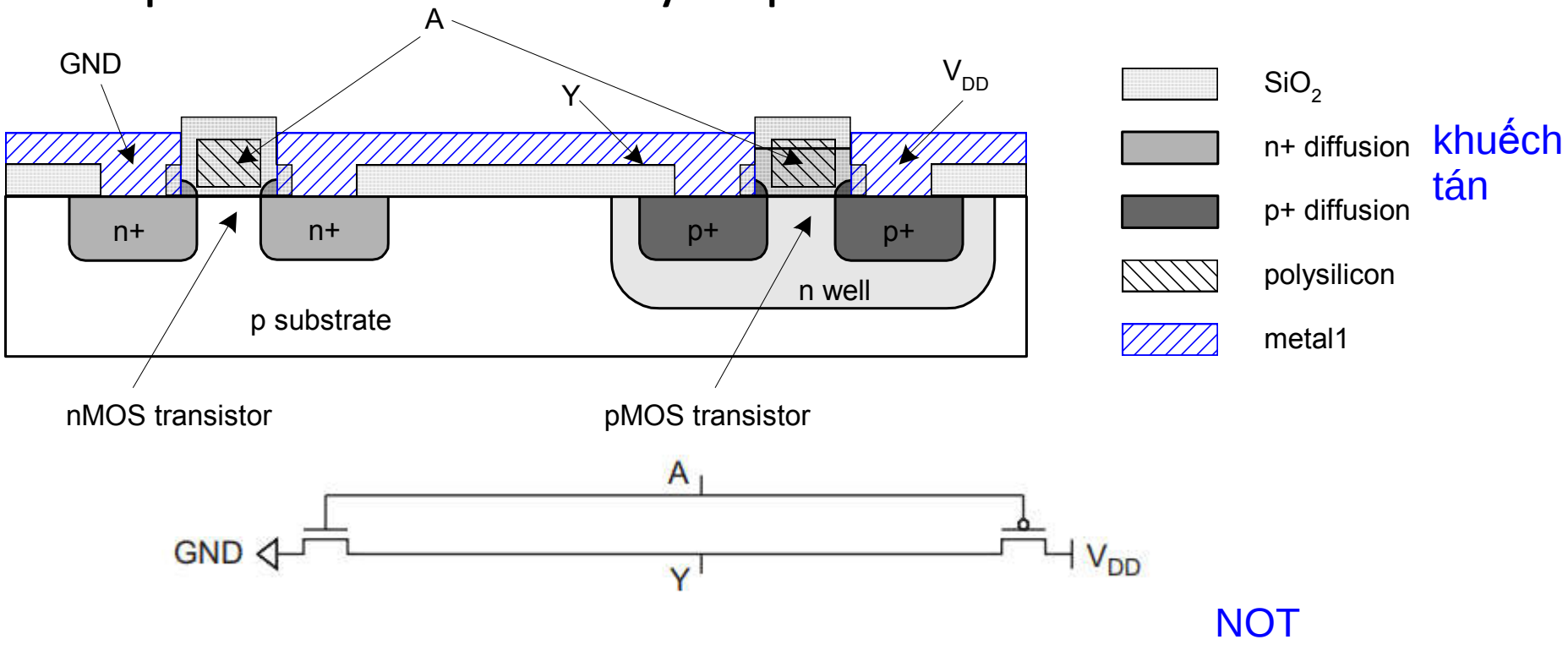
gửi

- On each step, different materials are deposited or etched khắc axit
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

Inverter Cross-section

chất nền

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



nút

Well and Substrate Taps

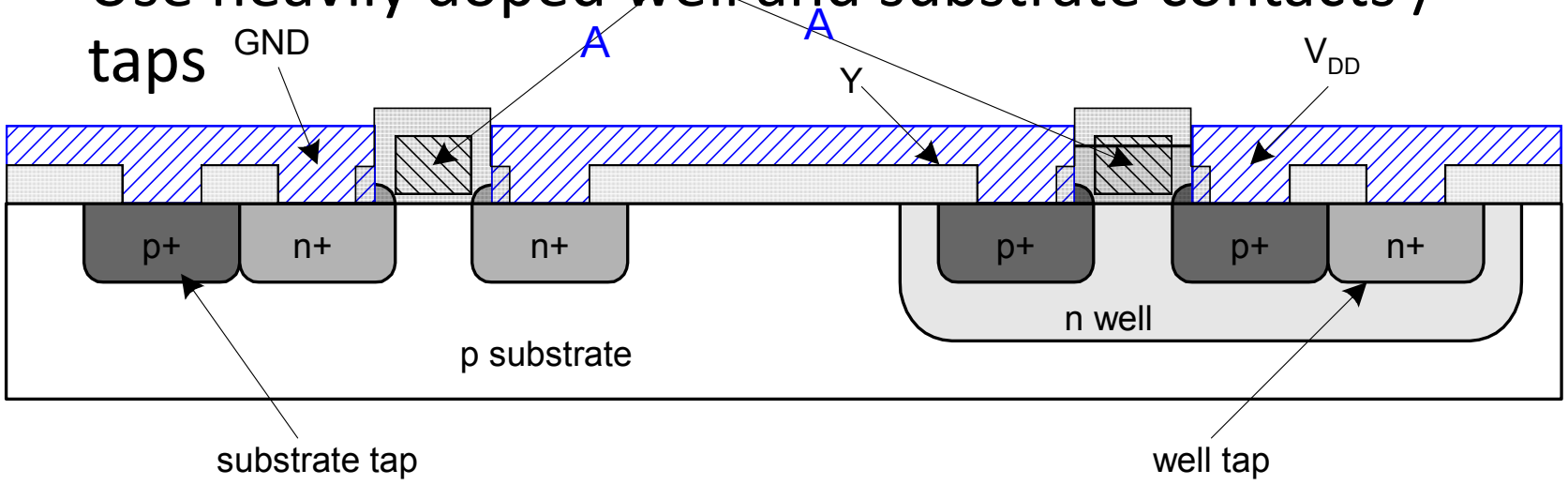
- Substrate must be tied to GND and n-well to V_{DD}

Kim loại pha tạp nhẹ

- Metal to lightly-doped semiconductor forms poor connection (used for Schottky Diode)

+

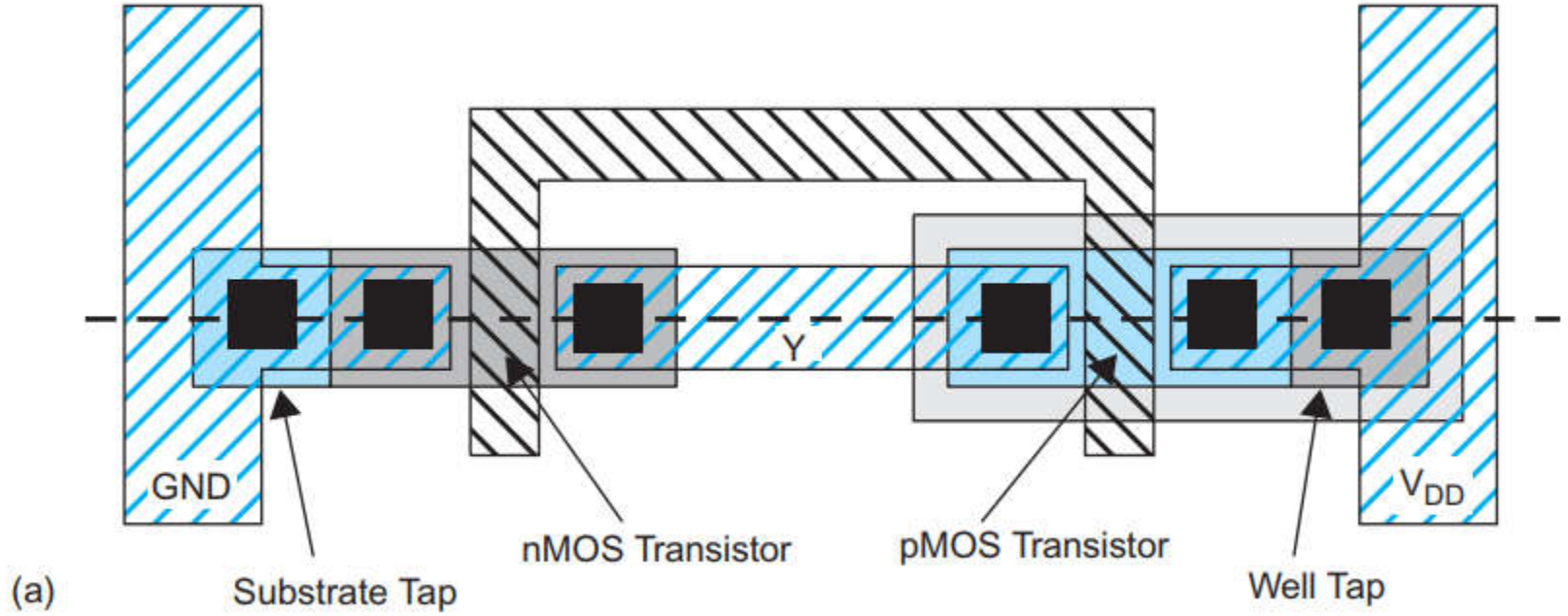
- Use heavily doped well and substrate contacts / taps

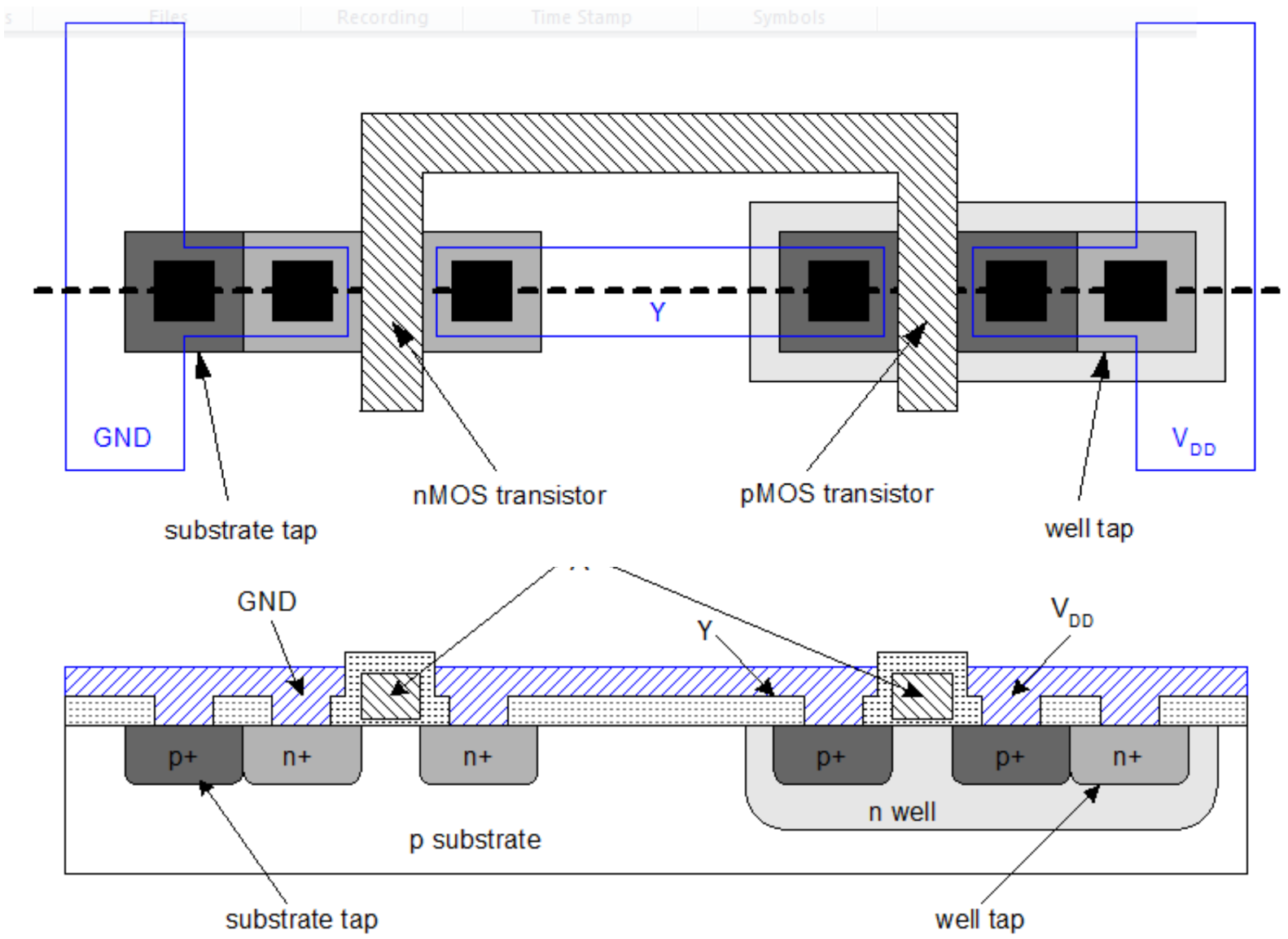


Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line

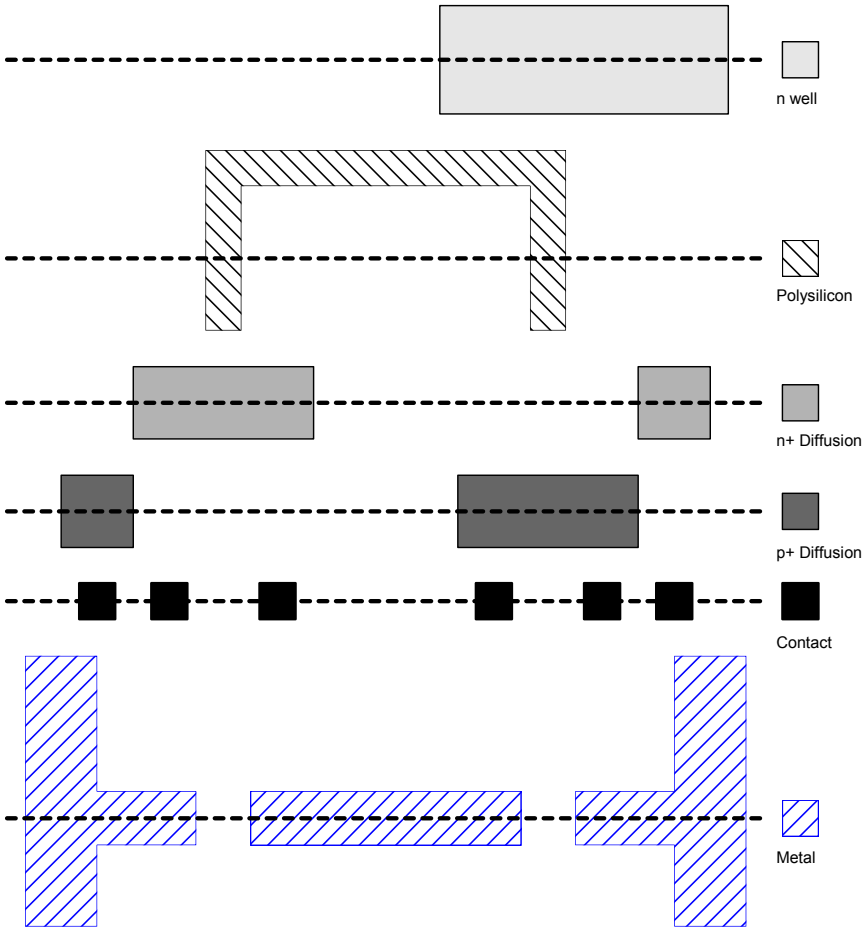
Mặt cắt ngang được thực hiện theo đường nét đứt




GND
Y
V_{DD}
substrate tap
nMOS transistor
pMOS transistor
well tap
GND
Y
V_{DD}
p+
n+
n+
p+
p+
n+
n well
p substrate
substrate tap
well tap

Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal



https://www.youtube.com/watch?v=1Lad28K3Xi0

Fabrication Steps

Wafer là một miếng silicon mỏng chừng 30 mil (0.76 mm) được cắt ra từ thanh silicon hình trụ

trống

- Start with blank wafer

từ dưới lên

- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built

cấy ghép

  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2

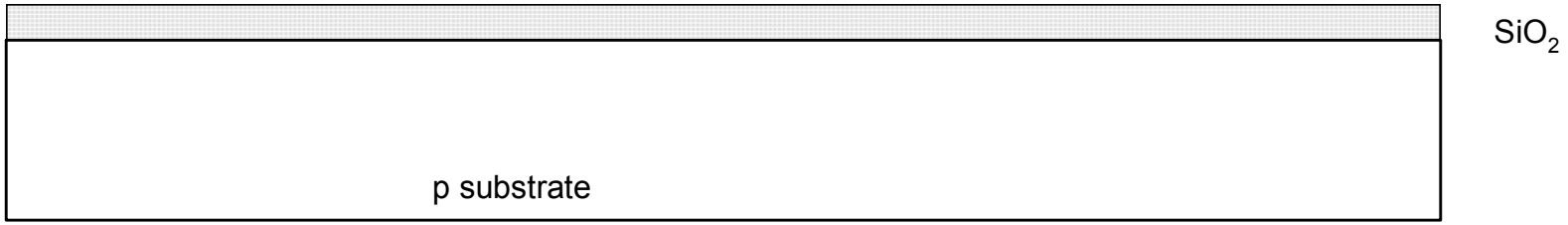
tháo rời

quá trình oxi hóa

Oxidation

- Grow SiO_2 on top of Si wafer
  - The wafer is first *oxidized* in a high-temperature (typically 900–1200 °C) furnace that causes Si and O2 to react and become SiO2 on the wafer surface

lò lửa



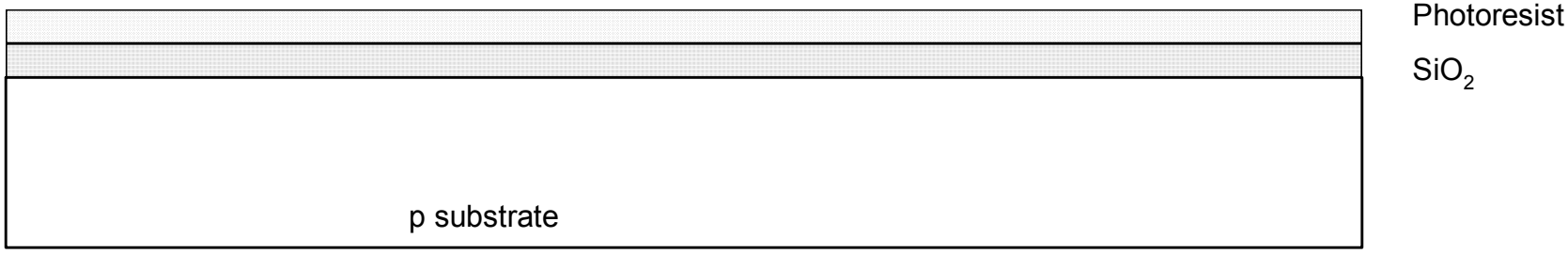
chất cản quang

Photoresist

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light

photoresist là một polyme hữu cơ nhạy cảm với ánh sáng và nó mềm đi khi tiếp xúc với ánh sáng

đổ chất cản quang lên



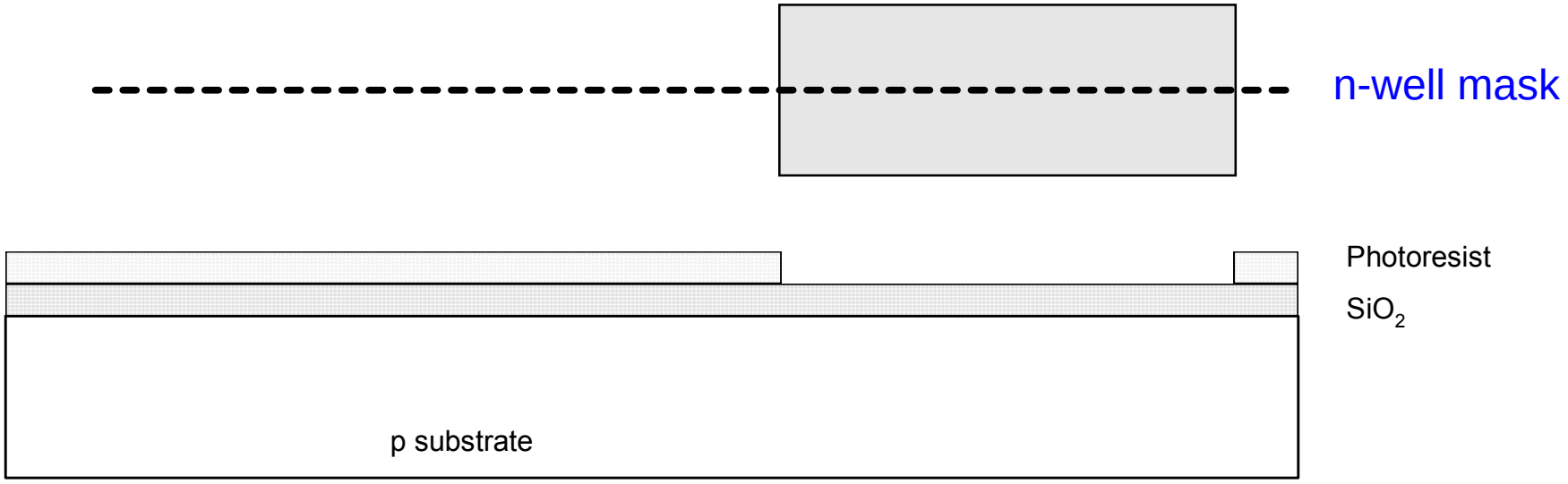
in thạch bản

Lithography

Phơi sáng chất cản quang qua mặt nạ n-well

- Expose photoresist through n-well mask
- Strip off exposed photoresist

loại bỏ 1 phần của lớp cản quang

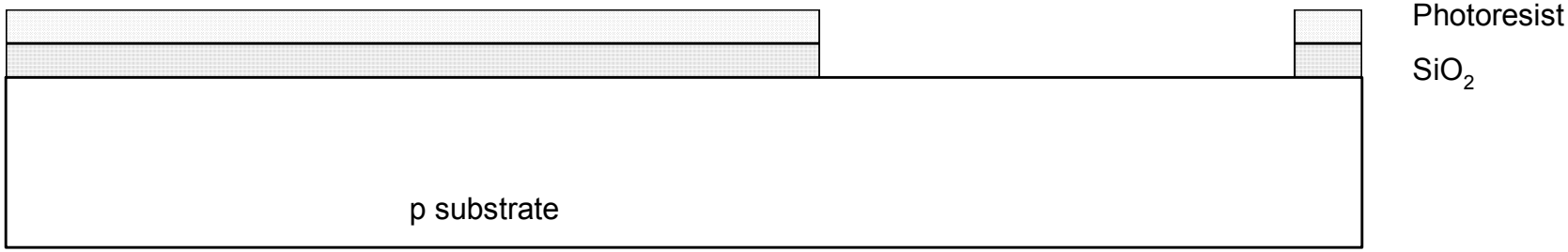


Etch

ăn mòn

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed

lộ ra

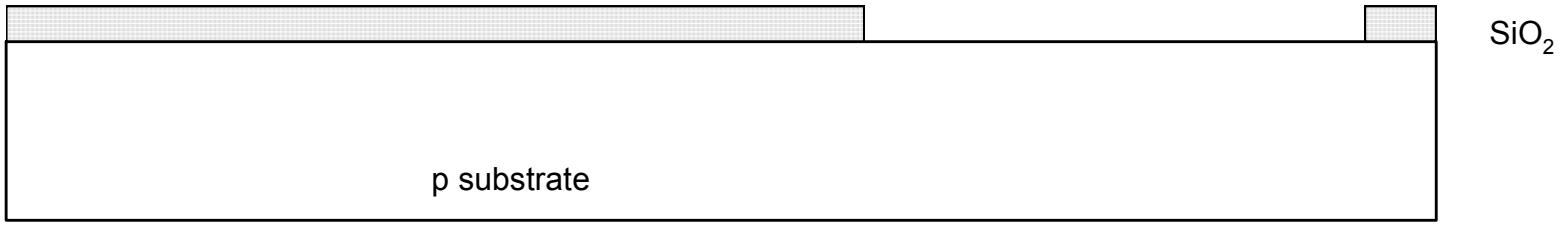


bám cái tia ánh sáng xuống để phá hủy lớp dưới

Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranha etch
- Necessary so resist doesn't melt in next step

bỏ cái lớp ko cần thiết



n-well

khuếch tán cấy

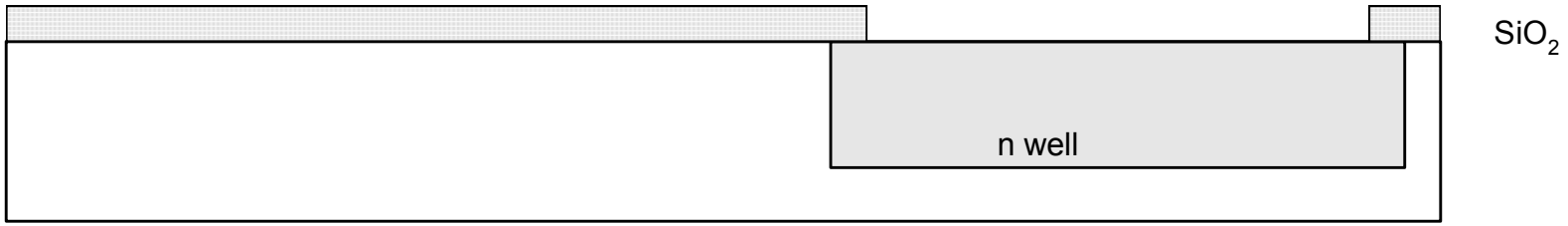
- n-well is formed with diffusion or ion implantation
- Diffusion

cho thêm tạp chất tạo thành bán dẫn loại n

  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si

nguyên tử

- Ion Implanatation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si



well: giếng

Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps

bỏ SiO2

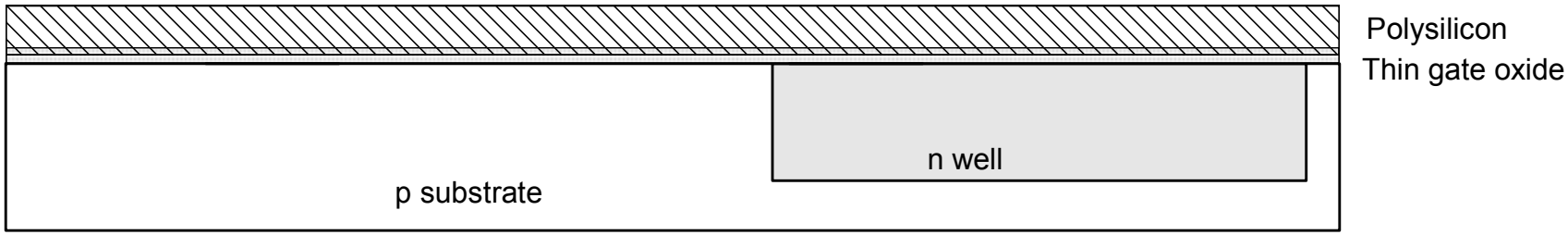
Polysilicon

đổ 1 lớp SiO2 mỏng

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)

lắng đọng hơi hóa chất

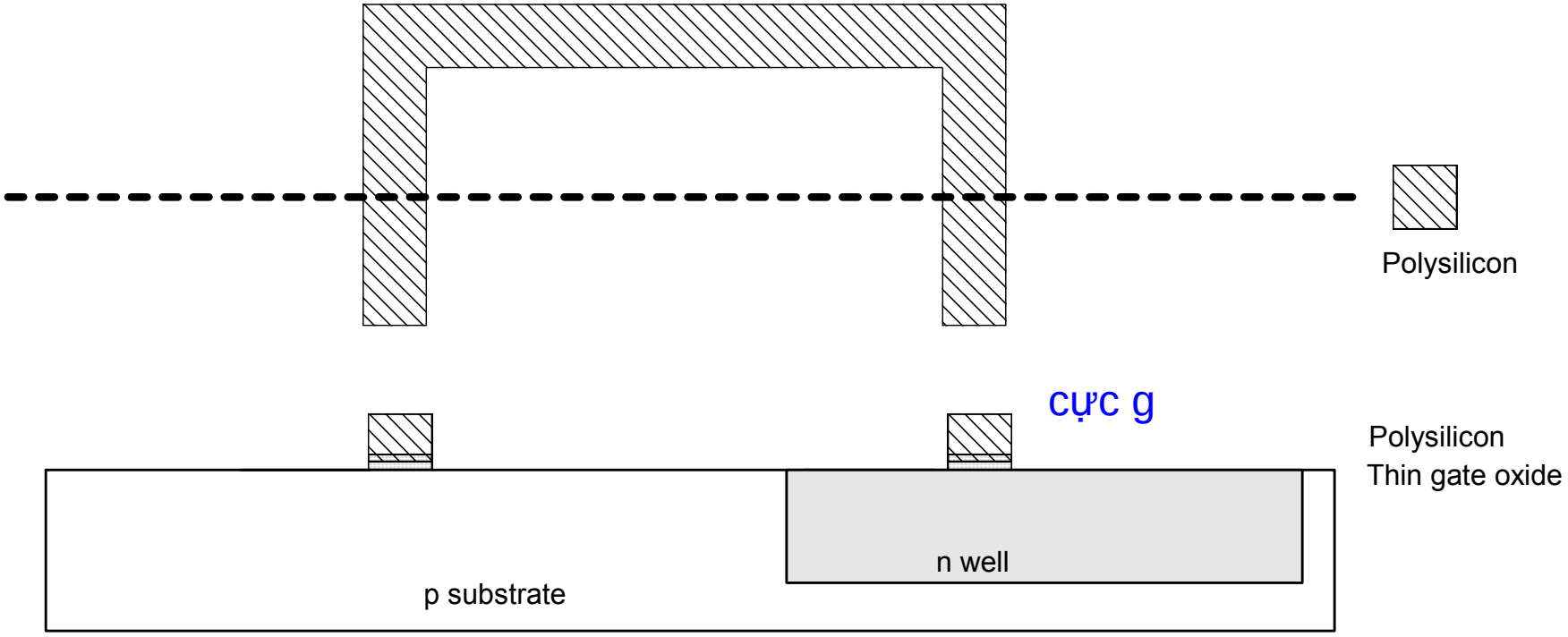
- Chemical Vapor Deposition (CVD) of silicon layer to form polysilicon
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon pha lê
  - Heavily doped to be good conductor



Polysilicon Patterning

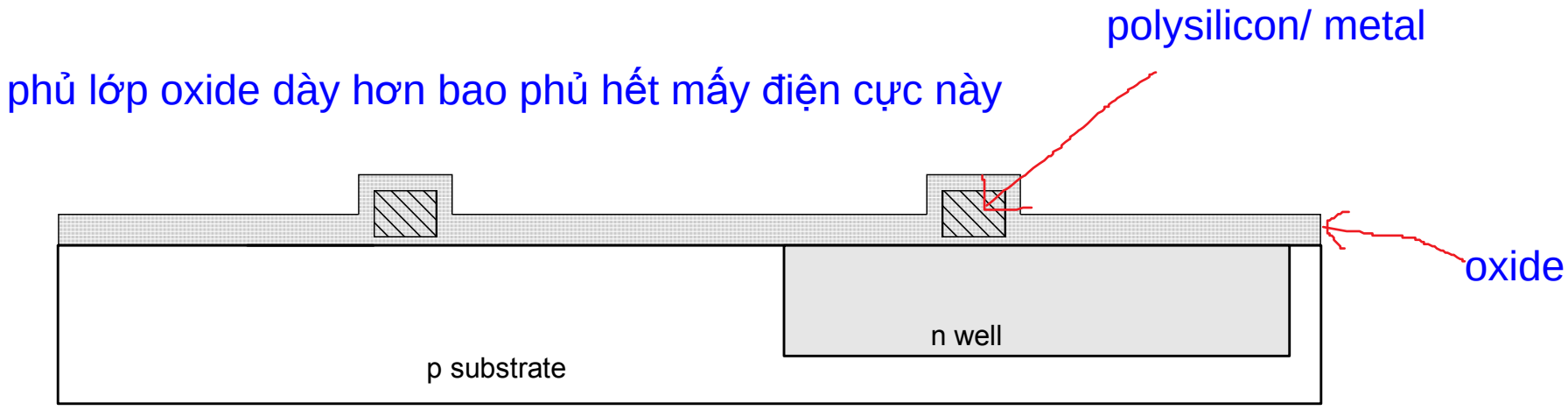
bỏ lớp polysilicon vs oxide những chỗ k cần thiết

- Use same lithography process to pattern polysilicon



N-diffusion

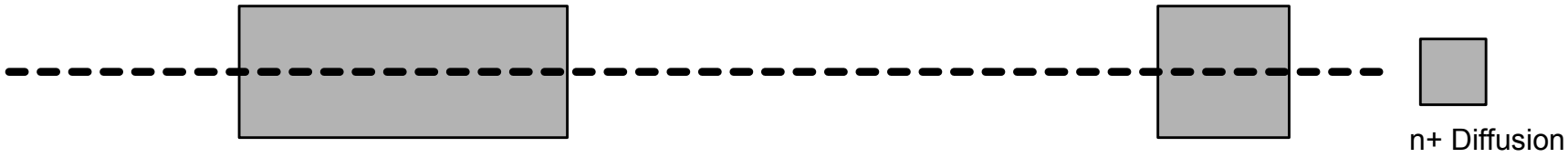
- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact

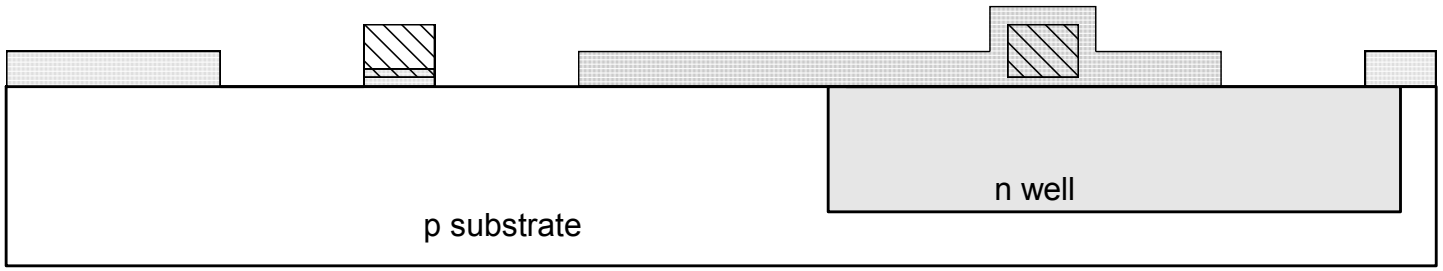


N-diffusion (cont.)

- Pattern oxide and form n+ regions

bỏ bớt những phần muốn gia công



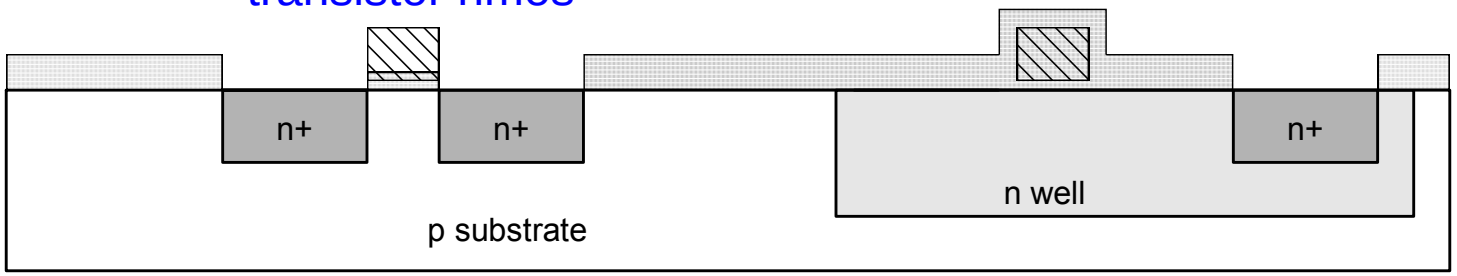


N-diffusion (cont.)

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion

cho thêm tạp chất vào để tạo thành bán dẫn loại n

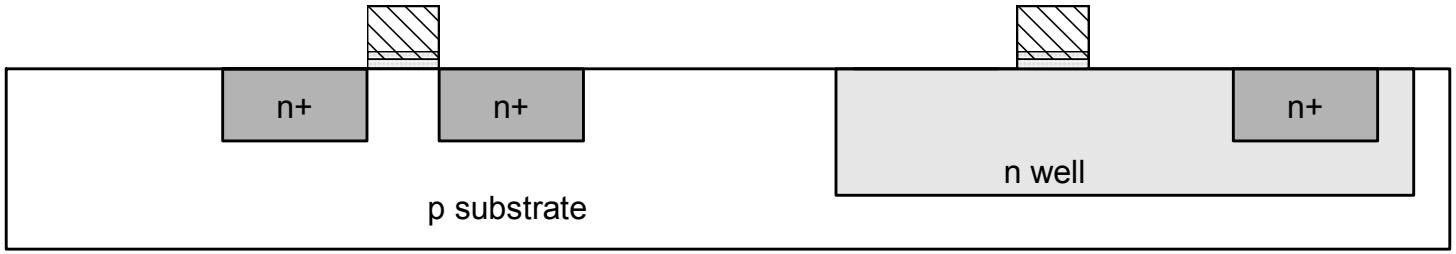
transistor nmos



N-diffusion (cont.)

làm theo khuôn

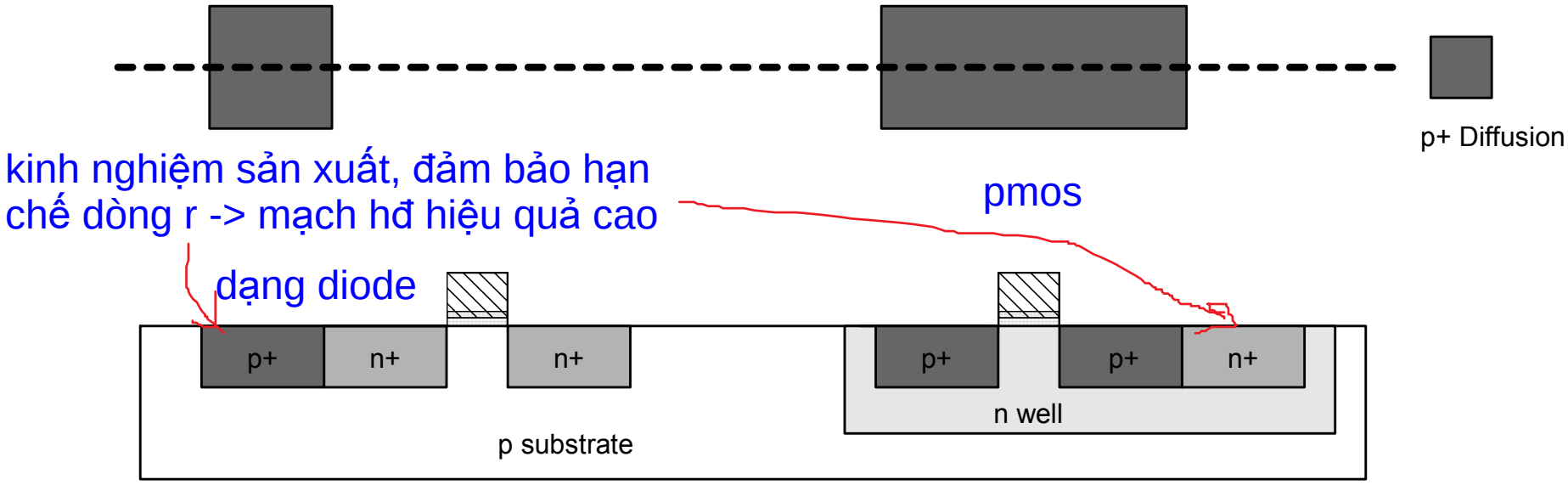
- Strip off oxide to complete patterning step



P-Diffusion

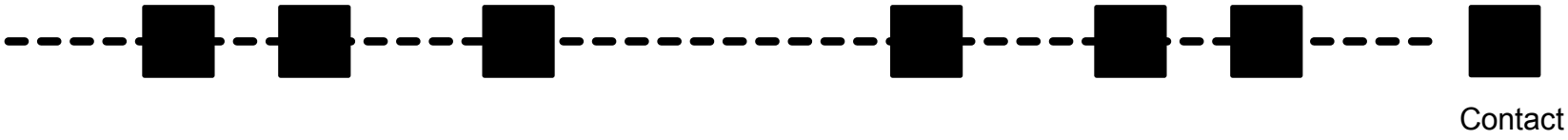
- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact

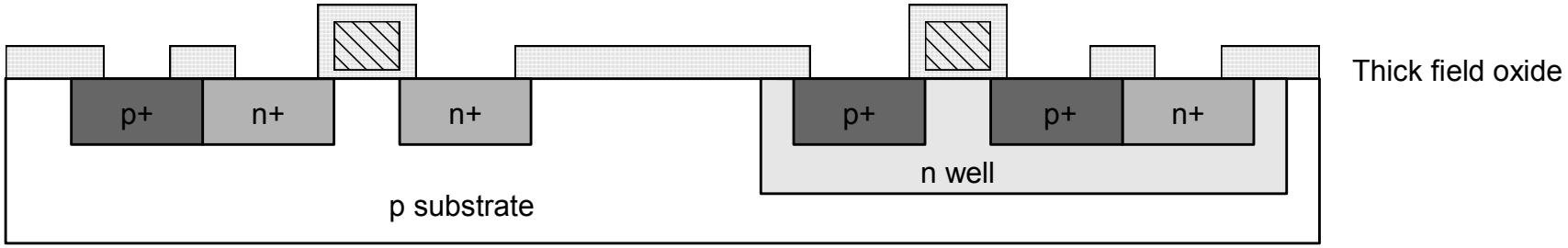
điểm tiếp xúc chất nền



Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed





Metalization

gia công xong inverter

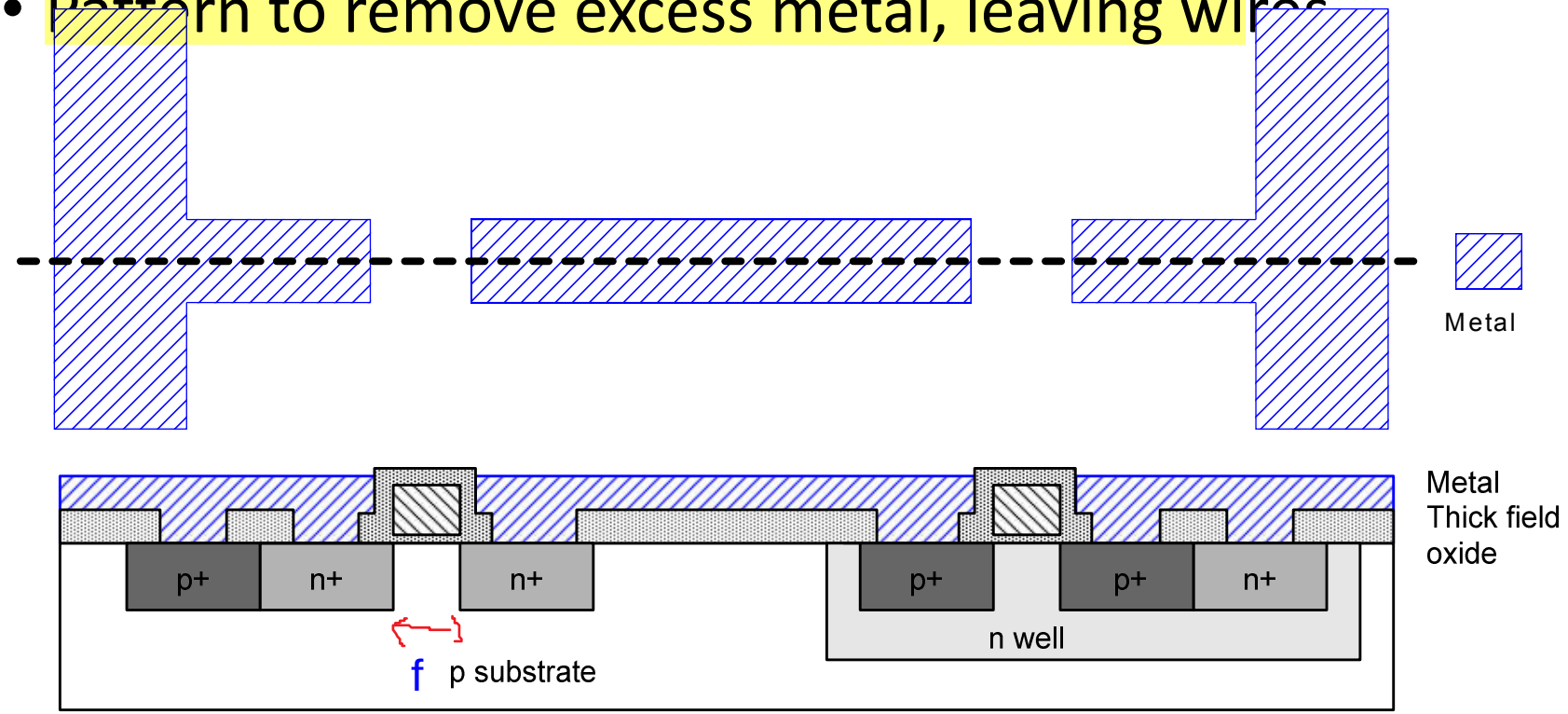
phun lên

nhôm

- Sputter on copper / aluminum over whole wafer

dư

- Pattern to remove excess metal, leaving wires



f càng thấp -> công nghệ càng cao càng khó khăn

Layout Design Rules

- Mead and Conway [Mead80] popularized scalable design rules based on a single parameter, λ, that characterizes the resolution of the process. λ is generally half of the minimum drawn transistor channel length. This length is the distance between the source and drain of a transistor and is set by the minimum width of a polysilicon wire. For example, a 180 nm process has a minimum polysilicon width (and hence transistor length) of 0.18 um and uses design rules with

đặc trưng

độ phân giải

Layout

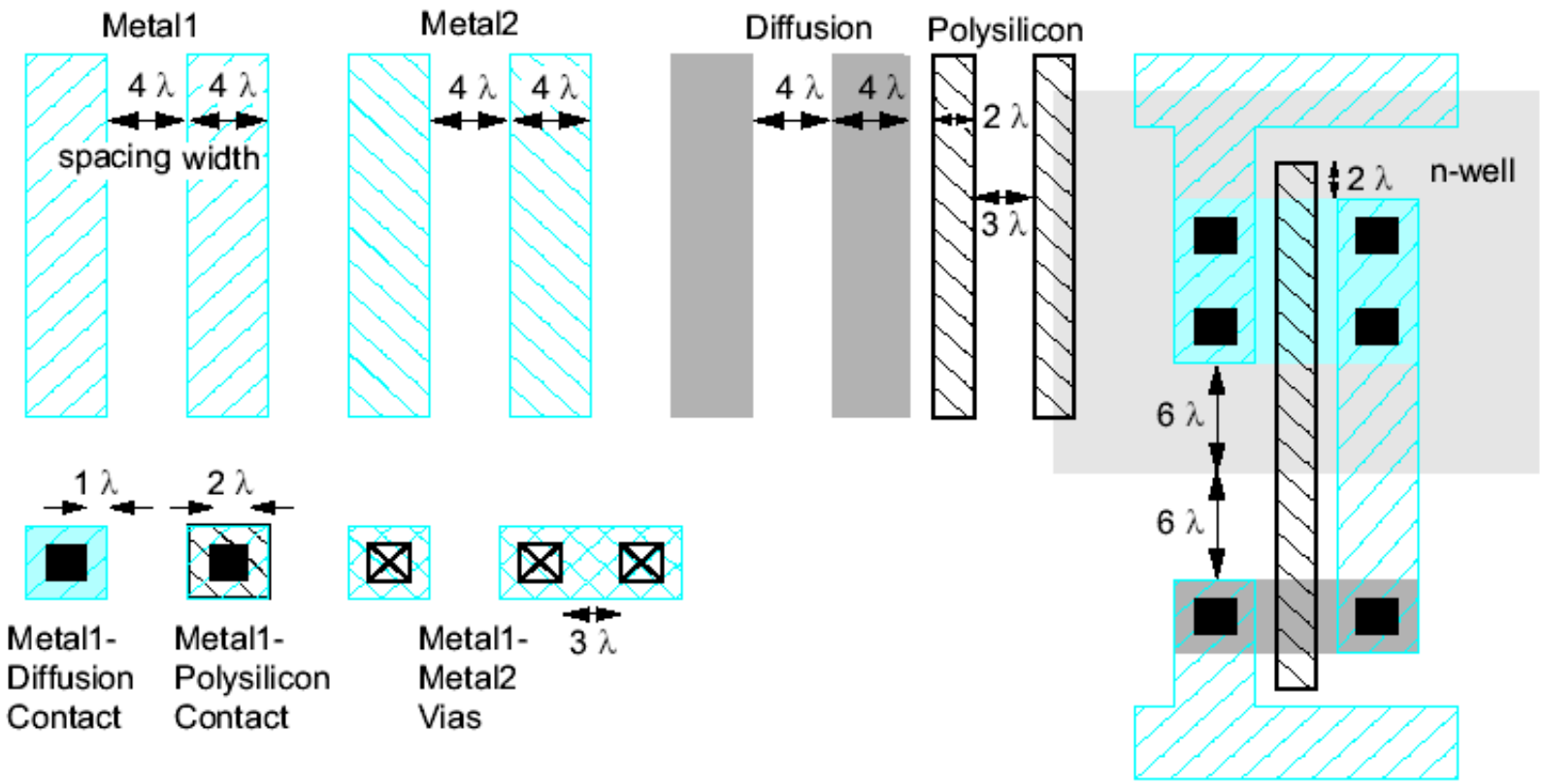
- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size f = distance between source and drain (or process)
  - Set by minimum width of polysilicon
- Feature size scales ~X0.7 every 2 years both lateral and vertical (cạnh)
  - Moore's law
- Normalize feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - E.g. λ = 0.3 μm in 0.6 μm process
- Today's λ = 0.01 μm (10 nanometer = 10^{-8} meter)

Simplified Design Rules

bảo toàn

- A conservative but easy-to-use set of design rules for layouts with two metal layers in an n-well process is as follows:
  - ❖Metal and diffusion have minimum width and spacing of 4 λ.
  - ❖Contacts are 2 λ × 2 λ and must be surrounded by 1 λ on the layers above and below.
  - ❖Polysilicon uses a width of 2 λ.

Simplified Design Rules



Inverter Layout

- Transistor dimensions specified as Width / Length
  - Minimum size is 4λ / 2λ, sometimes called 1 unit
  - In f = 0.01 μm process, this is 0.04 μm wide, 0.02 μm g