Introduction to CMOS VLSI Design

Chapter 3: CMOS Processing Technology

slides from David Harris

adapted by Duncan Elliott

Textbook: CMOS VLSI Design - A Circuits and Design Perspective,
4th Edition, N. H. E. Weste & D. Harris

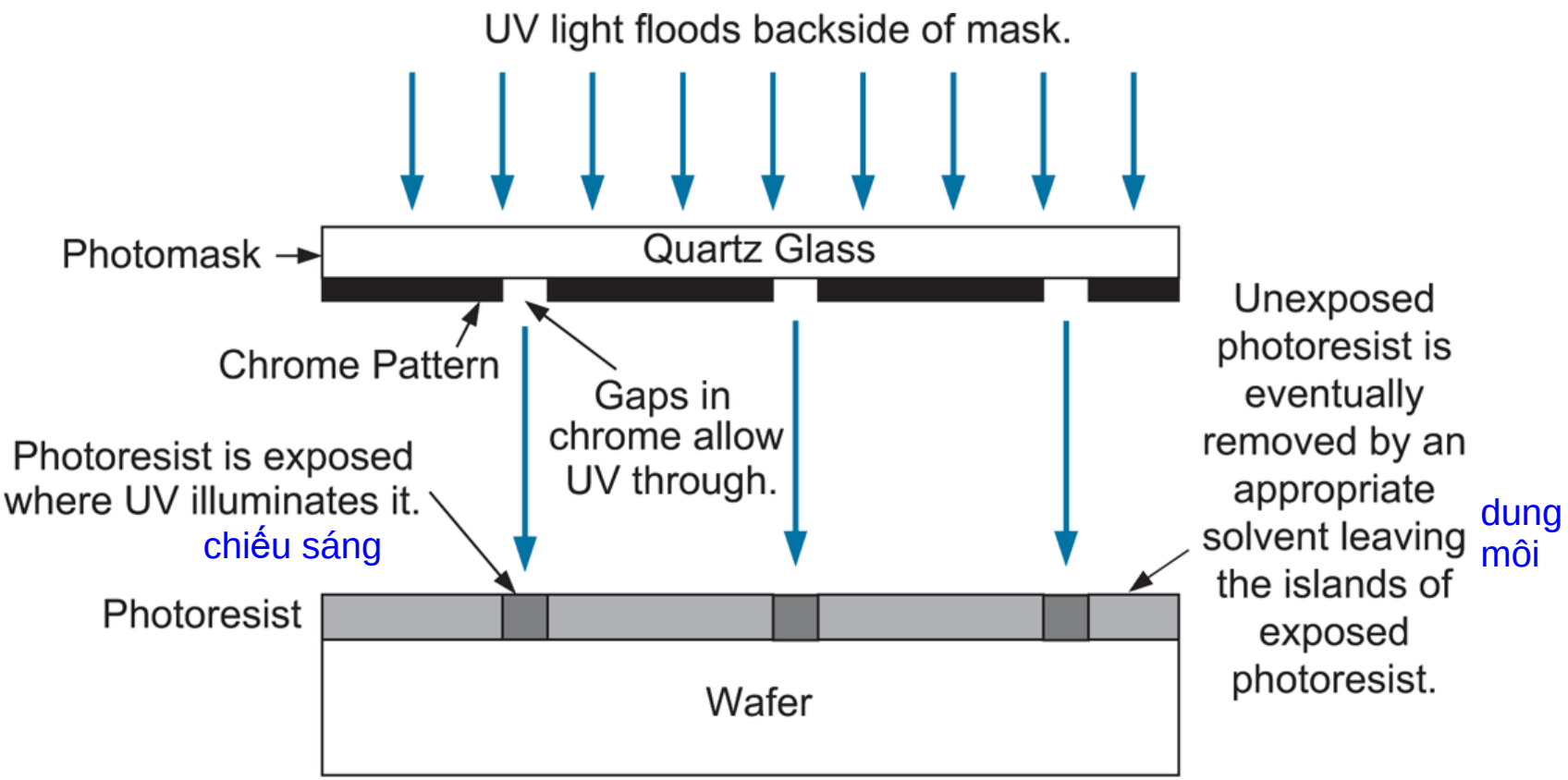
- https://www.youtube.com/watch?v=1Lad28K3Xi0
- https://www.youtube.com/watch?v=AcDn4bvW5IU
- https://www.youtube.com/watch?v=M-wNC3Z3ZX4
- https://www.youtube.com/watch?v=fwNkg1fsqBY

CMOS Fabrication Process (Animation)

SK hynix Wafer Fabrication

Making Memory Chips – Process Steps

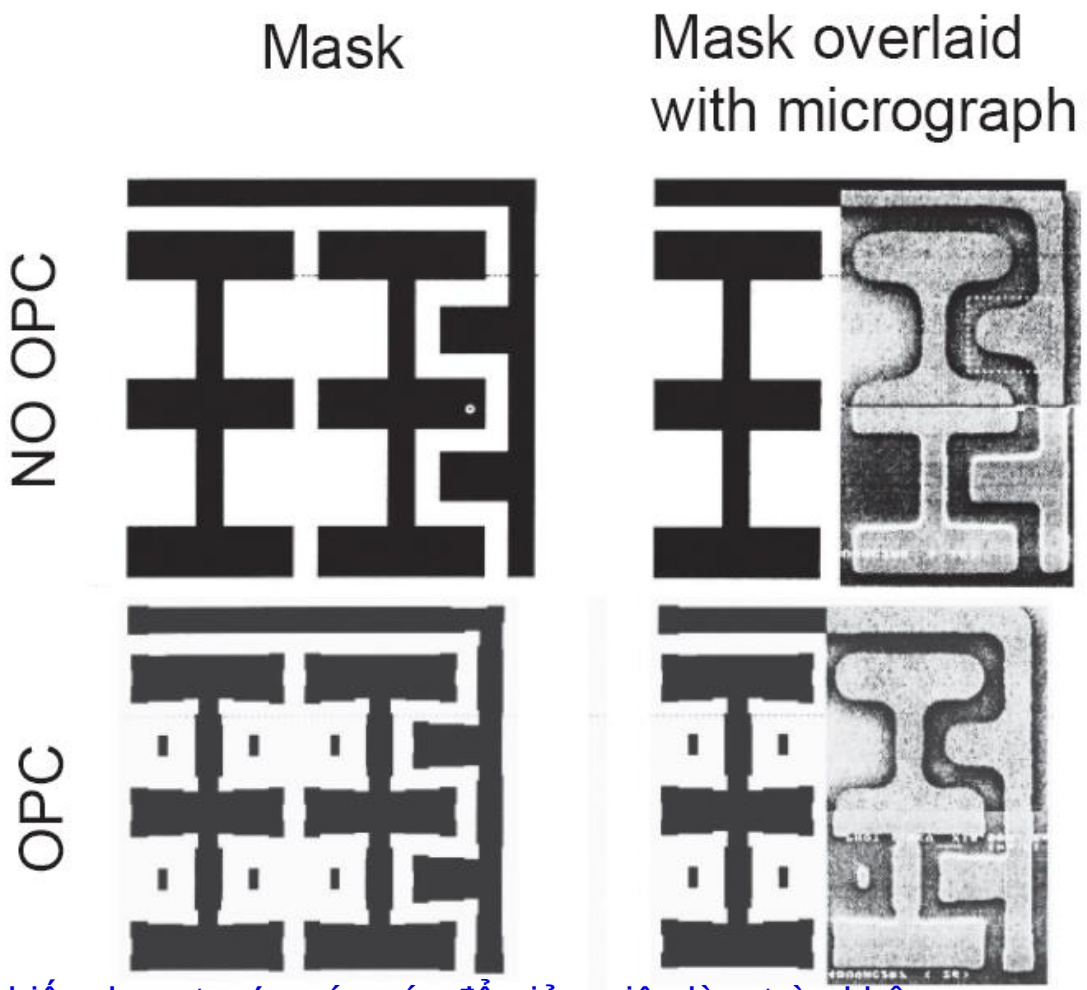
VLSI Fabrication Process



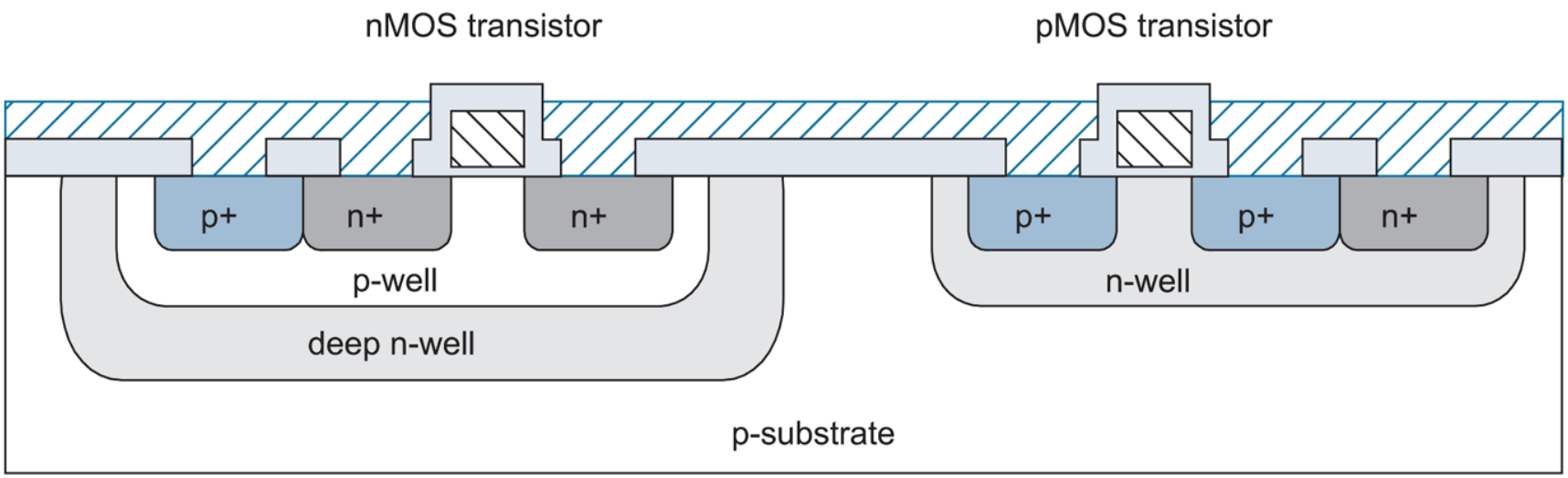
Photomasking with a negative resist (lens system between mask and wafer omitted to improve clarity and avoid diffracting the reader ☺)

Photomasking với điện trở âm (bỏ qua hệ thống thấu kính giữa mặt nạ và tấm wafer để cải thiện độ rõ nét và tránh làm nhiễu xạ người đọc

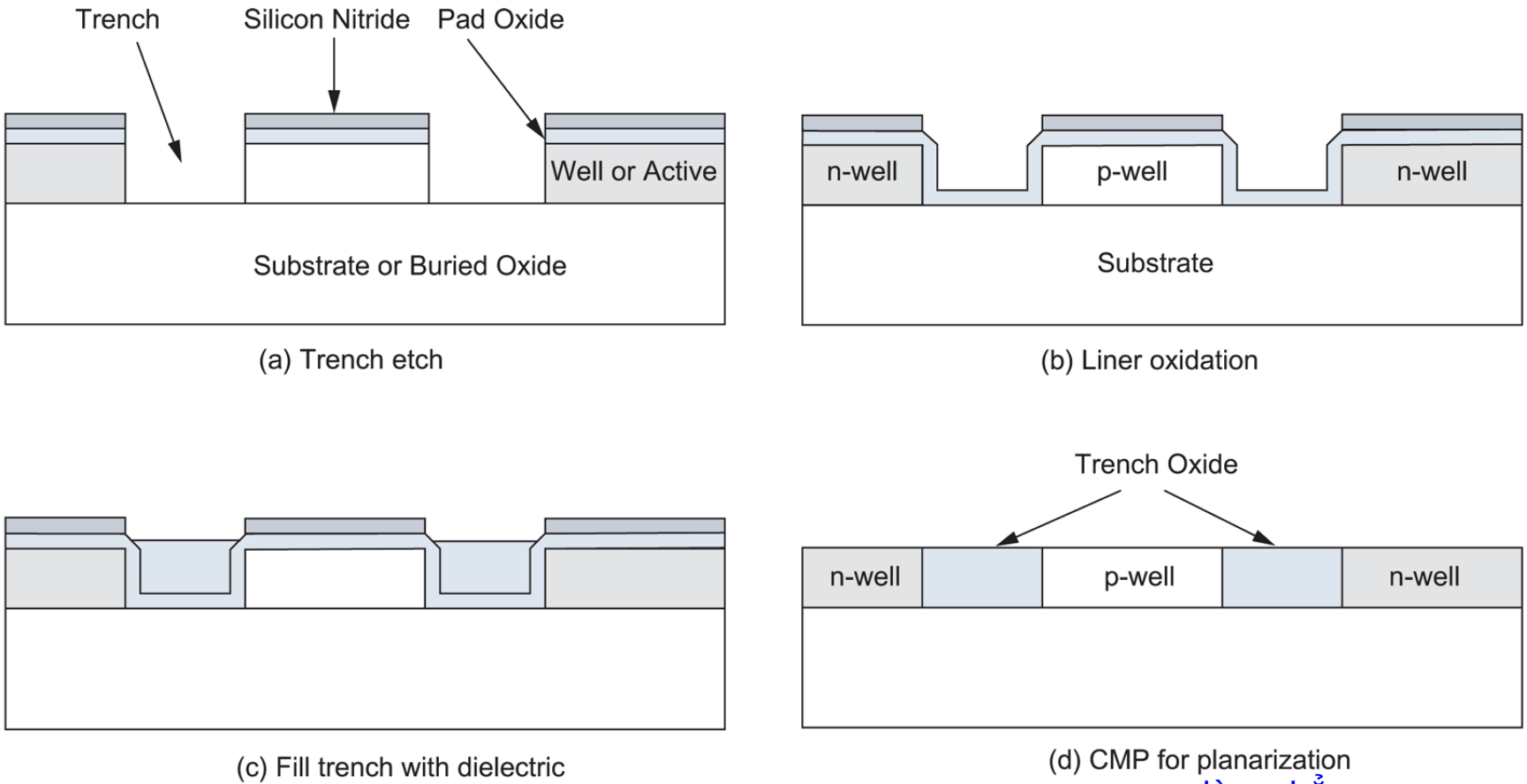
Optical Proximity Correction (OPC) Masks



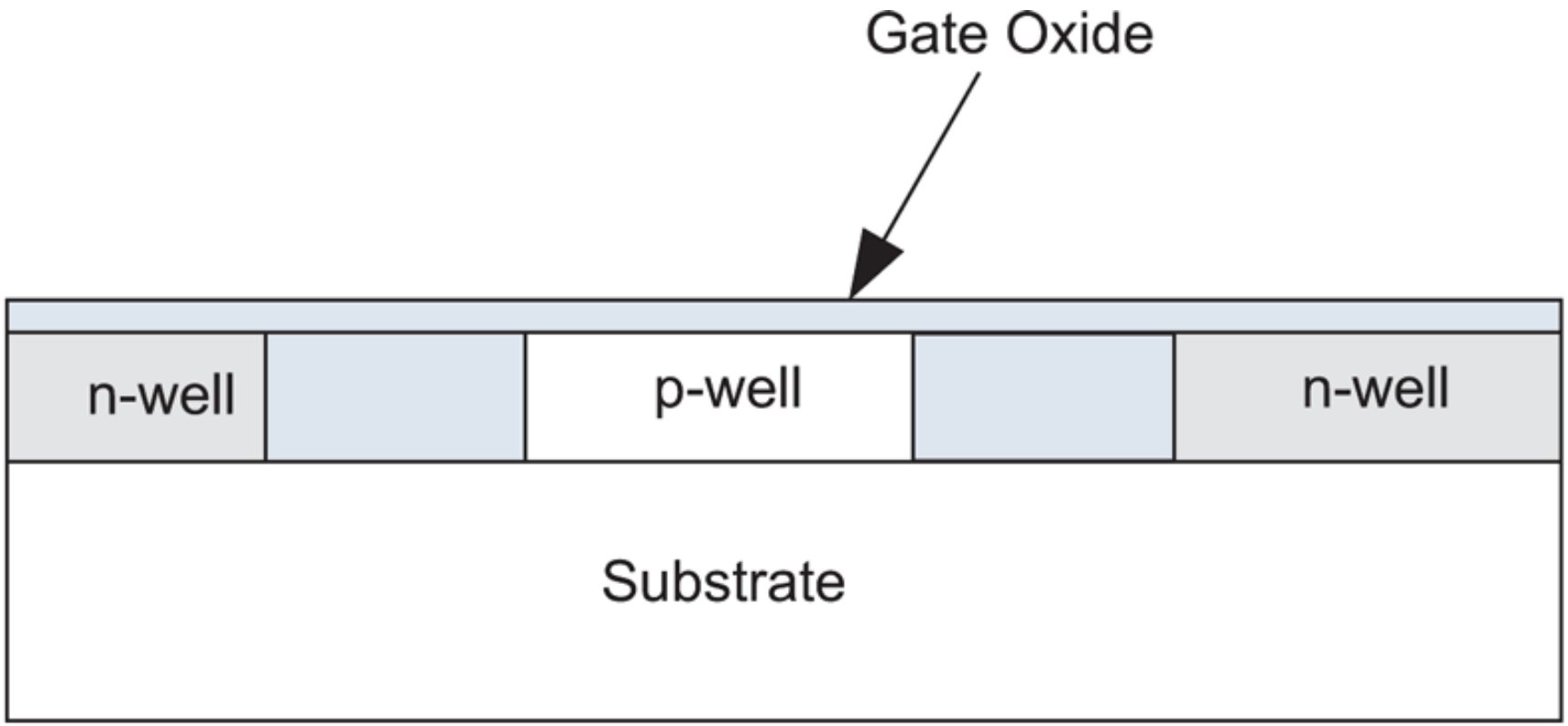
làm biến dạng trước các góc để giảm việc làm tròn không mong muốn



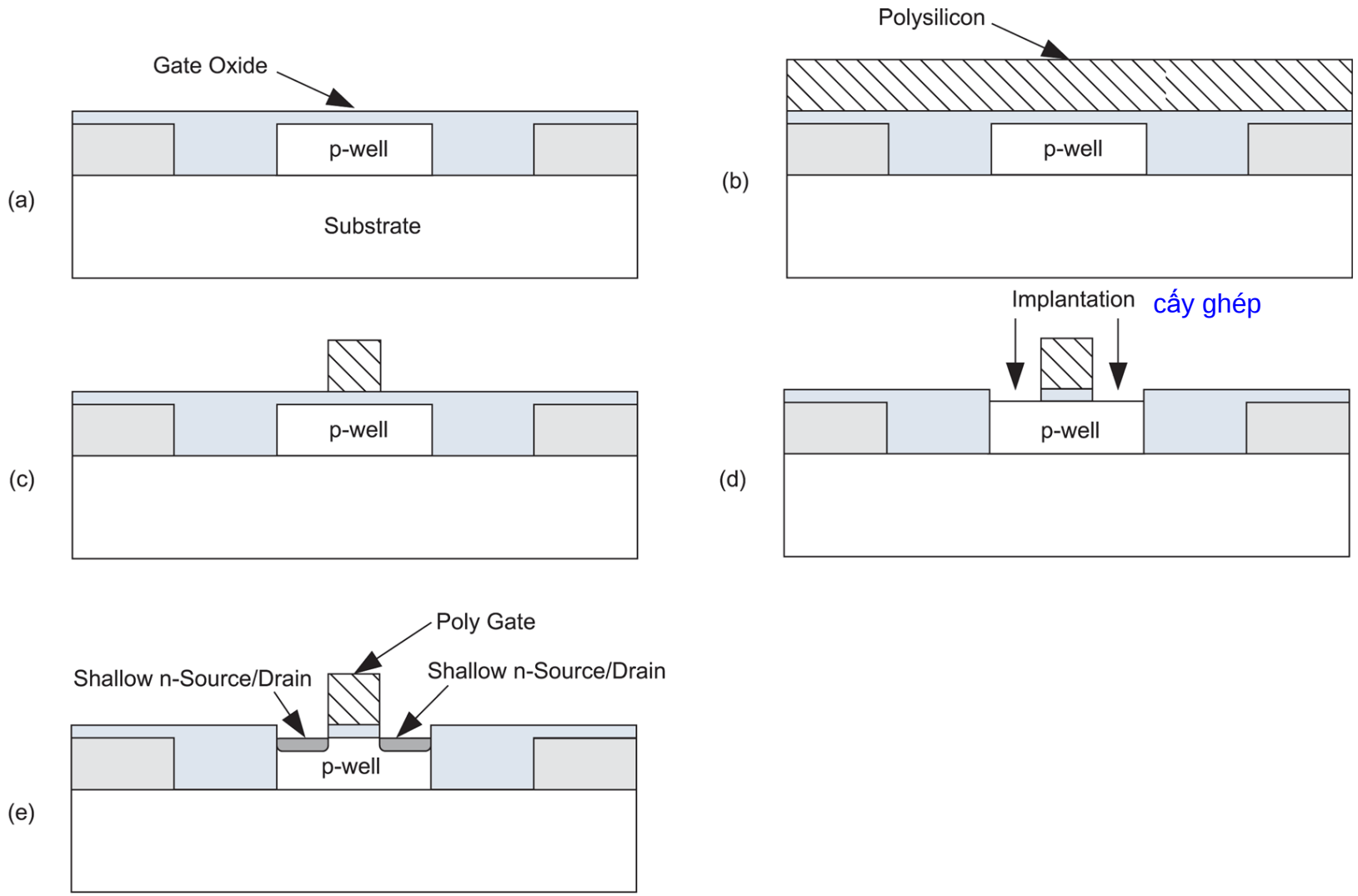
Well structure in triple-well process



Shallow trench isolation



Gate oxide formation



Gate and shallow source/drain definition

Hot Carriers

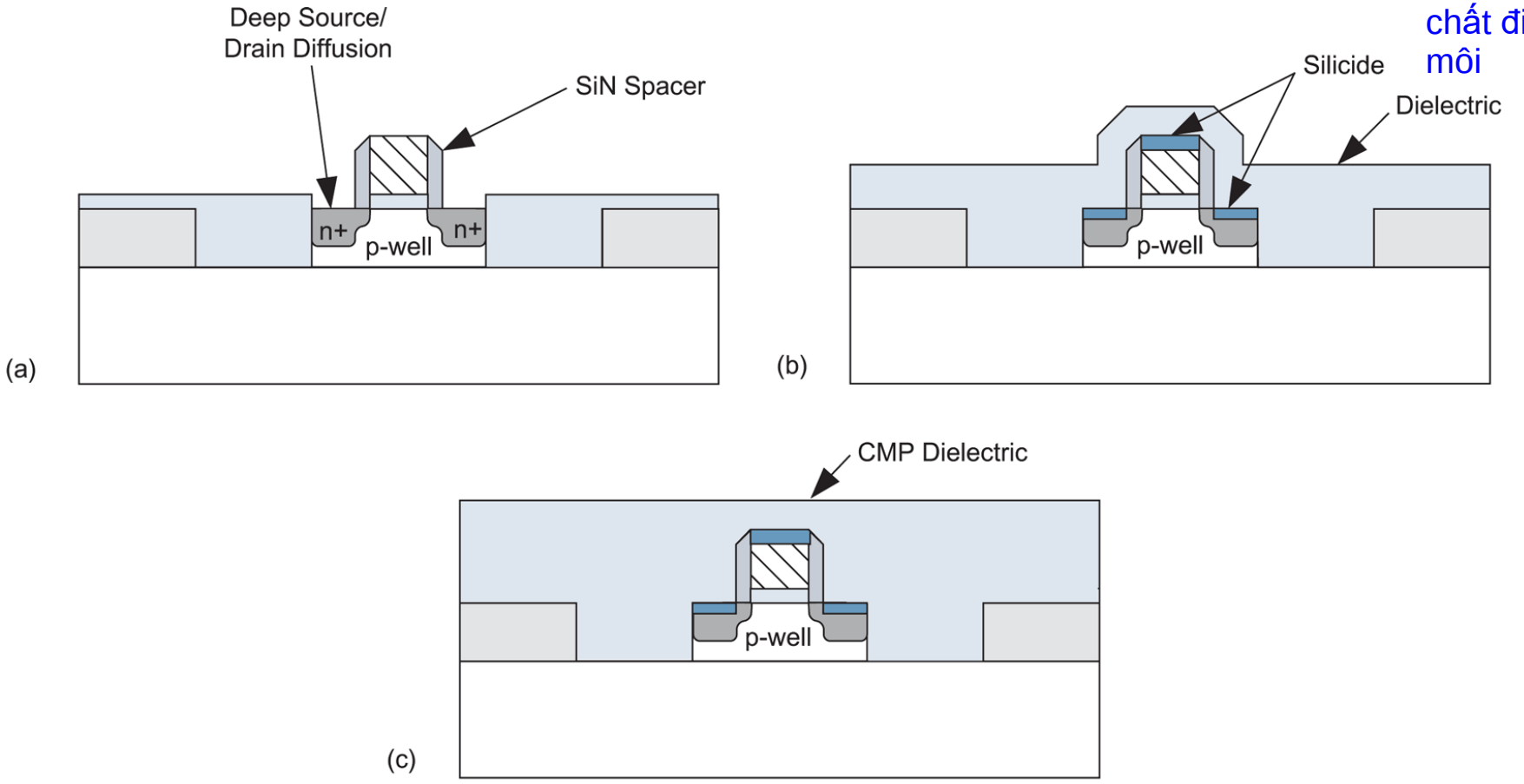
Điện trường qua kênh truyền năng lượng cao cho một số hạt tải

- Electric fields across channel impart high energies to some carriers
  - These “hot” carriers may be blasted into the gate oxide where they become trapped
  - Accumulation of charge in oxide causes shift in V_t over time
  - Eventually V_t shifts too far for devices to operate correctly
- Choose V_{DD} to achieve reasonable product lifetime
  - Worst problems for inverters and NORs with slow input risetime and long propagation delays
  - Use lightly doped drains (LLD) to reduce hot carrier injection (HCI)

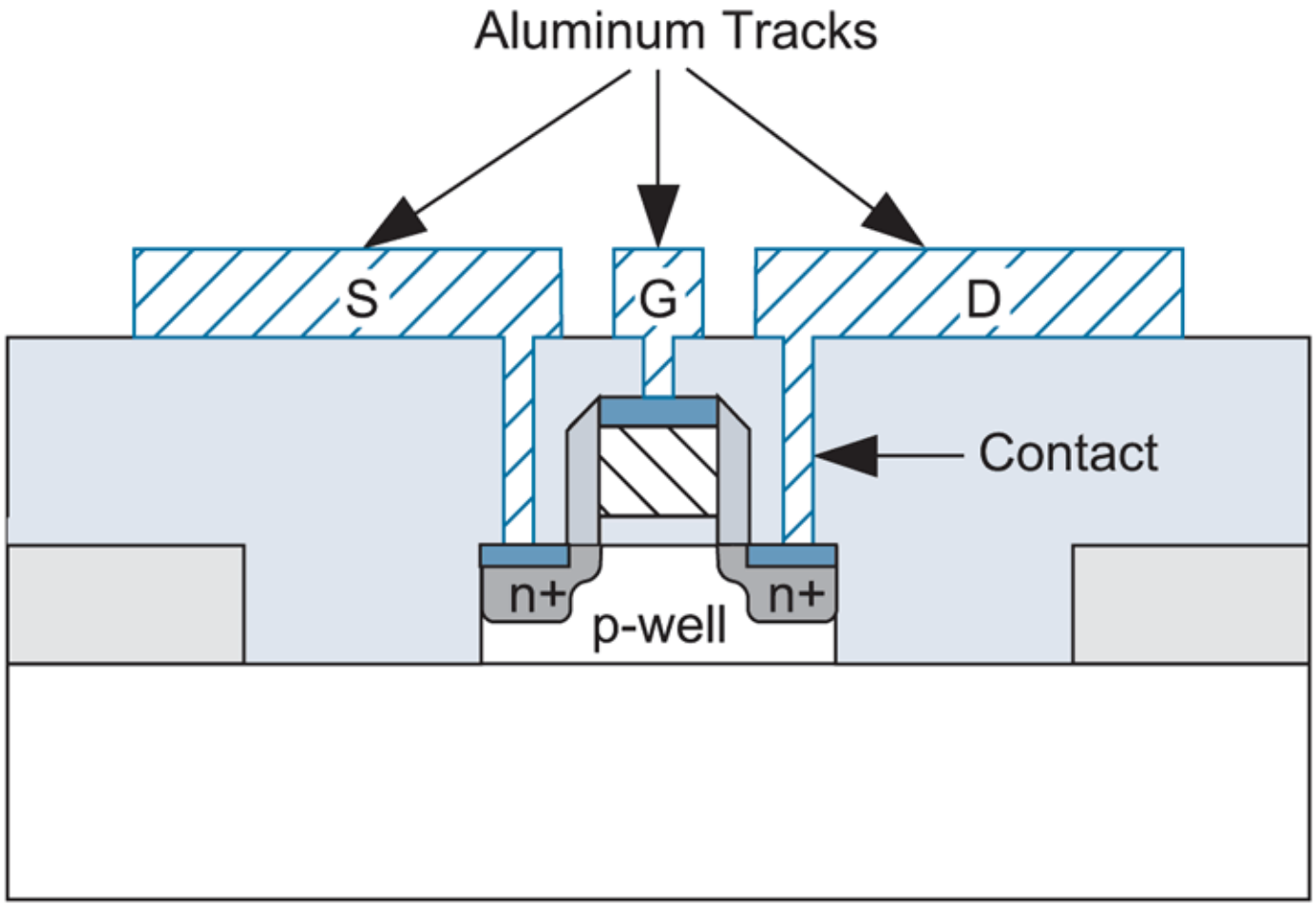
thổi bay

bị mắc kẹt

chất điện môi



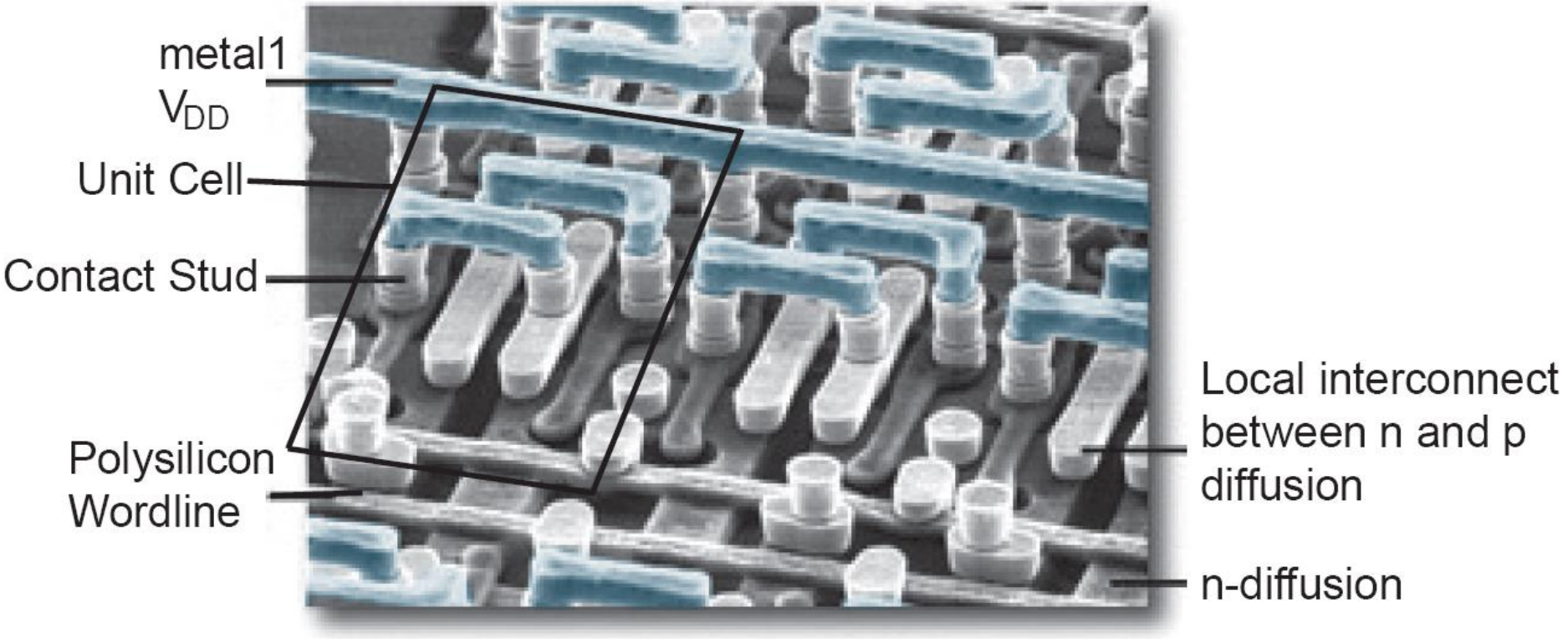
Lightly Doped Drain (LDD) structure

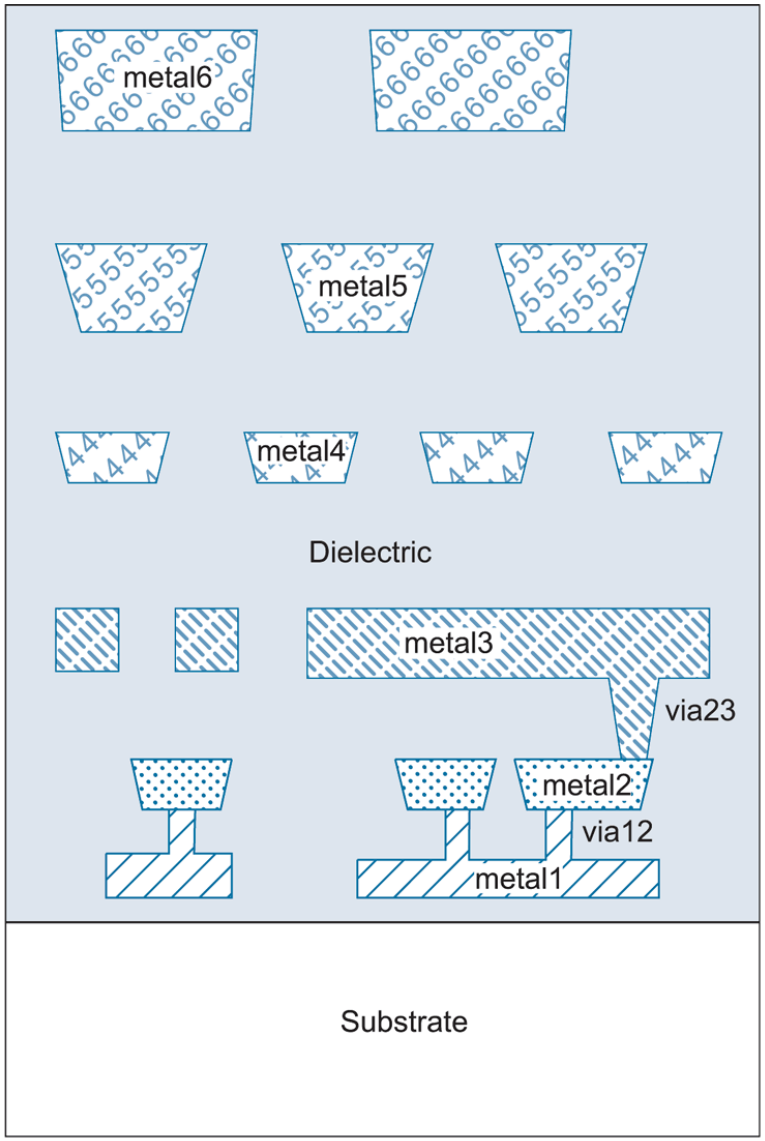


Aluminum metallization

kim loại hóa nhôm

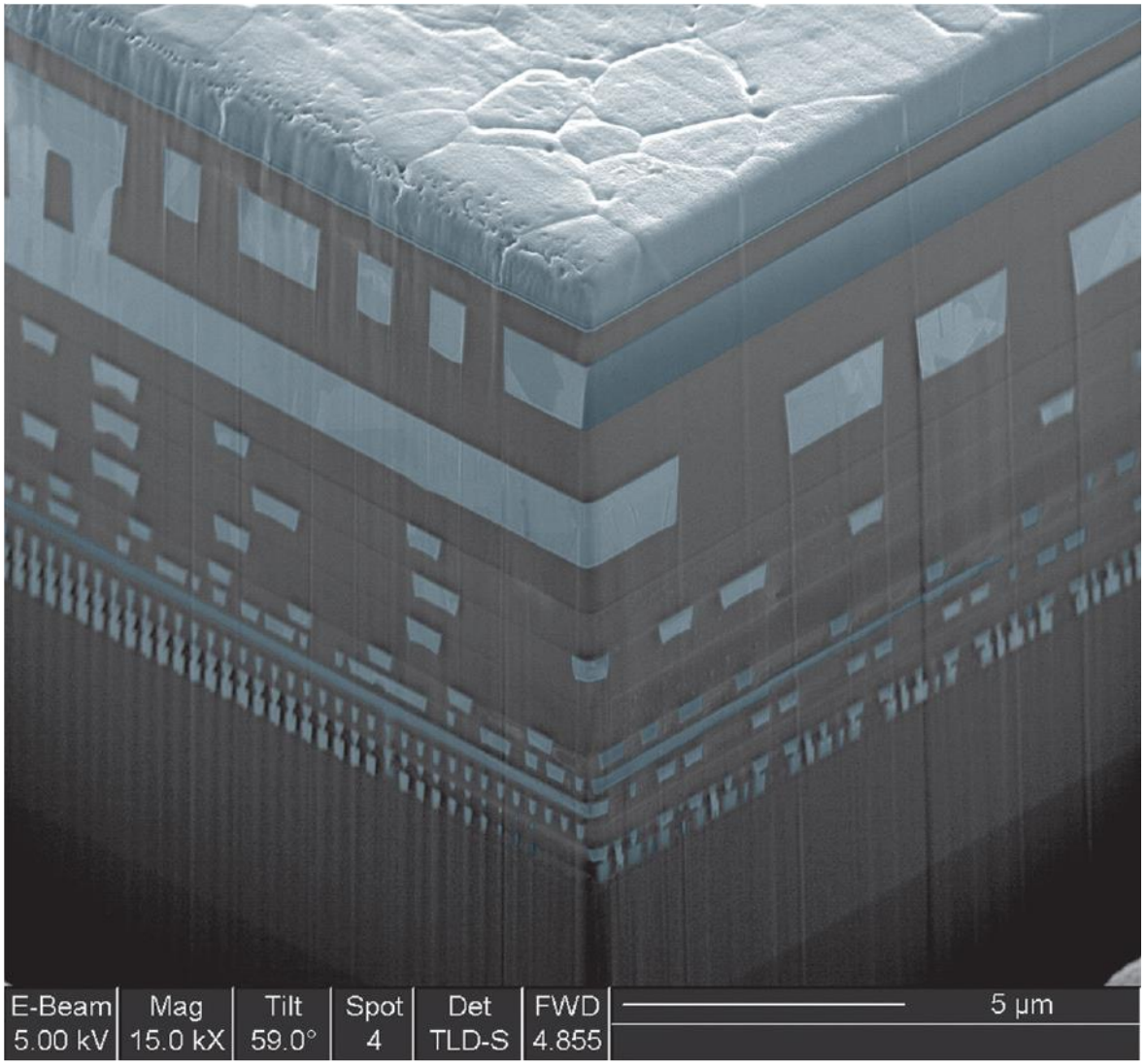
Local Interconnect





Typical metallization cross-section

11 layers of metal [IBM]



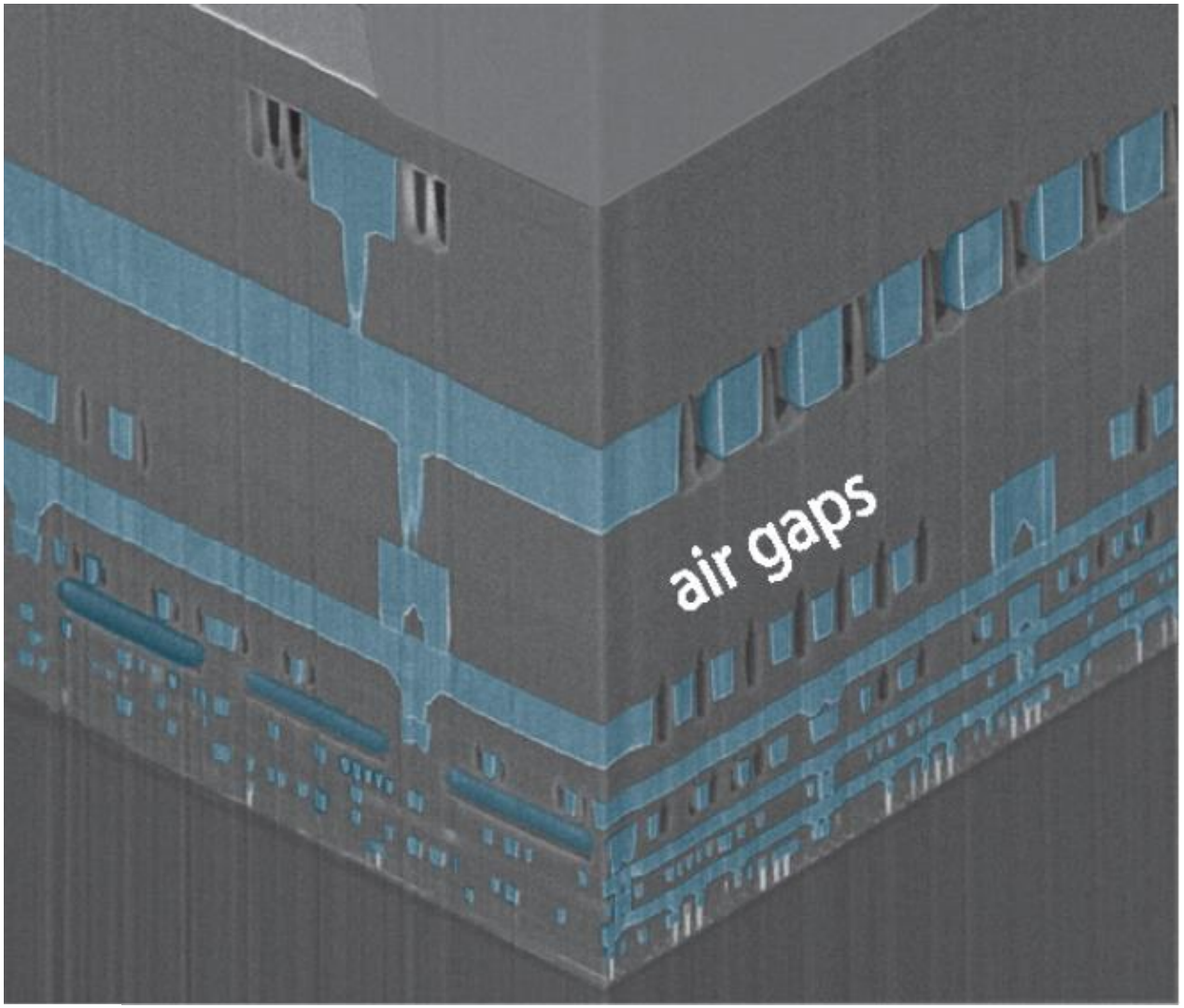
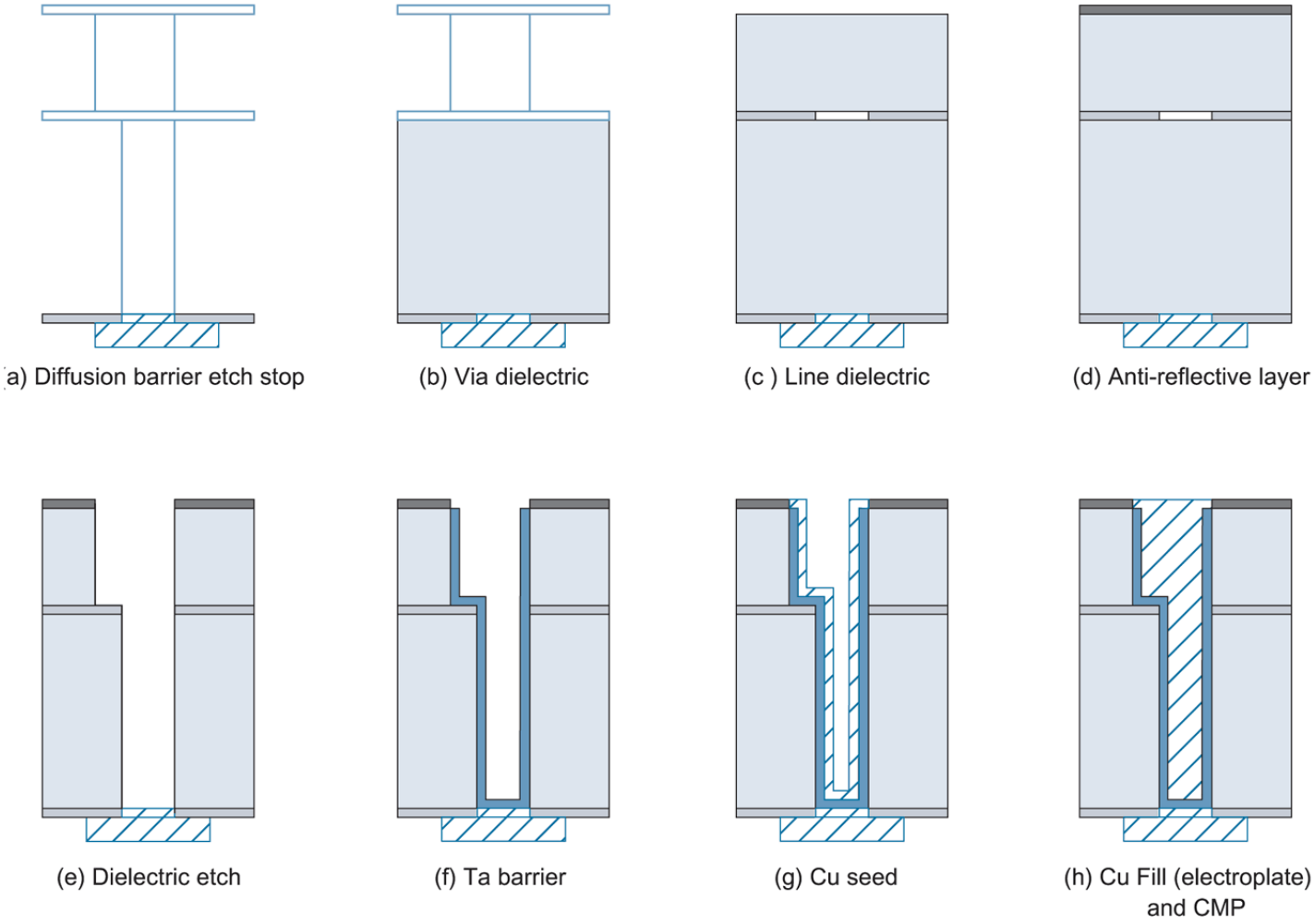
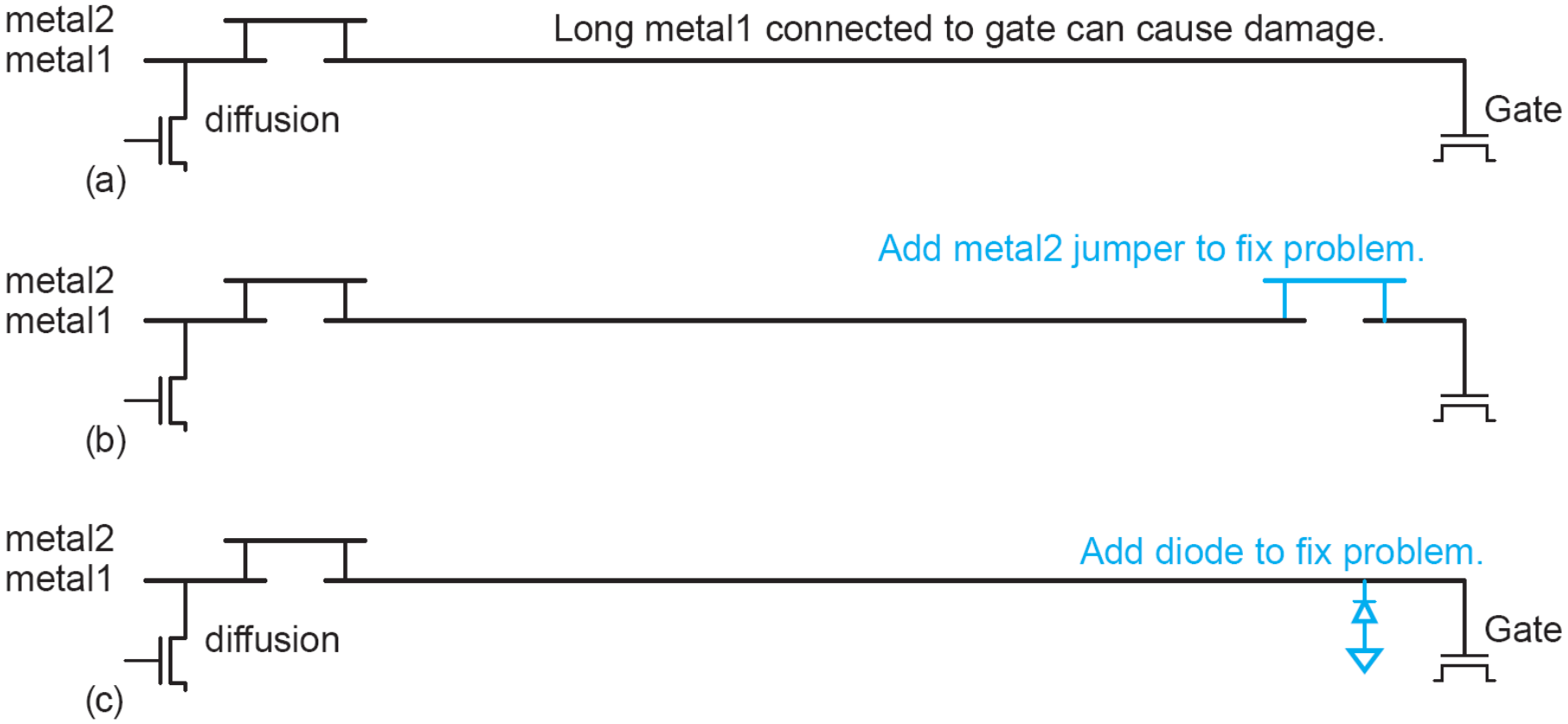


FIGURE 3.22 Micrograph showing air gap insulation between copper wires (Courtesy of International Business Machines Corporation. Unauthorized use not permitted.)



Copper dual damascene interconnect processing steps


metal2
metal1
Long metal1 connected to gate can cause damage.
diffusion
Gate
(a)
Add metal2 jumper to fix problem.
metal2
metal1
(b)
metal2
metal1
Add diode to fix problem.
diffusion
Gate
(c)

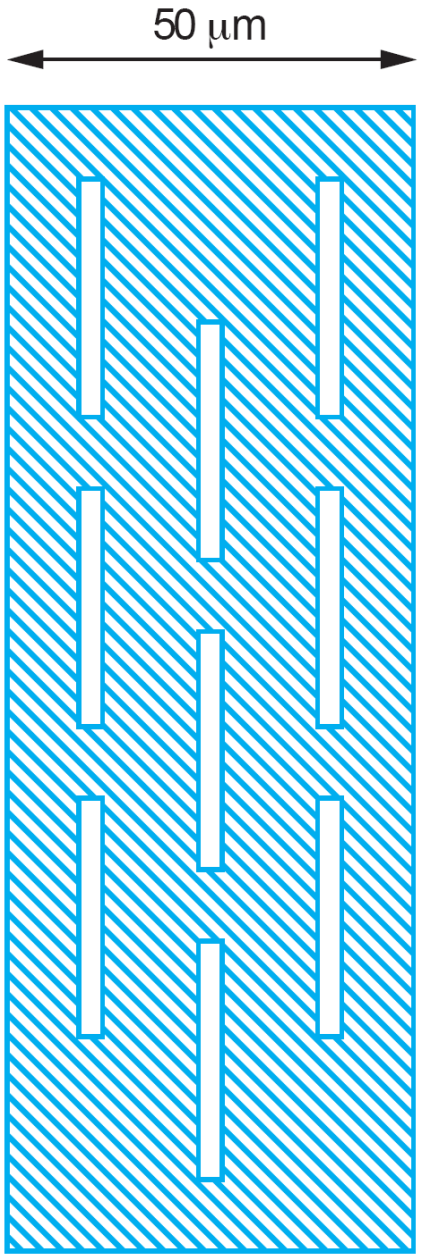
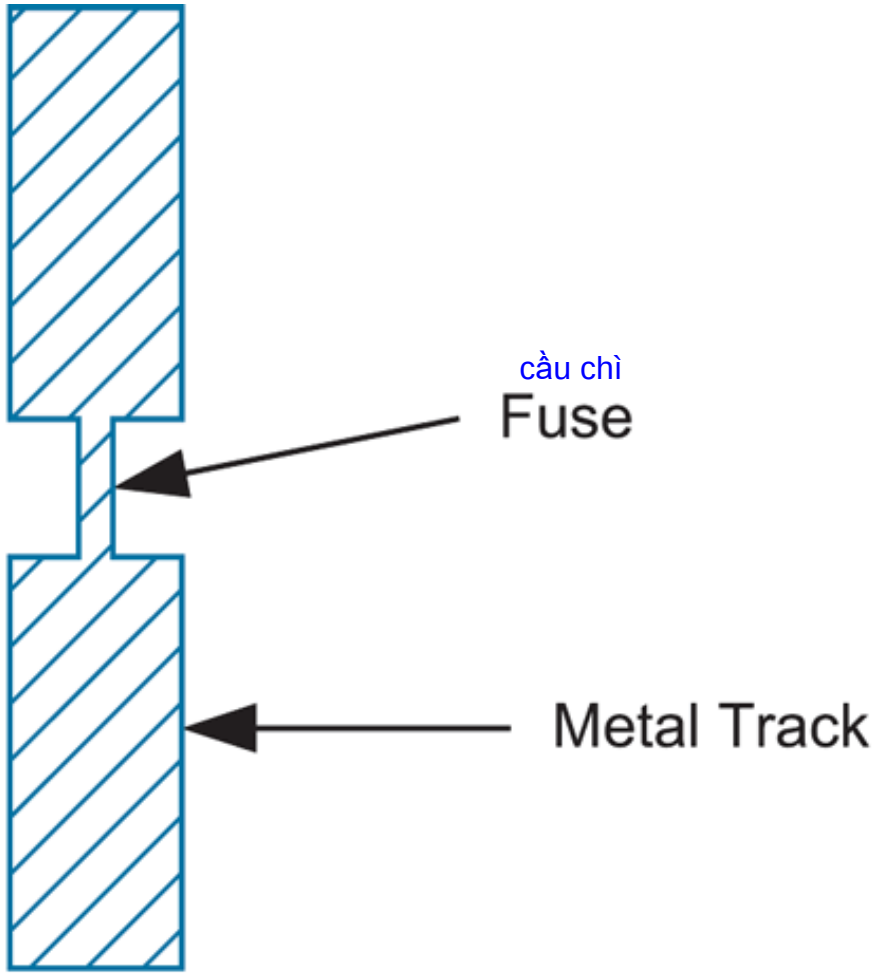
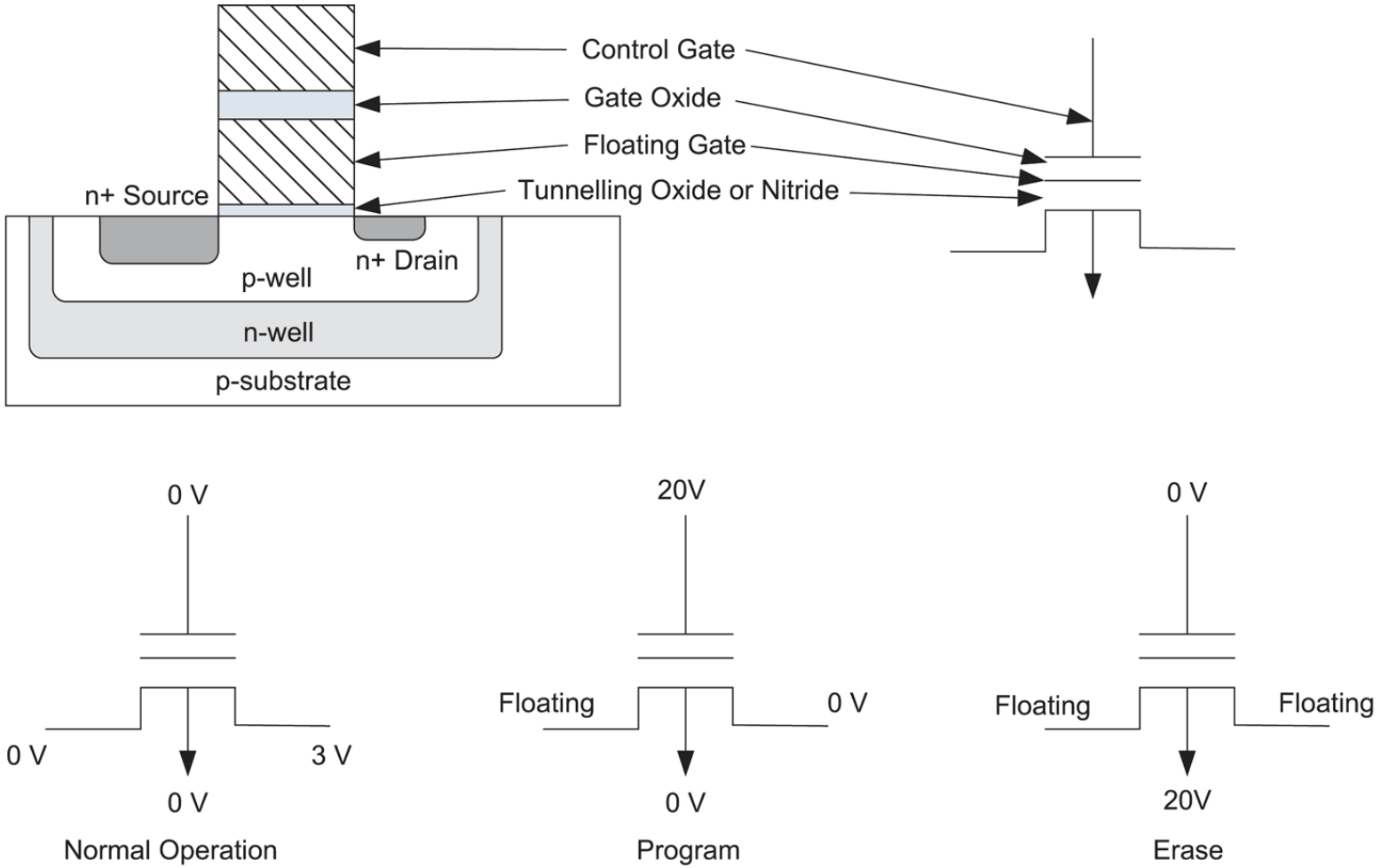


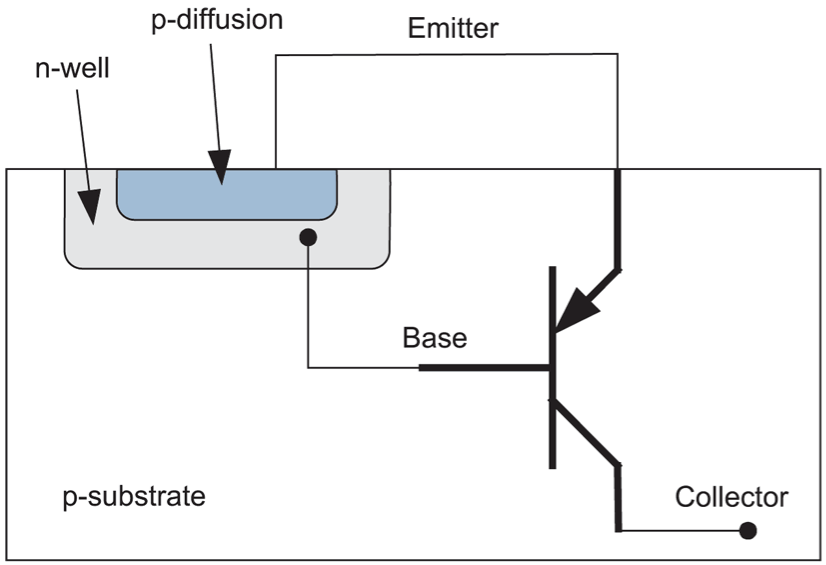
FIGURE 3.37 Slots in wide metal power bus



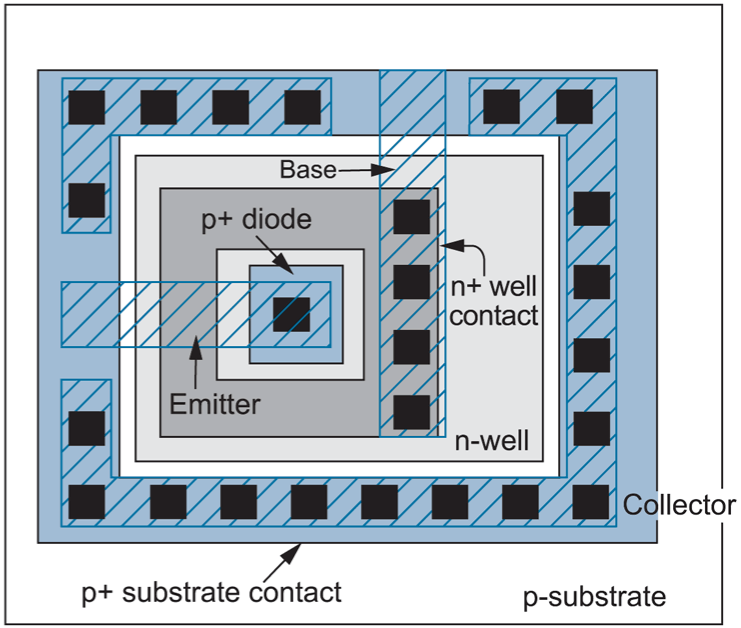
A typical metal fuse



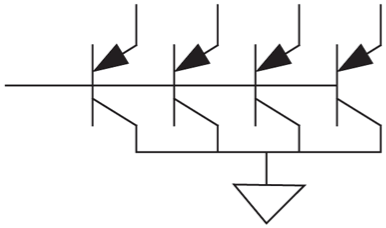
Flash memory construction and operation



Cross-section

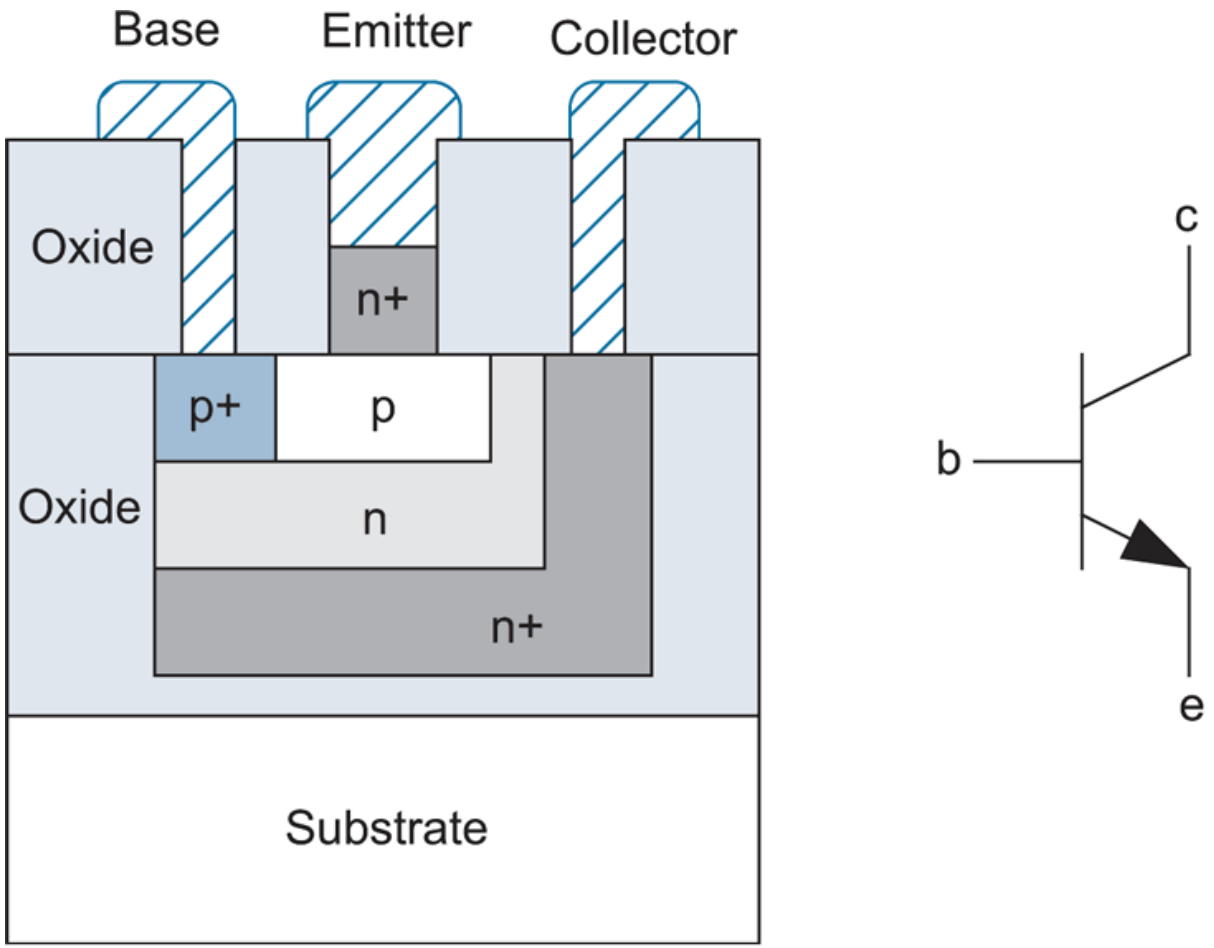


Representative Layout

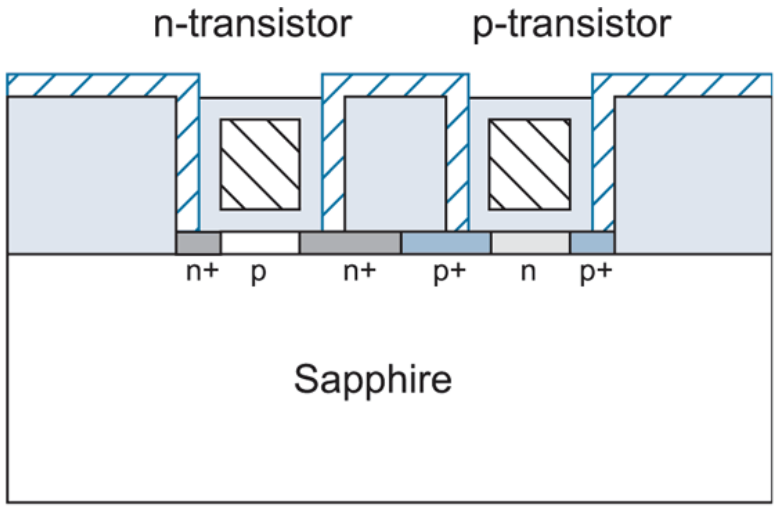


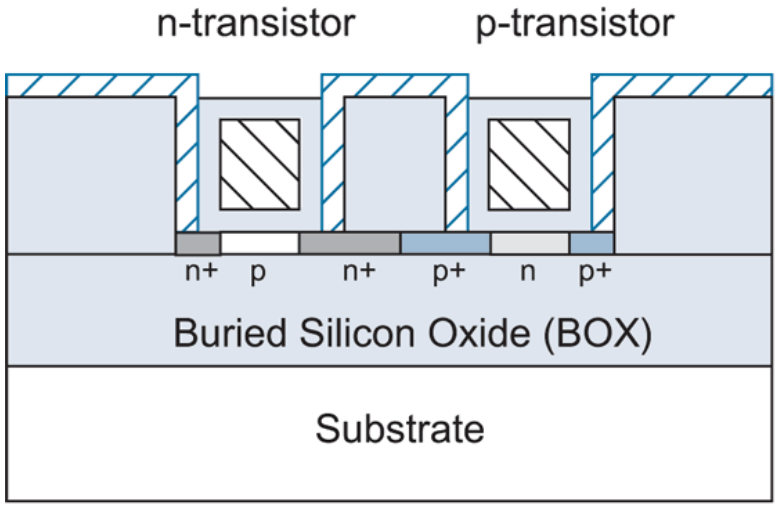
Typical pnp circuit structure as used in voltage reference

Parasitic pnp bipolar transistor



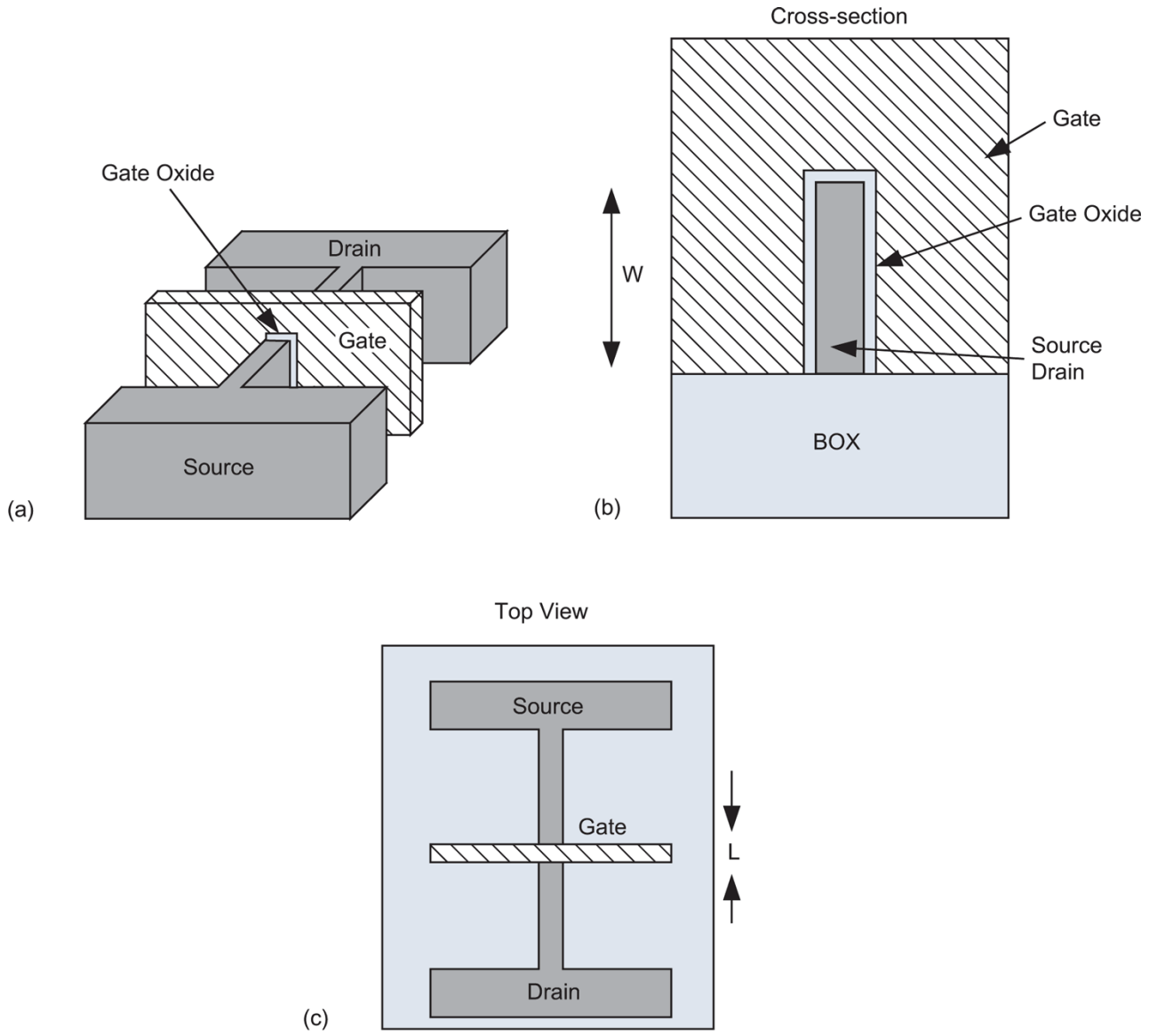
SiGe bipolar transistor structure





SOI types Silicon on Insulator

chất cách điện



Finfet structure

fin: vây

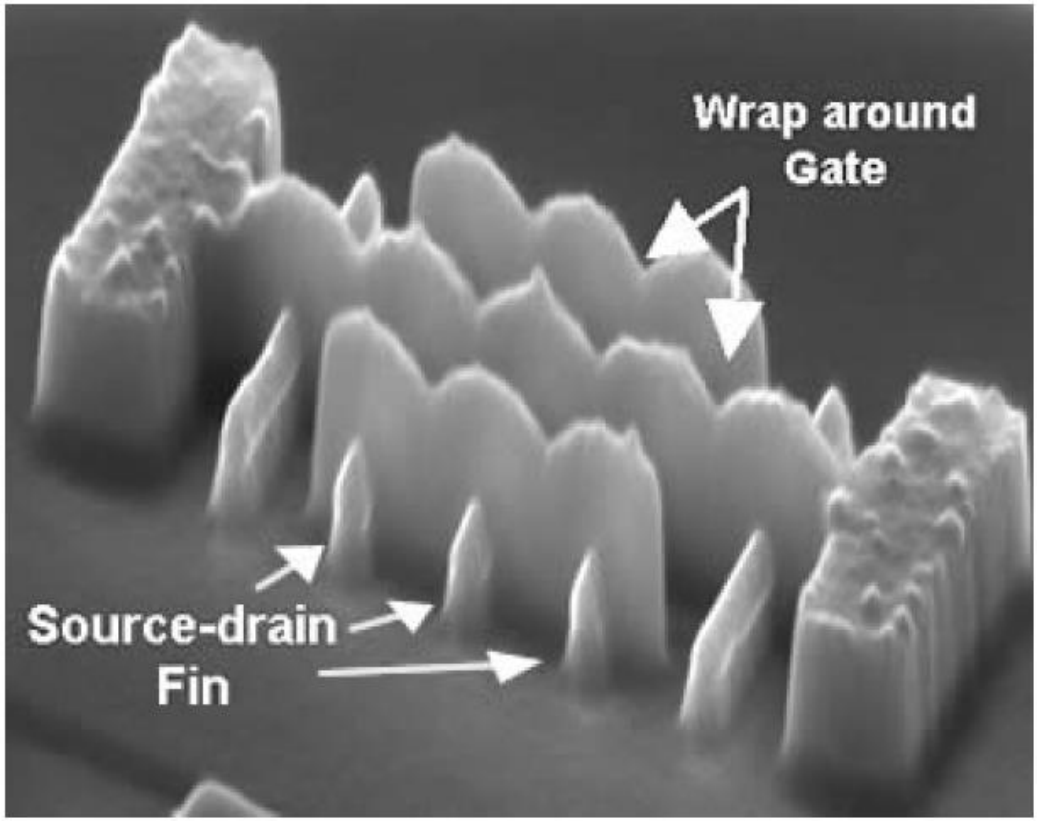
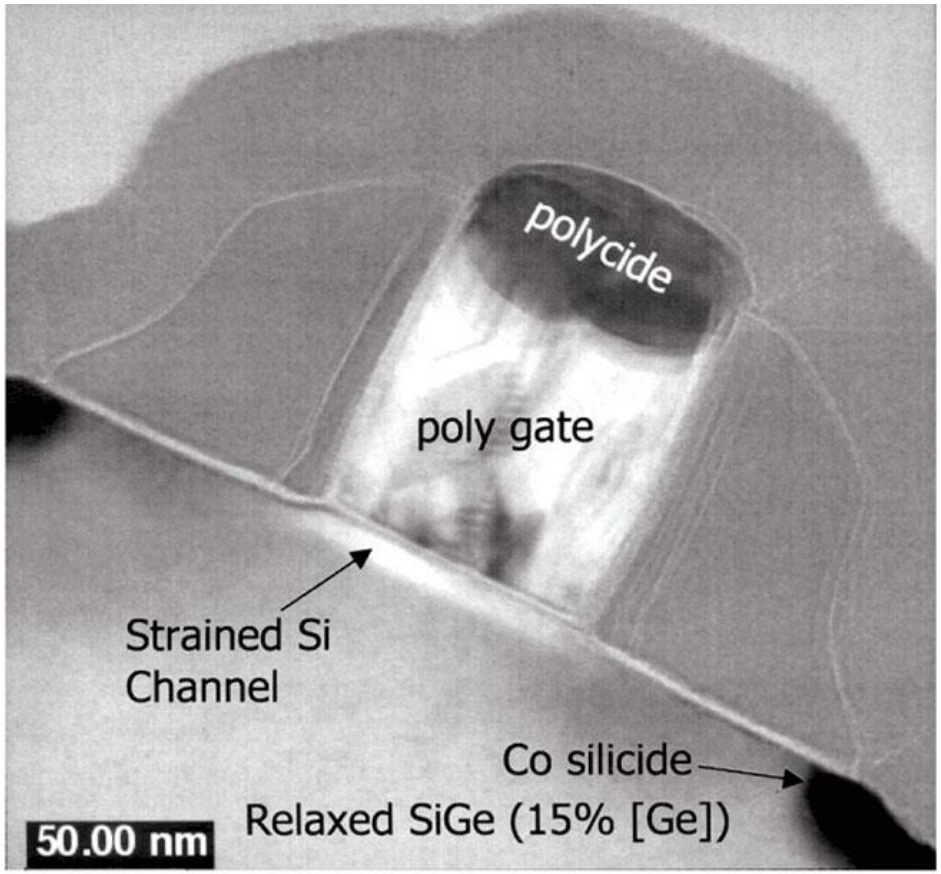


FIGURE 3.34 Trigate transistor (Reprinted with permission of Intel Corporation.)



IBM strained silicon transistor.
Courtesy of International Business Machines Corporation.
Unauthorized use not permitted.

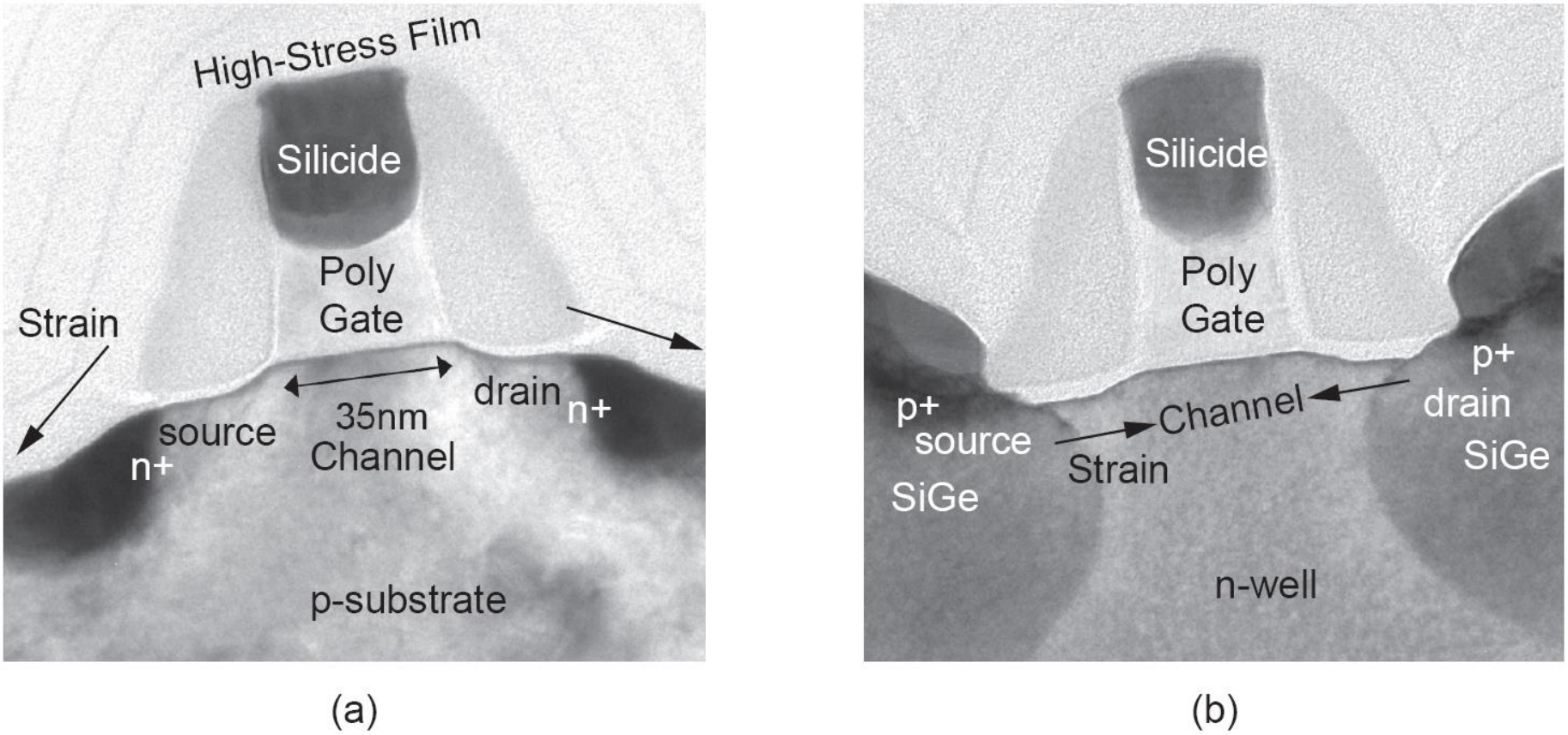
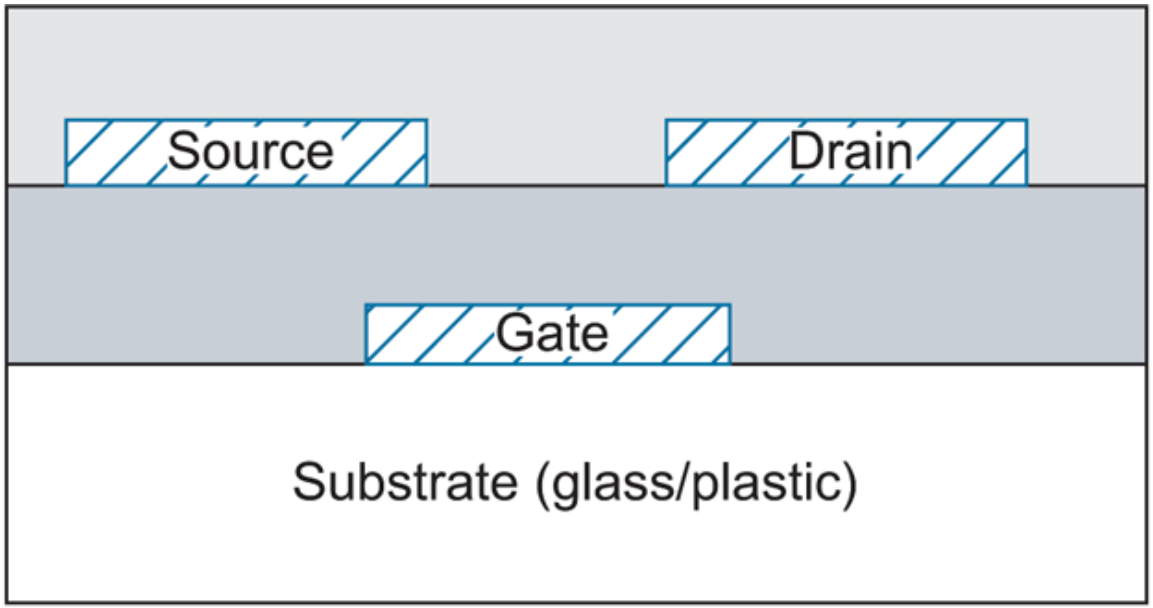


FIGURE 3.19 Strained silicon transistor micrographs: (a) nMOS, (b) pMOS (© IEEE 2005.)

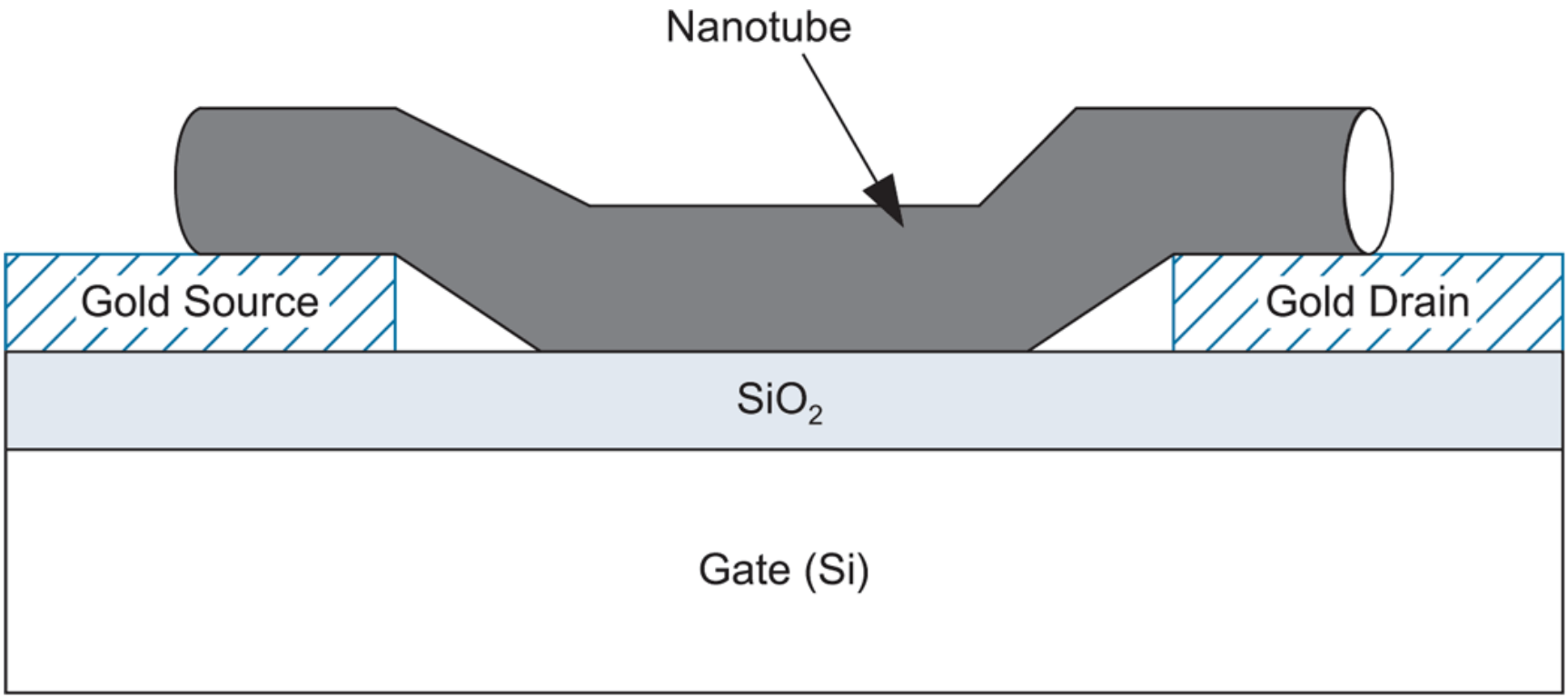


Semiconductor (Pentacene)

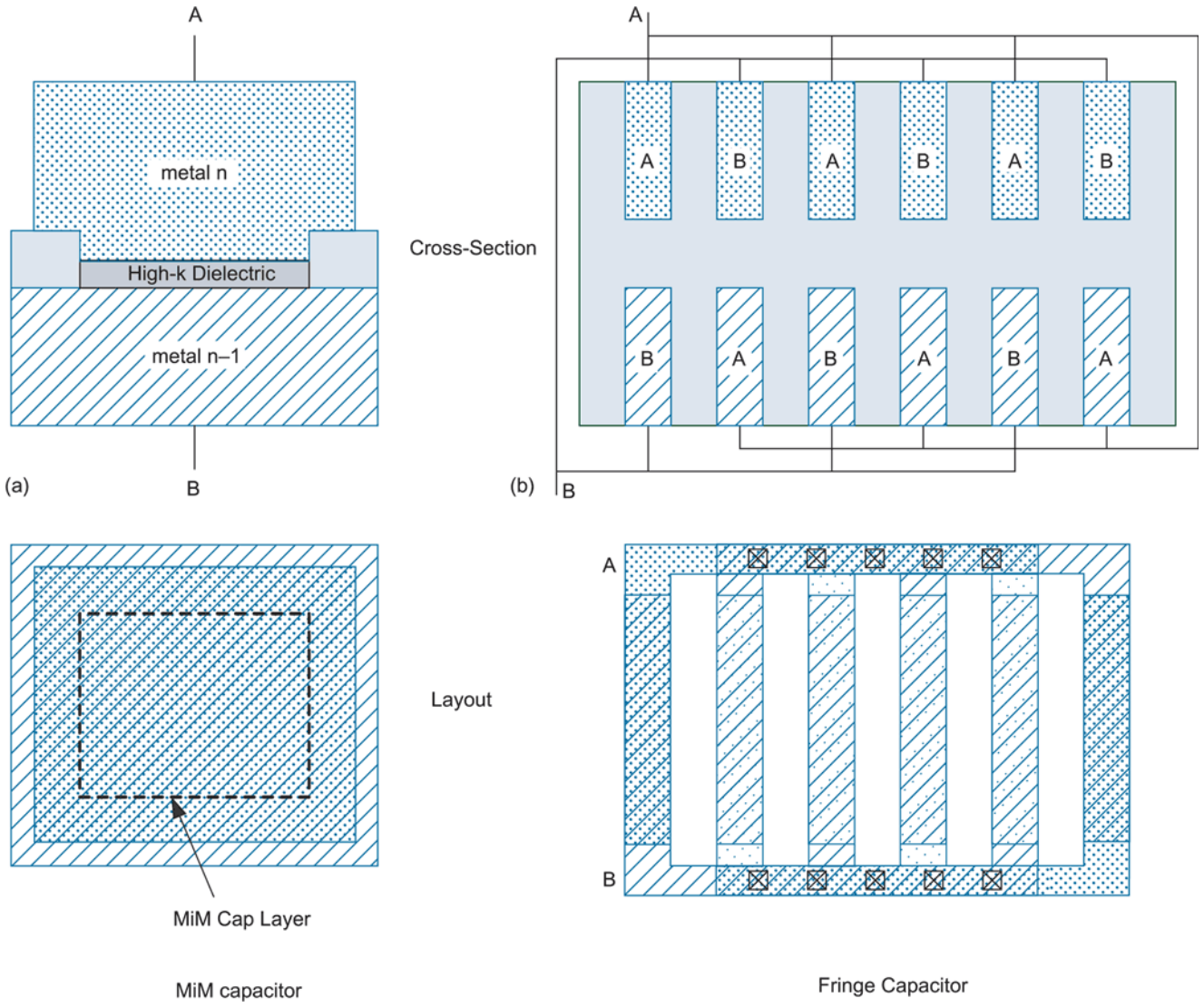
Gold Terminals

Insulator (Polymer Si/Nx)

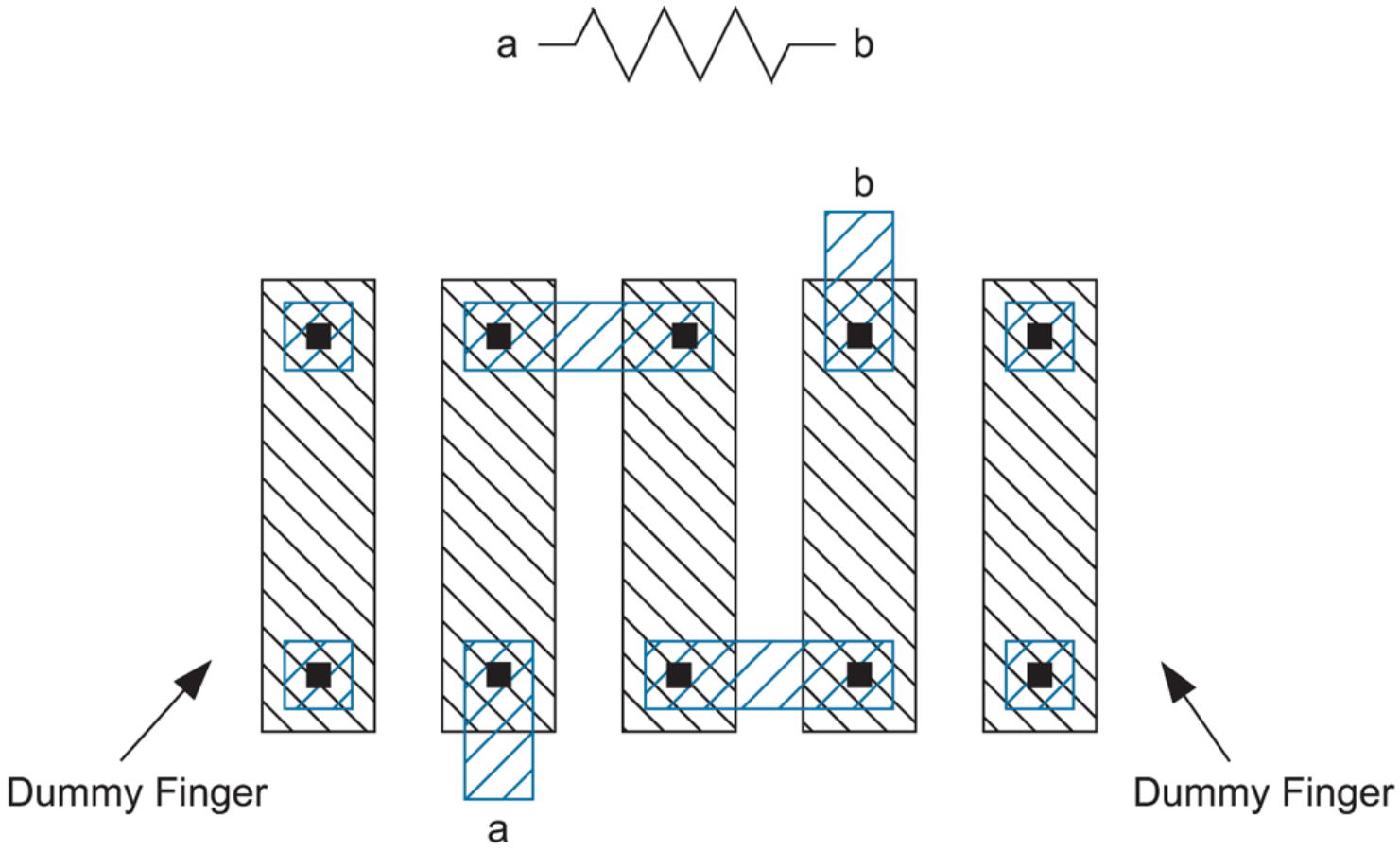
Plastic transistors



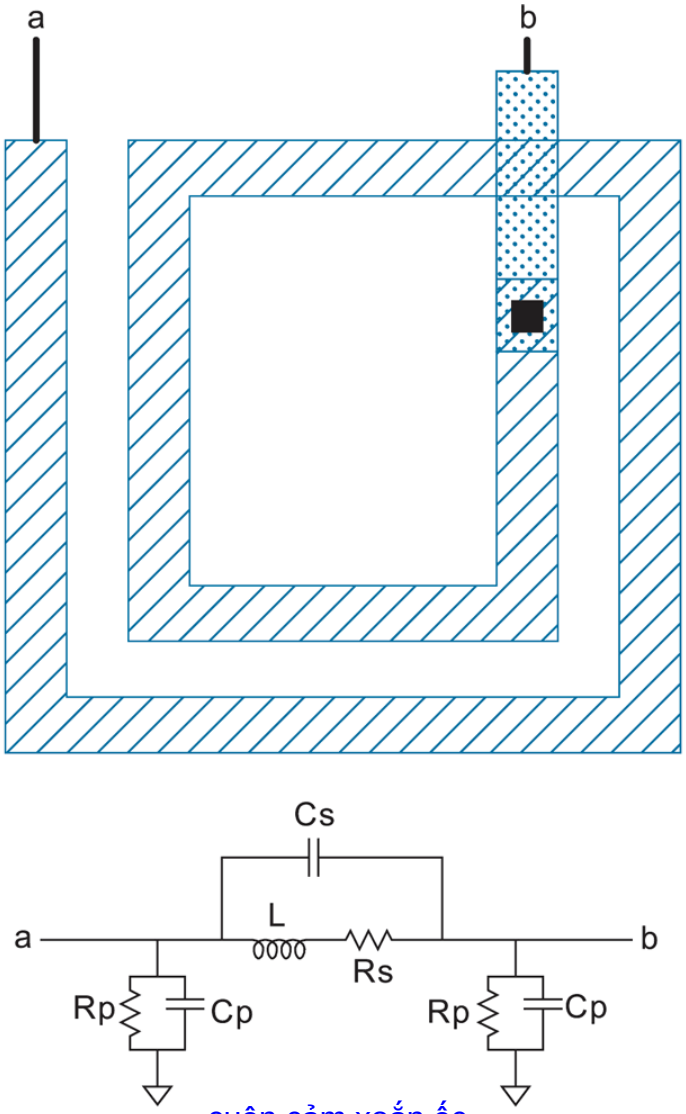
Carbon nanotube transistor



MIM and fringe capacitors

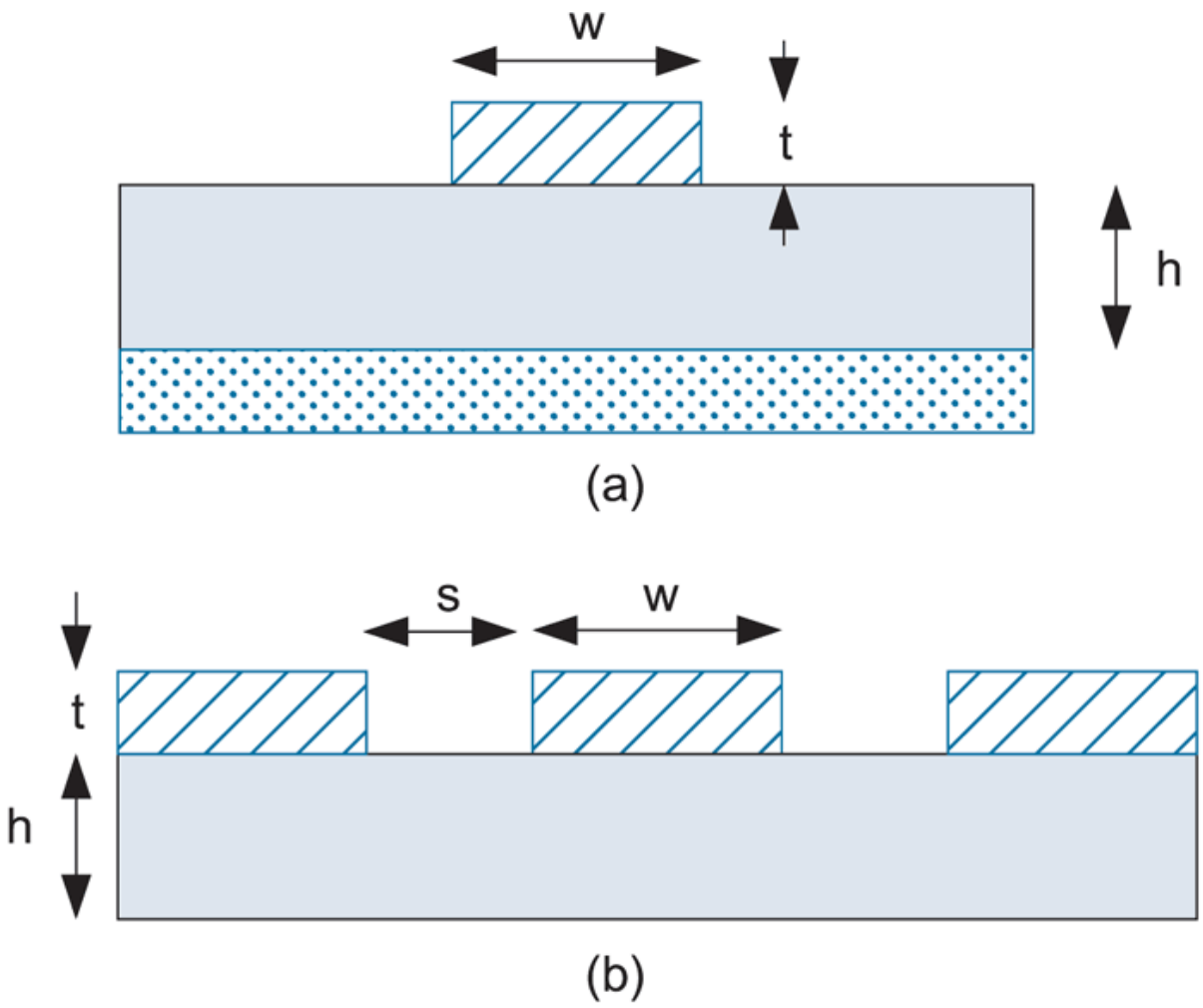


Resistor layout



cuộn cảm xoắn ốc

Typical spiral inductor and equivalent circuit [Rotella02]



Microstrip and coplanar waveguide

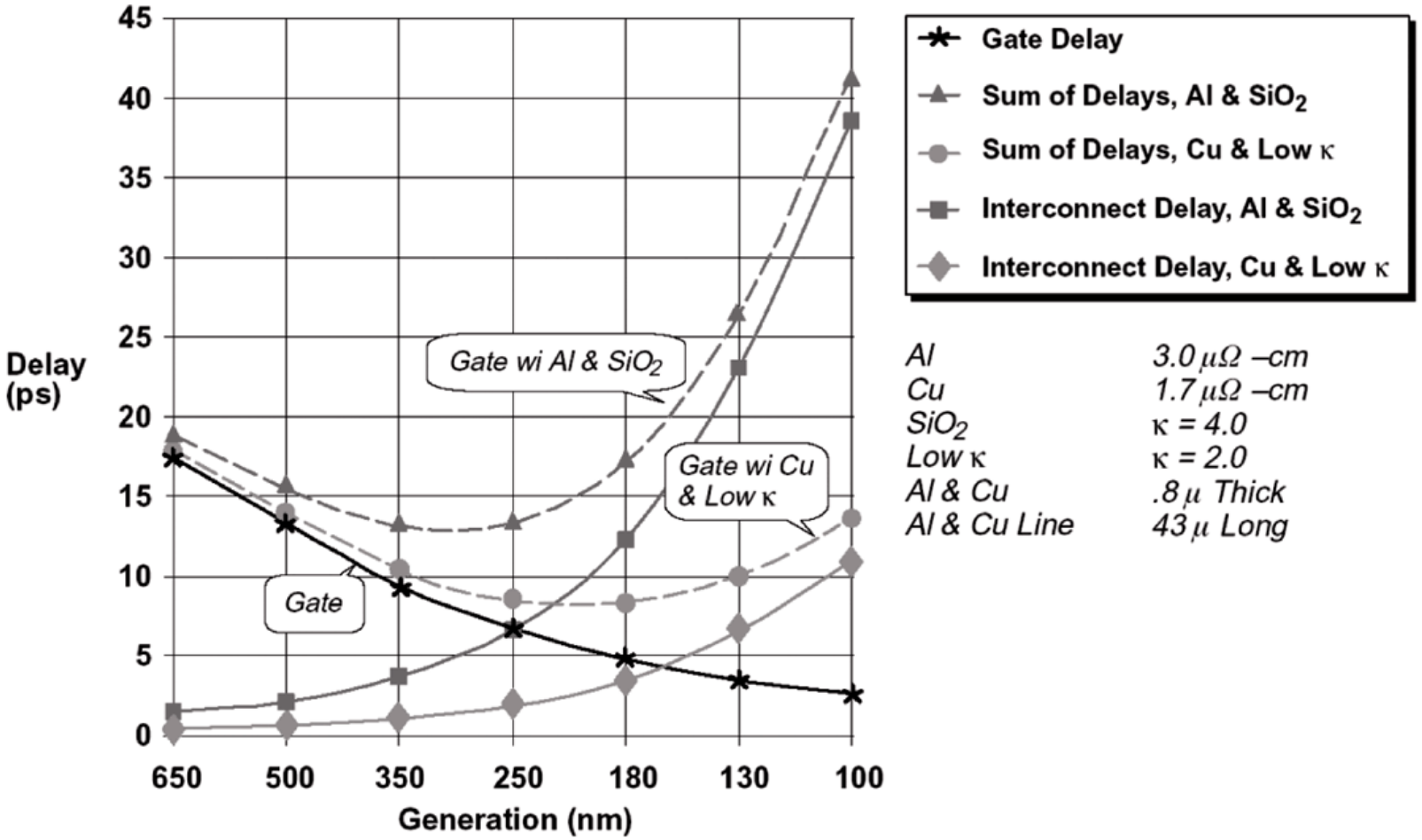


FIG 4.67 Gate and wire delay scaling. Reprinted from [SIA97] with permission of the Semiconductor Industry Association.

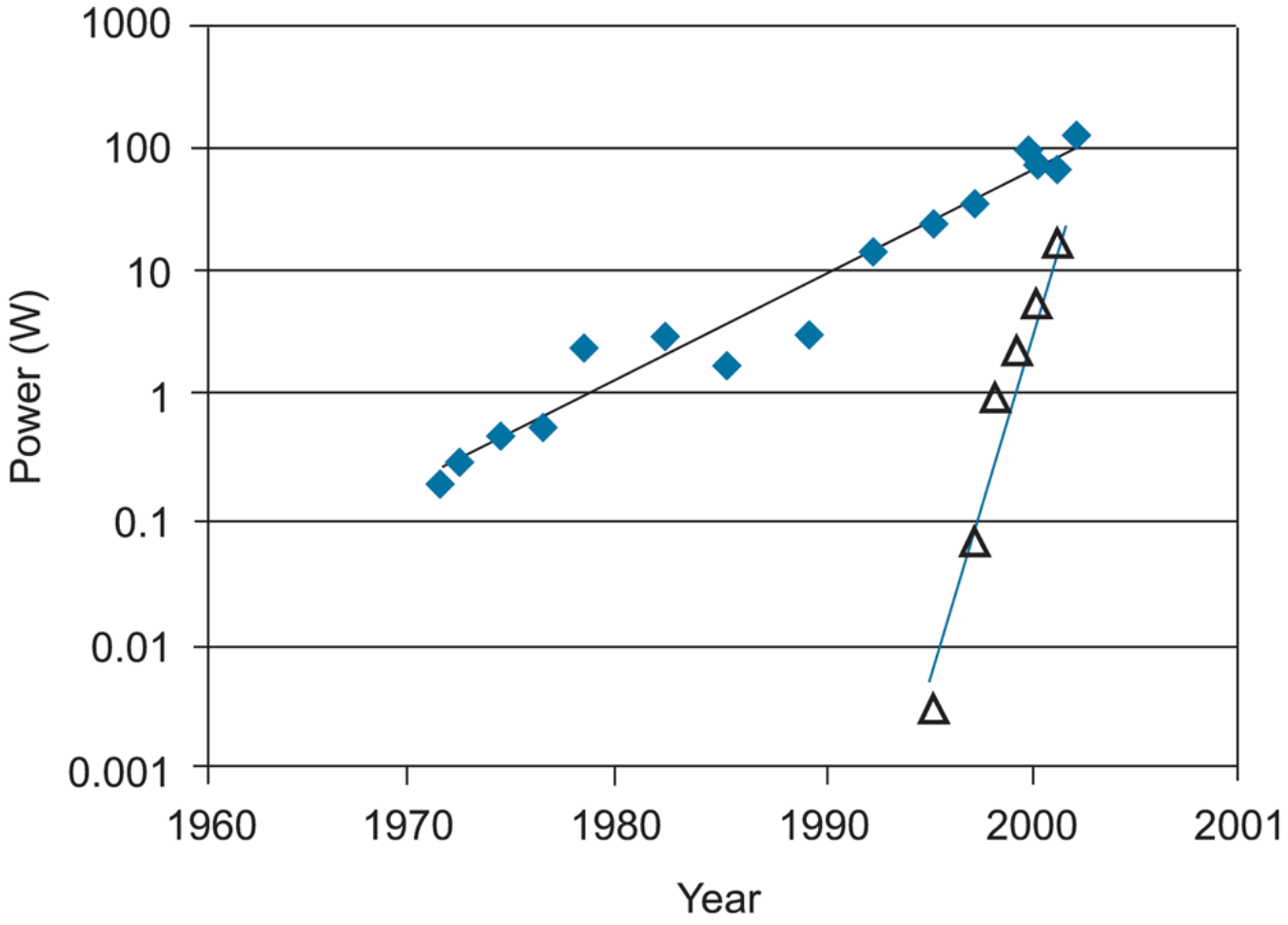
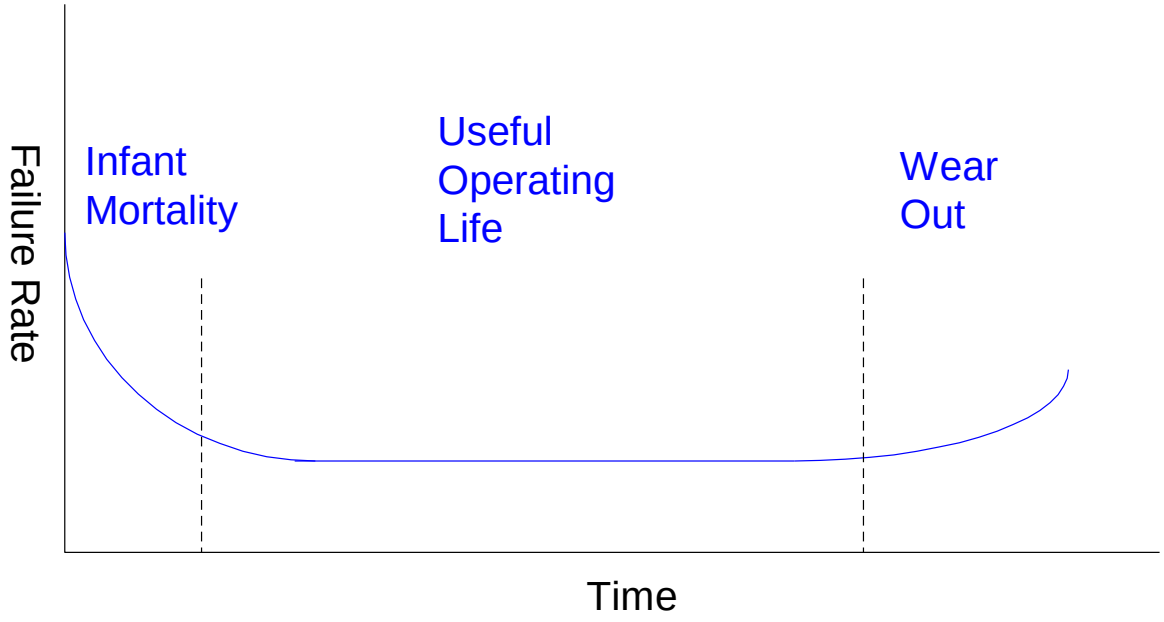


FIG 4.70 Dynamic and static power trends. © IEEE 2003.

Ch7 Robustness & Reliability

Reliability

- Hard Errors
- Soft Errors



Electromigration

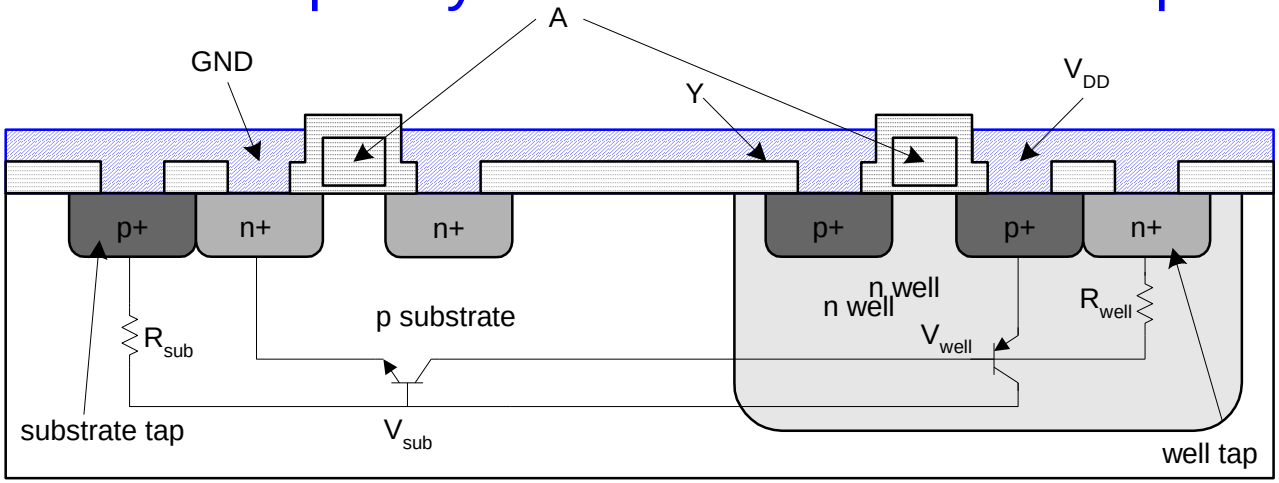
- "Electron wind" causes movement of metal atoms along wires
- Excessive electromigration leads to open circuits
- Most significant for unidirectional (DC) current
  - Depends on current density J_{dc} (current / area)
  - Exponential dependence on temperature
  - Mean Time to Failure (MTTF)
  - Typical limits: $J_{dc} < 1 – 2$ mA / μm^2

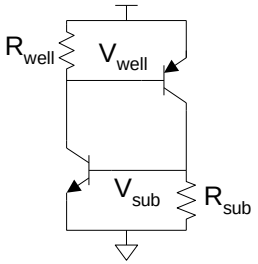
Self-Heating

- Current through wire resistance generates heat
  - Oxide surrounding wires is a thermal insulator
  - Heat tends to build up in wires
  - Hotter wires are more resistive, slower
- Self-heating limits AC current densities for reliability
  - Typical limits: $J_{rms} < 15$ mA / μm^2

Latchup

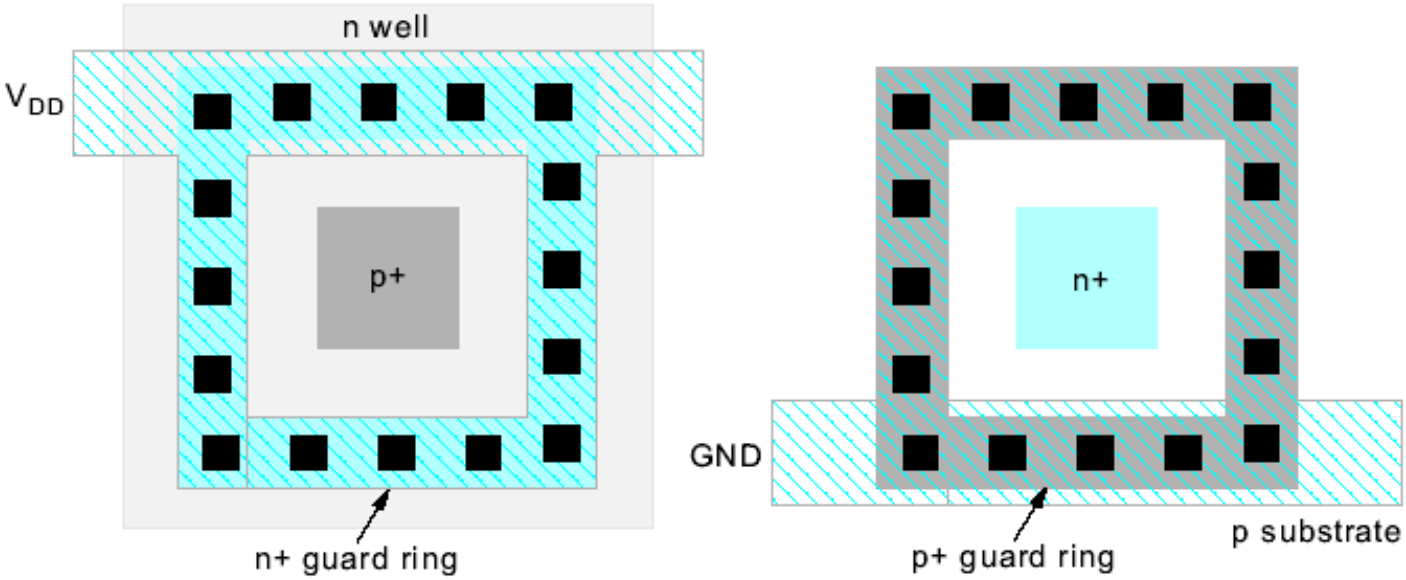
- Latchup: positive feedback leading to V_{DD} – GND short
  - Major problem for 1970's CMOS processes before it was well understood
- Avoid by minimizing resistance of body to GND / V_{DD}
  - Use plenty of substrate and well taps





Guard Rings

- Latchup risk greatest when diffusion-to-substrate diodes could become forward-biased
- Surround sensitive region with guard ring to collect injected charge



Overvoltage

- High voltages can damage transistors
  - Electrostatic discharge
  - Oxide arcing
  - Punchthrough
  - Time-dependent dielectric breakdown (TDDB)
    - Accumulated wear from tunneling currents
- Requires low V_{DD} for thin oxides and short channels
- Use ESD protection structures where chip meets real world

Soft Errors

- In 1970's, DRAMs were observed to occasionally flip bits for no apparent reason
  - Ultimately linked to alpha particles and cosmic rays
- Collisions with particles create electron-hole pairs in substrate
  - These carriers are collected on dynamic nodes, disturbing the voltage
- Minimize soft errors by having plenty of charge on dynamic nodes
- Tolerate errors through ECC, redundancy

Pitfalls Summary

- Static CMOS gates are very robust
  - Will settle to correct value if you wait long enough
- Other circuits suffer from a variety of pitfalls
  - Tradeoff between performance & robustness
- Very important to check circuits for pitfalls
  - For large chips, you need an automatic checker.
  - Design rules aren't worth the paper they are printed on unless you back them up with a tool.