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Noise Margin

Related terms:

Memristors, Complementary Metal Oxide Semiconductor, Inverters, Logic Level, Performance Metric, Supply Voltage, Threshold Voltage, Transistors

Fundamentals of CMOS design

Xinghao Chen, Nur A. Touba, in Electronic Design Automation, 2009

2.2.4 Noise margin

Noise margin is a measure of design margins to ensure circuits functioning properly within specified conditions. Sources of noise include the operation environment, power supply, electric and magnetic fields, and radiation waves. On-chip transistor switching activity can also generate unwanted noise. To ensure that transistors switch properly under specified noisy conditions, circuits must be designed with specified **noise margins**.

Figure 2.12 illustrates noise margin and the terms, assuming that the signal generated by the driving device is wired to the input of the receiving device and that the wire is susceptible to noise. The minimum output voltage of the driving device for logic high, $V_{OH\ min}$, must be greater than the minimum input voltage, $V_{IH\ min}$, of the receiving device for logical high. Because of noise being induced on the wire, a logic high signal at the output of the driving device may arrive with lower voltage at the input of the receiving device. The noise margin, $NM_H = |V_{OH\ min} - V_{IH\ min}|$, for logical high is the range of tolerance for which a logical high signal can still be received correctly. The same can be said with noise margin, $NM_L = |V_{IL\ max} - V_{OL\ max}|$, for logical low, which specifies the range of tolerance for logical low signals on the wire. Smaller noise margins mean circuits are more sensitive to noise.

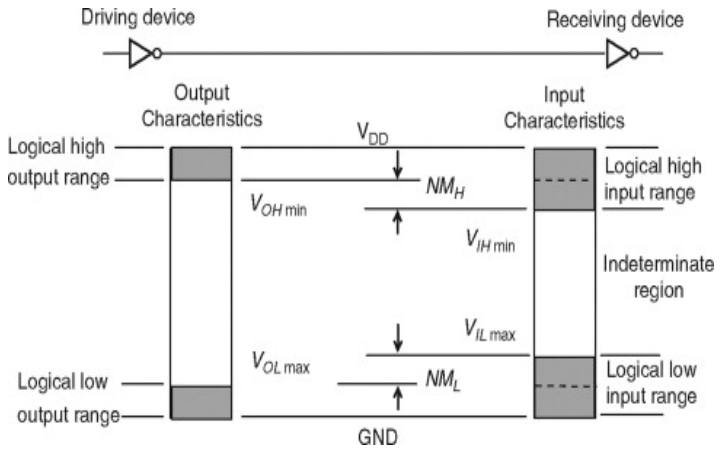

FIGURE 2.12. Noise margin and terms.

It is important to note that as CMOS technologies continue to advance, device feature size gets smaller, and channel length gets shorter. The miniaturization of transistors forces ever lower supply voltages, resulting in smaller noise margins.

Table 2.1 shows the typical noise margin measurements with respect to technology advances.

Table 2.1. Noise Margin Measures for Some Technologies [Wakerly 2001]

	Noise-Margin Measures					
Technology	V_{DD}	V_{OH}	V_{IH}	V_{TH}	V_{IL}	V_{OL}
5-V CMOS	5.0	4.44	3.5	2.5	1.5	0.5
5-V TTL	5.0	2.4	2.0	1.5	0.8	0.4
3.3-V LVTTL	3.3	2.4	2.0	1.5	0.8	0.4
2.5-V CMOS	2.5	2.0	1.7	1.2	0.7	0.4
1.8-V CMOS	1.8	1.45	1.2	0.9	0.65	0.45

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Noise Analysis and Design in Deep Submicron Technology

Mohamed Elgamel, Magdy Bayoumi, in The Electrical Engineering Handbook, 2005

7.4.1 Small-Signal Unity Gain Failure Criteria

Traditional analysis of noise margins rely on the **small-signal unity gain** failure criteria [4]. As illustrated in Figure 7.18, for a small change in input noise to a circuit biased at an operating point, the resultant change in output noise is measured. If $|d(\text{output})/d(\text{input})| > 1$ then the circuit is considered unstable. Unity gain is a good design metric but is neither necessary nor sufficient for noise immunity.

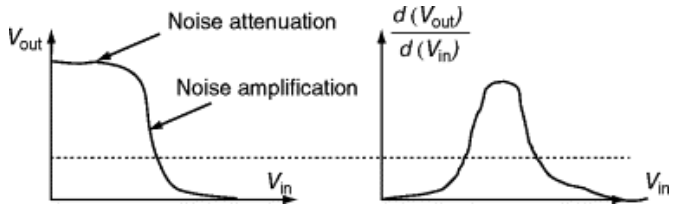

FIGURE 7.18. Direct Current Transfer Function of an Inverter Illustrating Small-Signal Unity Gain

Most aggressively designed paths have some noise-sensitive stages interspersed with quiet stages. Some noise amplification needs to be allowed in the sensitive stage because it should be attenuated in the quiet stage.

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From Zero to One

Sarah L. Harris, David Money Harris, in Digital Design and Computer Architecture, 2016

1.6.3 Noise Margins

If the output of the driver is to be correctly interpreted at the input of the receiver, we must choose $V_{ol} < V_{Il}$ and $V_{oh} > V_{IH}$. Thus, even if the output of the driver is contaminated by some noise, the input of the receiver will still detect the correct logic level. The *noise margin* is the amount of noise that could be added to a worst-case output such that the signal can still be interpreted as a valid input. As can be seen in Figure 1.23, the low and high noise margins are, respectively

$$NM_L = V_{IL} - V_{OL} \tag{1.2}$$

$$NM_H = V_{OH} - V_{IH} \tag{1.3}$$

Example 1.18

Calculating Noise Margins

Consider the inverter circuit of Figure 1.24. V_{O1} is the output voltage of inverter I1, and V_{I2} is the input voltage of inverter I2. Both inverters have the following characteristics: $V_{DD} = 5$ V, $V_{IL} = 1.35$ V, $V_{IH} = 3.15$ V, $V_{OL} = 0.33$ V, and $V_{OH} = 3.84$ V. What are the inverter low and high noise margins? Can the circuit tolerate 1 V of noise between V_{O1} and V_{I2}?

Figure 1.24. Inverter circuit

Solution

The inverter noise margins are: $NM_L = V_{IL} - V_{OL} = (1.35\text{ V} - 0.33\text{ V}) = 1.02$ V, $NM_H = V_{OH} - V_{IH} = (3.84\text{ V} - 3.15\text{ V}) = 0.69$ V. The circuit can tolerate 1 V of noise when the output is LOW ($NM_L = 1.02$ V) but not when the output is HIGH ($NM_H = 0.69$ V). For example, suppose the driver, I1, outputs its worst-case HIGH value, $V_{O1} = V_{OH} = 3.84$ V. If noise causes the voltage to droop by 1 V before reaching the input of the receiver, $V_{I2} = (3.84\text{ V} - 1\text{ V}) = 2.84$ V. This is less than the acceptable input HIGH value, $V_{IH} = 3.15$ V, so the receiver may not sense a proper HIGH input.

V_{dd} stands for the voltage on the *drain* of a metal-oxide-semiconductor transistor, used to build most modern chips. The power supply voltage is also sometimes called V_{CC}, standing for the voltage on the *collector* of a bipolar junction transistor used to build chips in an older technology. Ground is sometimes called V_{SS} because it is the voltage on the *source* of a metal-oxide-semiconductor transistor. See Section 1.7 for more information on transistors.

DC indicates behavior when an input voltage is held constant or changes slowly enough for the rest of the system to keep up. The term's historical root comes from *direct current*, a method of transmitting power across a line with a constant voltage. In contrast, the *transient response* of a circuit is the behavior when an input voltage changes rapidly. Section 2.9 explores transient response further.

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Noise in Analog and Digital Systems

Erik A. McShane, Krishna Shenai, in The Electrical Engineering Handbook, 2005

2.3.4 Noise Margins

The *I/O* noise margins, NM_L and NM_H, refer to the ability of a logic gate to accommodate input noise without producing a faulty logic output. The input noise threshold levels, V_{IL} and V_{IH}, are by convention defined as the input voltages that result in a slope of –1 in the dV_O/dV_I response. This is shown in Figure 2.8. As is clear from Table 2.4, the noise margins of CMOS logic gates are larger than for comparable NMOS technologies. This is evident because CMOS delivers rail-to-rail outputs, whereas the V_{OL} is a circuit constraint in NMOS.

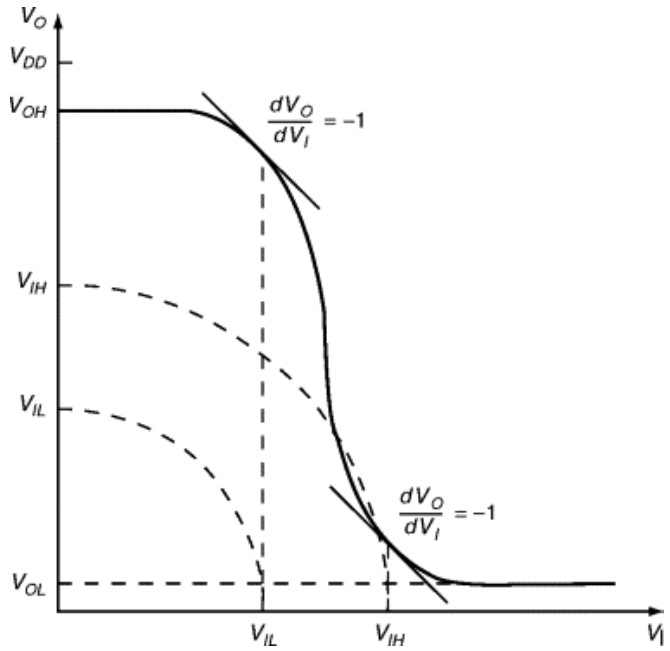

FIGURE 2.8.

The noise margins of a CMOS gate can be found by first examining the dc transfer curve shown in Figure 2.8. From graphical analysis, the V_{IL} occurs when the PMOS is in its linear regime and the NMOS is in its saturation regime. Since a CMOS gate is complementary in operation, the V_{IH} by symmetry occurs when the PMOS is in its saturation regime and the NMOS is in its linear regime.

Considering first the CMOS V_{IL}, begin by equating the NMOS and PMOS currents:

$$k_n \frac{W_n}{L_n} \frac{(V_I - V_{Tn})^2}{2} = k_p \frac{W_p}{L_p} \left(V_I - Vdd - V_{Tp} - \frac{V_O - Vdd}{2} \right) (V_O - Vdd). \tag{2.22}$$

Assuming that the inverter is designed to have a balanced transfer curve such that:

$$k_n \frac{W_n}{L_n} = k_p \frac{W_p}{L_p}, \tag{2.23}$$

then equation 2.22 reduces to a simpler form such that:

$$V_{IL} = \frac{3Vdd + 3V_{TP} + 5V_{TN}}{8}. \tag{2.24}$$

Considering next the CMOS V_{IH}, equating the NMOS and PMOS currents results in:

$$k_n \frac{W_n}{L_n} \left(V_I - V_{Tn} - \frac{V_O}{2} \right) V_O = k_p \frac{W_p}{L_p} \frac{(V_I - Vdd - V_{Tp})^2}{2}. \tag{2.25}$$

Again using the assumption of equation 2.23, this expression can also be reduced and rearranged, yielding the form:

$$V_{IH} = \frac{5Vdd + 5V_{TP} + 3V_{TN}}{8}. \tag{2.26}$$

The noise margins of an NMOS inverter can be found using similar methods. The derivations are not shown here but the steps are identified. Beginning with V_{IH} and examining through graphical techniques the output characteristics, the NMOS

inverter is found to be equivalent to the CMOS case; that is, the driver (enhancement mode) is in the linear regime and the load (depletion mode) is in the saturation regime. Assuming that the inverter pull-up: pull-down ratio is *k*, then:

$$V_{IH} = V_{TN} - \frac{2V_{TD}}{\sqrt{3k}}. \tag{2.27}$$

Considering the NMOS V_{IL}, the driver and load bias regimes are exchanged (as in CMOS), and the result is as follows:

$$V_{IL} = V_{TN} - \frac{V_{TD}}{\sqrt{k(1+k)}}. \tag{2.28}$$

Note that the NM_H of NMOS and CMOS inverters are similar since both achieve $V_{OH} \approx Vdd$. Because an NMOS inverter V_{OL} is not zero (100 mV – 500 mV are typical values), however, the NM_L of NMOS is considerably lower than for a CMOS inverter.

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Domino Circuits

David Harris, in Skew-Tolerant Circuit Design, 2001

Noise Feedthrough

When the input of a gate is near its noise margin, the output voltage will not be at the rail. Therefore, the input of the next gate will see some noise; this is called *noise feedthrough* or *residual noise*. Indeed, the noise margin of a gate is defined by this feedthrough: it is the point at which the noise slope of the transfer function is –1 so that the marginal increase in noise feedthrough to the next gate equals the marginal increase in noise margin of the current gate.

Figure 3.23 shows the transfer function of a hi-skew inverter using a pmos transistor four times as large as the nmos transistor. Because we are using the inverter after a dynamic gate, we are concerned about the high input noise margin, the amount the dynamic output can droop before the hi-skew inverter no longer produces a valid 0. This is determined by the unity-gain point marked on the transfer curve. Notice that at this point, the output is not quite zero. The nonzero voltage shows up as noise at the sensitive input of the next dynamic gate. In this case, the noise margin is 1.22 volts (37% of the supply) and the noise feedthrough is 0.23 volts (7% of the supply).

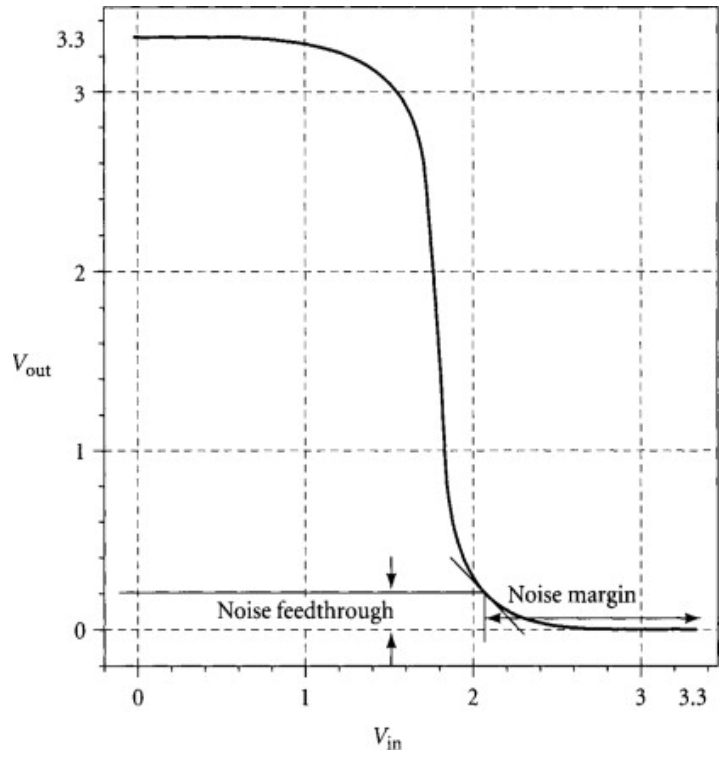

Figure 3.23. Inverter transfer function

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Implementation Issues

Bruce Jacob, ... David T. Wang, in Memory Systems, 2008

Transistor Sizing

The main initial considerations when sizing the transistors of the memory cell are the cell's area and its stability as measured by its static-noise margin (SNM). The SNM is defined as the amount of DC noise necessary to disturb the internal storage node of the cell and flip its stored data [Lohstroh et al. 1983]. The cell's stability affects the cell's SER and its sensitivity to PVT variations.

The cell's SNM can be calculated analytically by solving the cross-coupled inverter voltage transfer equations. Alternatively, it can be estimated using the graphical "maximum squares" method using the inverter's I/O voltage transfer function [Seevinck 1987], as shown in Figure 5.5.

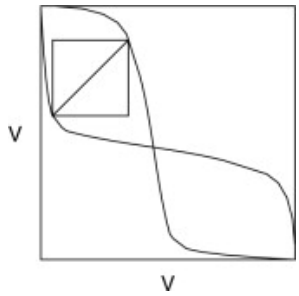

FIGURE 5.5. The inverter's voltage transfer function.

When sizing, the main variables that can be varied are the widths and lengths of the driver, pullup, and access transistors.

Using the terminology from Seevinck, sizing involves the parameters (r, β, q), where the beta figure β is the ratio of the widths and lengths of the individual FETs,

r is the ratio between the beta figures of the driver and the access transistor, and q is the ratio of the beta figures of the pullup and the access transistors.

The main conclusions from Seevinck's analysis is as follows:

1. The SNM depends only on Vdd, transistor voltages, and beta ratios, not on the absolute values of the transistor betas.
2. Designing the cells for maximum SNM requires maximizing r and q/r by the appropriate choice of W/L ratios, constrained by area limitations and a proper cell-write operation (i.e., some choices of W/L ratios will be difficult to write to).
3. For fixed r and q, the SNM of 6T MC will be independent of Vdd variations.
4. Finally, the SNM increases with increasing threshold voltages.

All of these factors must be considered and balanced when designing the memory cell to achieve the desired cell area, stability, and performance.

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URL: https://www.sciencedirect.com/science/article/pii/B9780123797513500072

Electromagnetic Compatibility

J.F. Dawson, ... C.A. Marshman, in Encyclopedia of Physical Science and Technology (Third Edition), 2003

IV.B.2 Robust, Quiet Circuits

If circuits can be made robust in the presence of interference, then the need for shielding and filtering can be reduced. We suggest the following rules.

a. Select logic circuits with the lowest bandwidth and highest noise margins.
b. Minimize the bandwidth of analog circuits.
c. Apply adequate decoupling on analog and digital circuits.
d. Consider the recovery of analog circuits from transients (simple measures such as limiter diodes can reduce recovery times drastically).
e. Consider carefully partitioning and noise propagation in power supplies.
f. Ensure that unused states in digital (and microprocessor) circuits have transitions into safe states to allow recovery after disruption by interference and use “watchdog” circuits to force reset after failure in microprocessor systems.
g. Separate I/O busses from the main processor bus to reduce interference transfer to and from interfaces.
h. Use filters and/or isolation to prevent interference propagation.

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URL: https://www.sciencedirect.com/science/article/pii/B0122274105002106

Durable Phase-Change Memory Architectures

Marjan Asadinia, Hamid Sarbazi-Azad, in Advances in Computers, 2020

7.1 Analysis of drift tolerance

It should be noted that the main feature of VR-PCM is the interstate noise margin reduction in an MLC cell. This narrower noise margin in VR-PCM would consume less energy as it reduces the number of integrations required during P&V. But still this narrow noise margin might be insufficient to avoid the overlapping of states from the unwanted resistance drift. If the final design could tolerate the resistance drift leading to soft errors, VR-PCM would be energy efficient and acceptable. To analyze MLC PCM reliability, we show the bit error rate of the readout data in Fig. 8 for the evaluated structures in Section 5 for various workloads. Indeed, using the resistance partitioning model used throughout analysis, the conventional baseline memory and VR-PCM MLC designs tolerate about 1.2 s and 1.23 s drift at 300°K,

respectively. As it is shown in this figure, the same level of drift reliability with an average of 16.1% reduction in writes' energy is presented by VR-PCM and its alternative designs.

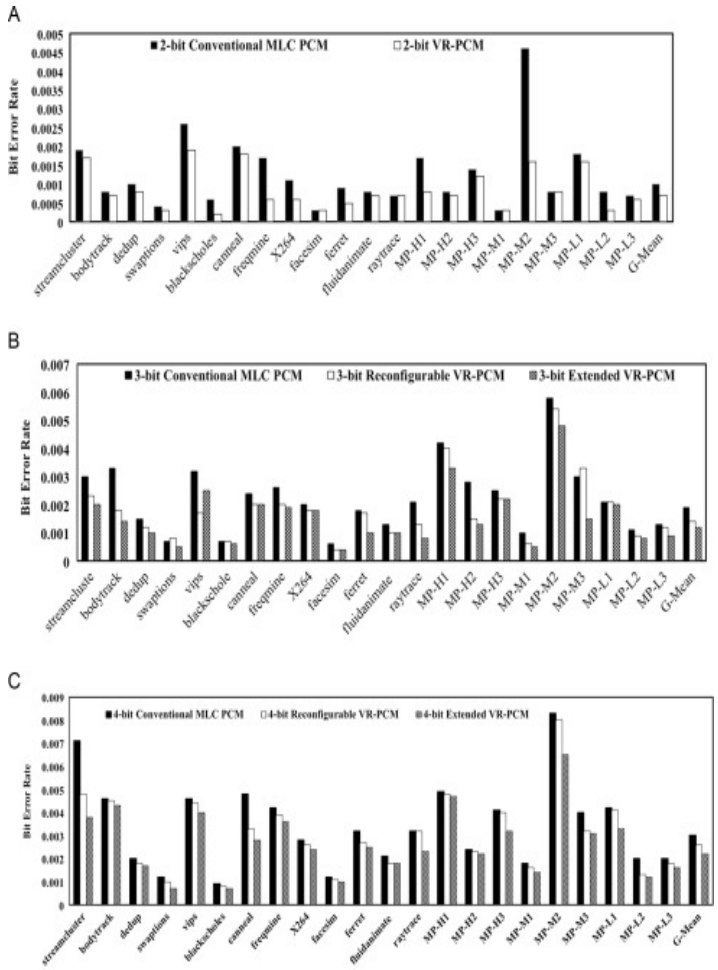

Fig. 8. Rate of soft error (in terms of bit error rate) for VR-PCM compared to conventional MLC PCM design. These charts along with Table 1 confirm that VR-PCM gives same level of soft-error reliability with average of 18% reduction in MLC PCM write energy.

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Device- and Circuit-Level Modeling, Measurement, and Mitigation

In Architecture Design for Soft Errors, 2008

2.2.1 Impact of Alpha Particle or Neutron on Circuit Elements

An alpha particle or a neutron strike typically manifests itself as a transient disturbance that would usually last less than 100 picoseconds. If this charge disturbance is smaller than the noise margin, the circuit will continue to operate correctly. Otherwise, the disturbed voltage may invert the logic state.

Let us examine an SRAM cell to understand this phenomenon better (see Rabaey et al. [21], for more detail on SRAM cell design). Figure 2.1 shows an SRAM cell made of a pair of cross-coupled inverters. When the wordline is low, the cell holds data in the cross-coupled inverters and the bitlines are decoupled. If a particle strike causes one of the sensitive nodes to transition, then the disturbance may propagate through the inverter and cause a transient disturbance on the second

sensitive node. This will cause the second node to propagate the incorrect value, thereby causing both nodes to flip. This results in flipping the state of the bit held in the SRAM cell. Radiation-hardened cell design—described later in this chapter—is one way to correct such bit flips using a regenerative circuit.

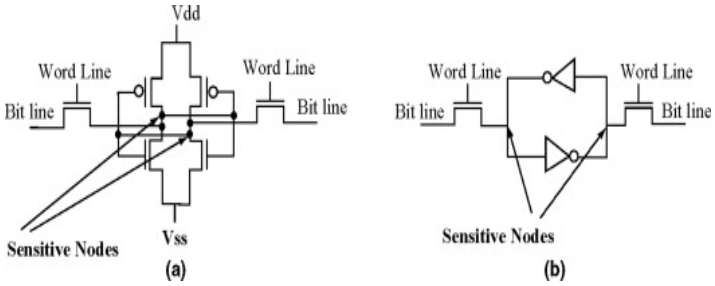

FIGURE 2.1. Nodes in an SRAM cell most sensitive to an alpha or a neutron strike. (a) A transistor-level diagram. (b) The same figure at a logic level, in which the two cross-coupled inverters represent the memory element. The bitlines are complements of each other, whereas the wordlines are the same for both.

An SRAM cell can also encounter a soft error when the wordline is high and the data are being read out through the bitlines. The voltage differential, which is used to sense if the cell holds a value “0” or a “1,” can be disturbed causing a corrupted value to be read out.

Other circuit elements, such as DRAM cells, register file cells, latches, static logic gates, and dynamic logic gates, are affected in similar ways by particle strikes. The size of these cells, number of ports, nature of their operation, etc. affect the degree to which a particle strike can introduce a disturbance in each circuit's operation. The next section explains how to reason about the rate at which a particle strike will introduce a sufficiently large disturbance to cause a circuit element to malfunction.

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Choosing a means of implementation

John Crowe, Barrie Hayes-Gill, in Introduction to Digital Electronics, 1998

Example 9.16

Two inverters from a 74LS04 hex inverter IC (i.e. six inverters in one package) are connected in series such that one inverter is driving the other. From Table 9.1 determine the high and low noise margins.

Solution

$$NM_{\mathrm{H}} = V_{\mathrm{OHmin}} - V_{\mathrm{IHmin}} = 2.7 - 2.0 = 0.7\mathrm{V}$$
$$NM_{\mathrm{L}} = V_{\mathrm{ILmax}} - V_{\mathrm{OLmax}} = 0.8 - 0.5 = 0.3\mathrm{V}$$

Example 9.17

Repeat 9.16 for a 74HCT04 (CMOS version of 74LS04).

Solution

$$NM_{\mathrm{H}} = V_{\mathrm{OHmin}} - V_{\mathrm{IHmin}} = 4.3 - 2.0 = 2.3\mathrm{V}$$
$$NM_{\mathrm{L}} = V_{\mathrm{ILmax}} - V_{\mathrm{OLmax}} = 0.8 - 0.33 = 0.47\mathrm{V}$$

Hence an improved noise margin is obtained with CMOS. It should be noted, however, that since the CMOS output is driving another CMOS device then the current drawn from the output is small. Hence the output voltage levels for a CMOS device will be much closer to the supply than indicated in Table 9.1 resulting in an even larger noise margin.

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