Abstract

In this experiment, we have learnt to use the Cadence virtuoso software. We have simulated MOS transitor to get its I-V characteristics. We also have determined threshold voltage for MOS transistor. We have used different design corners TT, FF, FS & SS and observed the differences in their performances.

Keywords

1. I-V Characteristics of MOS
2. Virtuoso
3. Threshold Voltage
4. gpdk090
5. Subthreshold Current

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1 Introduction

This experiment has been designed to make us introduced to the Cadence software. We created a new directory in the Cadence Server and used the Cadence virtuoso software to simulate the I-V characteristics of MOS transistor using the generic PDK 90nm process.

We have analyzed the current-voltage relationship of MOS in different design corner (SS, TT, FF & FS). We also found the threshold voltages for differnt MOS design. Non-linear effects such as channel length modulation and subthreshold current have also been observrd.

These observations are very useful in designing practical circuits.

2 Theory

2.1 MOSFETs

The metal-oxidesemiconductor field-effect transistor (MOSFET) is a transistor used for amplifying or switching electronic signals. In MOSFETs, a voltage on the oxide-insulated gate electrode can induce a conducting channel between the two other contacts called source and drain. The channel can be of n-type or p-type and is accordingly called an nMOSFET or a pMOSFET (also commonly nMOS, pMOS). It is by far the most common transistor in both digital and analog circuits

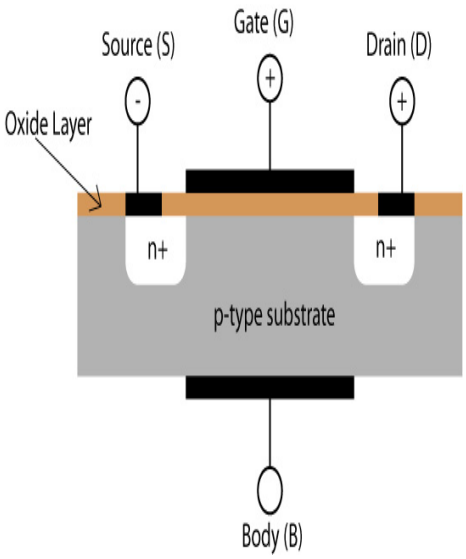

Figure 1: Schematic of a MOS structure

2.2 I-V characteristics

Any MOS transistor has three regions of operation depending upon the terminal voltages :

1. Cutoff or subthreshold region ($V_{GS} < V_{th}$)
2. Triode mode or linear region $\Big(V_{GS} > V_{th}$ and $V_{DS} < (V_{GS} - V_{th})\Big)$
3. Saturation or active mode $\Big(V_{GS} > V_{th}$ and $V_{DS} > (V_{GS} - V_{th})\Big)$

2.2.1 Cutoff or subthreshold region

When $V_{GS} < V_{th}$ the MOS is in cutoff region. Ideally there will be no current flow. But practically a small subthreshold current is found which will increase exponentially with drain to source voltage.

2.2.2 Triode mode or linear region

When $V_{GS} > V_{th}$ and $V_{DS} < (V_{GS} - V_{th})$ the MOS is in triode or linear region. The drain current in this region can be modeled as:

$$I_{Dlin} = \mu_n C_{ox} \frac{W}{L}\Big((V_{GS} - V_{th})^2 V_{DS} - \frac{1}{2}V_{DS}^2\Big) \tag{1}$$

2.2.3 Saturation or active region

When $V_{GS} > V_{th}$ and $V_{DS} > (V_{GS} - V_{th})$ the MOS is in Saturation or active region. The drain current in this region can be modeled as:

$$I_{Dsat} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})^2 \tag{2}$$

The characteristics curve is shown in figure 2 at page 7

2.3 Threshold voltage

To determine the threshold voltage we have to plot the $\sqrt{I_D}$ vs. V_{GS} curve and determine the x-axis intercept of the curve while maintaining $V_{GS} = V_{DS}$ as shown in figure 3 at page 7.

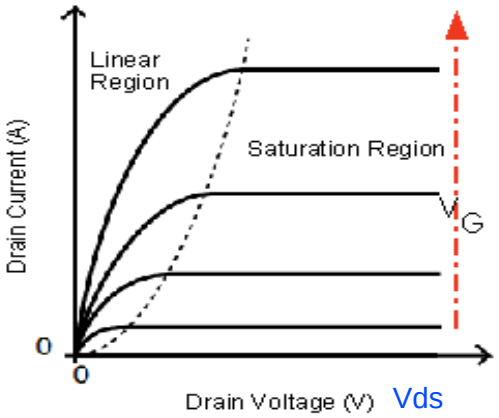

Figure 2: MOS IV characteristics

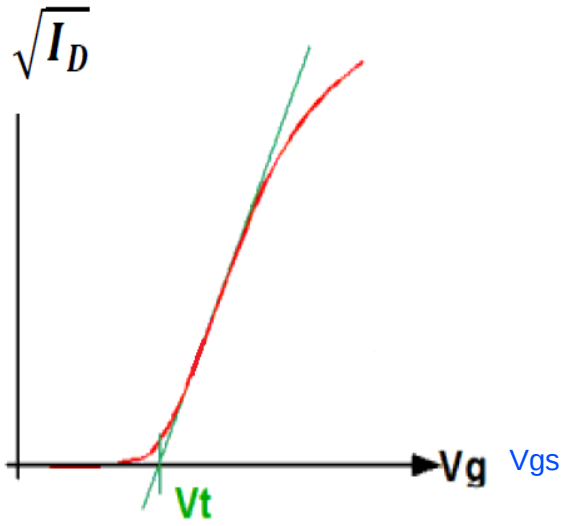

Figure 3: Determination of Threshold Voltage

3 Lab Handout Question

Question: Observe the BSIM3v3 MOS models of the different MOS transistors available in the gpdk090 technology library and try to understand the meaning of different parameters. In a table summarize the values of the critical parameters for different types of MOS transistors.

Parameter	Description	Default value	unit
t_{ox}	Gate oxide thickness	150×10^{-10}	m
X_j	Junction depth	0.15×10^{-6}	m
N_{gate}	Polygate doping concentration	0	cm^{-3}
V_{th0}	Threshold at $V_{SB} = 0$ and small V_{DS}	0.7 NMOS, −0.7 PMOS	V
N_{sub}	Substrate doping concentration	6×10^{16}	cm^{-3}
x_t	Doping depth	1.55×10^{-7}	m
θ	Drain induced barrier lowering coeff.	0.02	V^{-1}
t_{nom}	Parameters measurement temperature	-	C
pclm	Carrier saturation velocity at t_{nom}	9.58×10^4	m
v_{sat}	Channel length modulation coeff.	1.3	-
r_s	Source resistance	0	Ω
c_{gdo}	Gate-drain overlap capacitance	-	F/m
c_j	Zero-bias junction bottom capacitance density	5×10^{-4}	F/m
c_{jsw}	Zero-bias junction sidewall capacitance density	5×10^{-10}	F/m

Table 1: Critical parameters for different types of MOS transistors

4 Procedure

- Created a new directory to make a new design
- Added the gpdk090 library to this library path
- Used *Cadence virtuoso* to create a cellview named *'MOS_IV'*
- Used dc analysis and parametric sweep to vary two variables at a time
- Created Netlist and ran Simulation using Spectre

The schematic of the circuit is shown in figure 4 at page 9

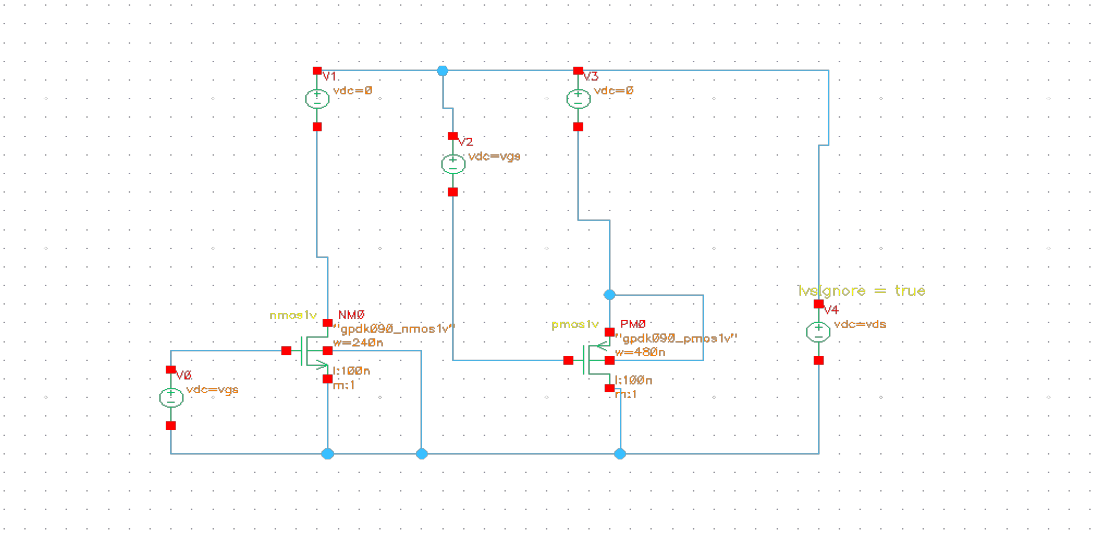

Figure 4: Schematic of simulation

5 Results

5.1 I-V Characteristics for *NMOS1V* & *PMOS1V*

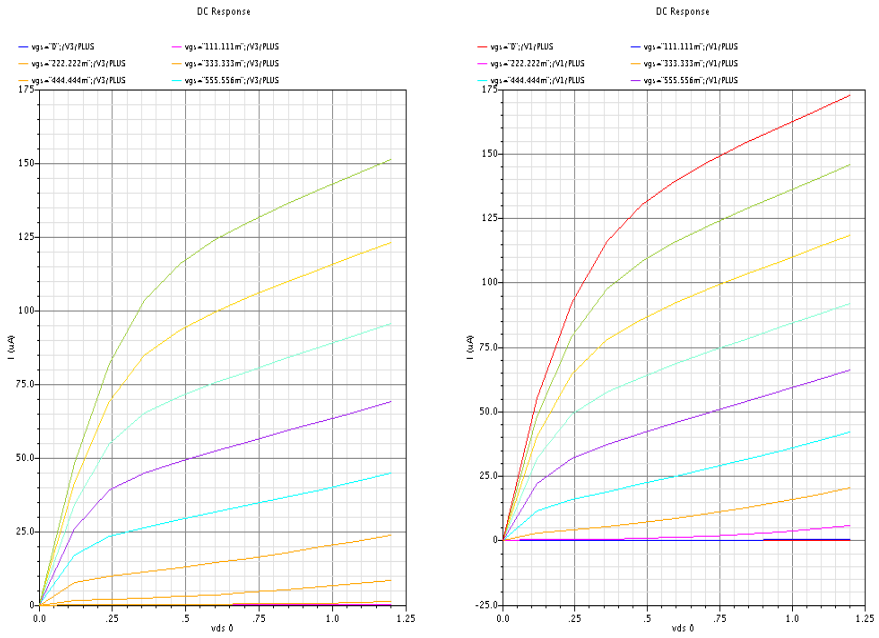

Figure 5: I-V Characteristics for the TT corner *NMOS1V* & *PMOS1V*

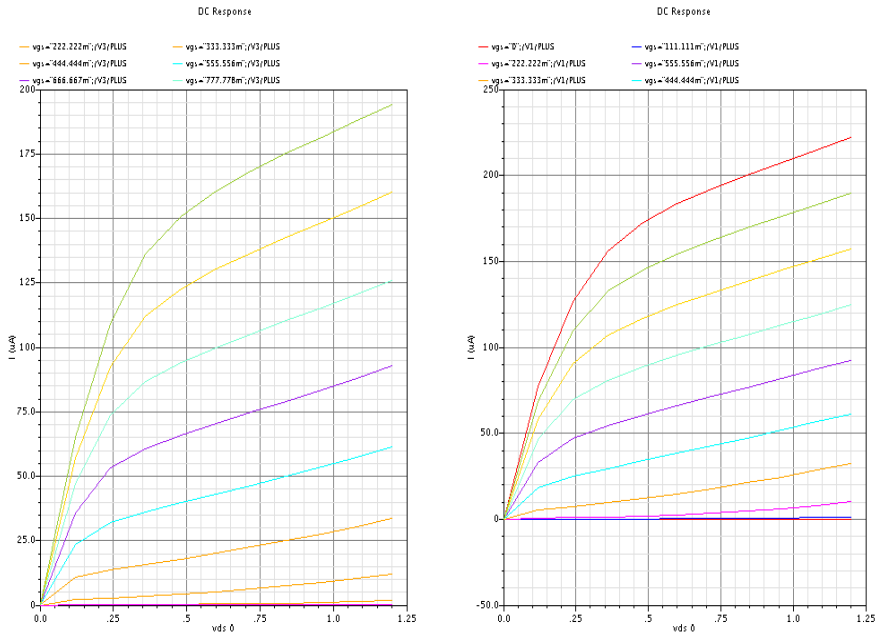

Figure 6: I-V Characteristics for the FF corner *NMOS1V* & *PMOS1V*

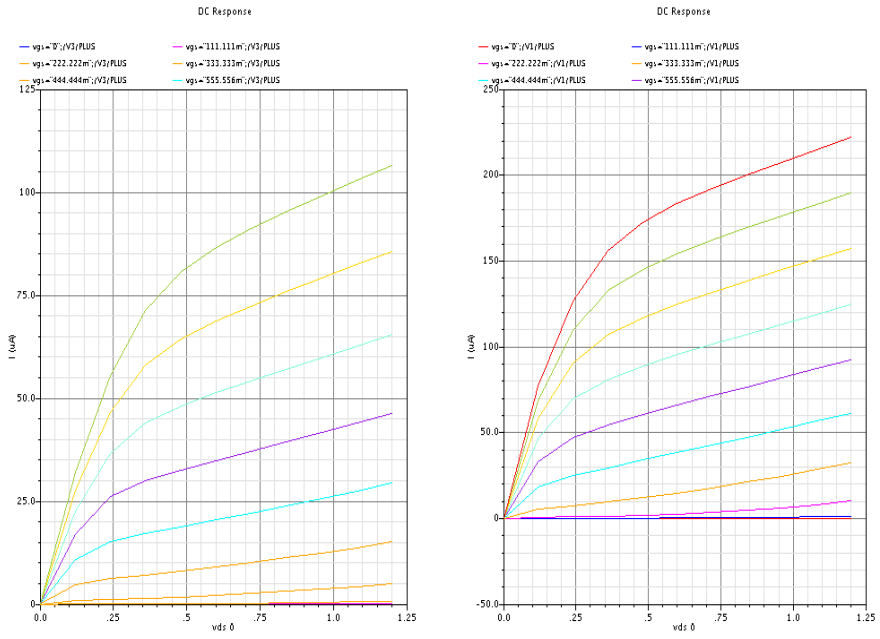

Figure 7: I-V Characteristics for the FS corner *NMOS1V* & *PMOS1V*

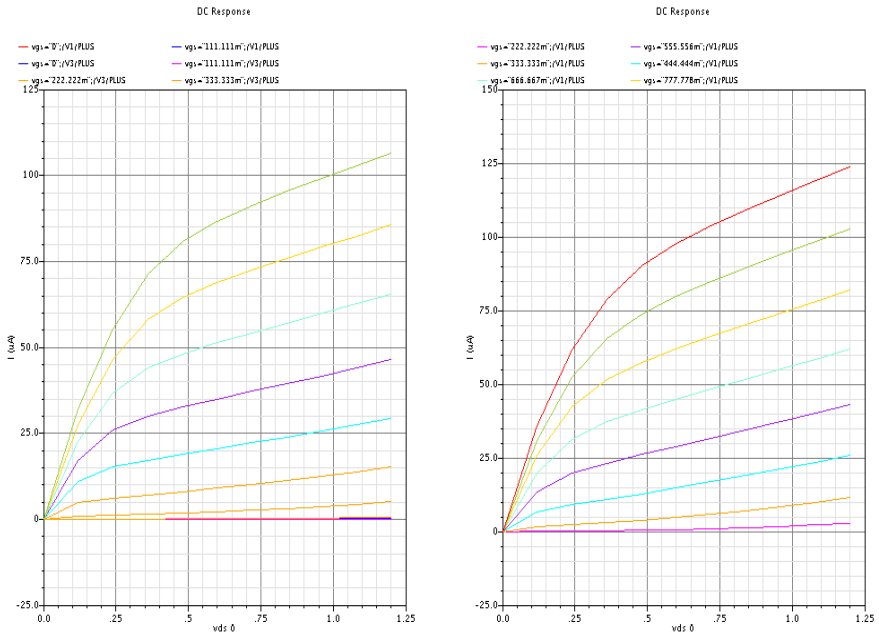

Figure 8: I-V Characteristics for the SS corner *NMOS1V* & *PMOS1V*

5.2 I-V Characteristics for *NMOS2V* & *PMOS2V*

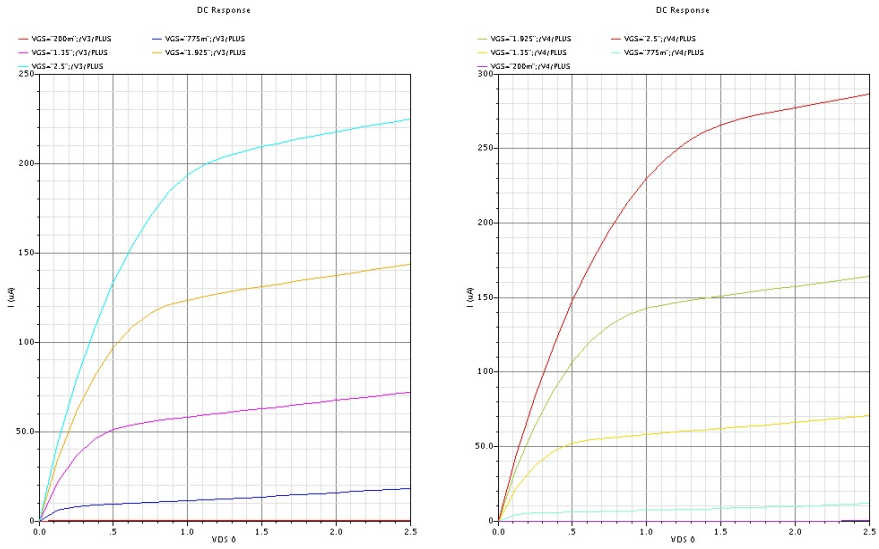

Figure 9: I-V Characteristics for the FF corner *NMOS2V* & *PMOS2V*

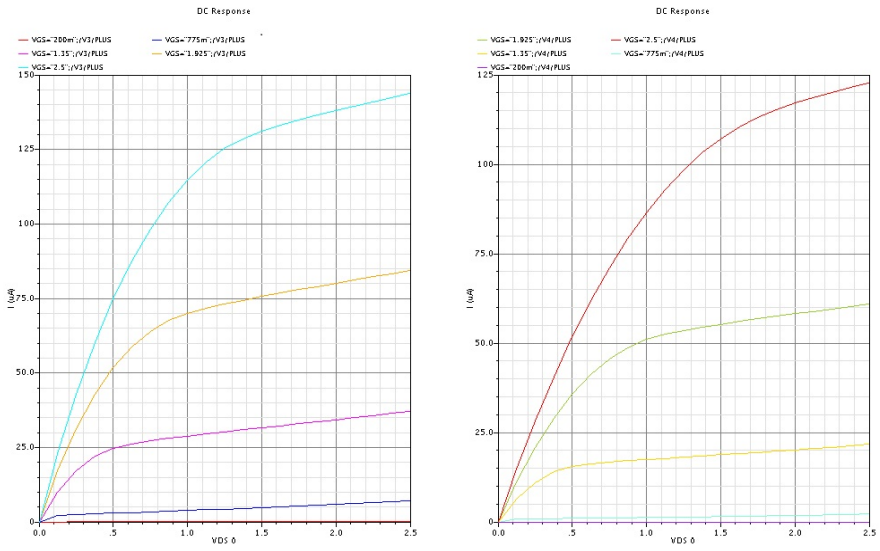

Figure 10: I-V Characteristics for the SS corner *NMOS*2*V* & *PMOS*2*V*

5.3 Threshold voltage determination for *NMOS*1*V*

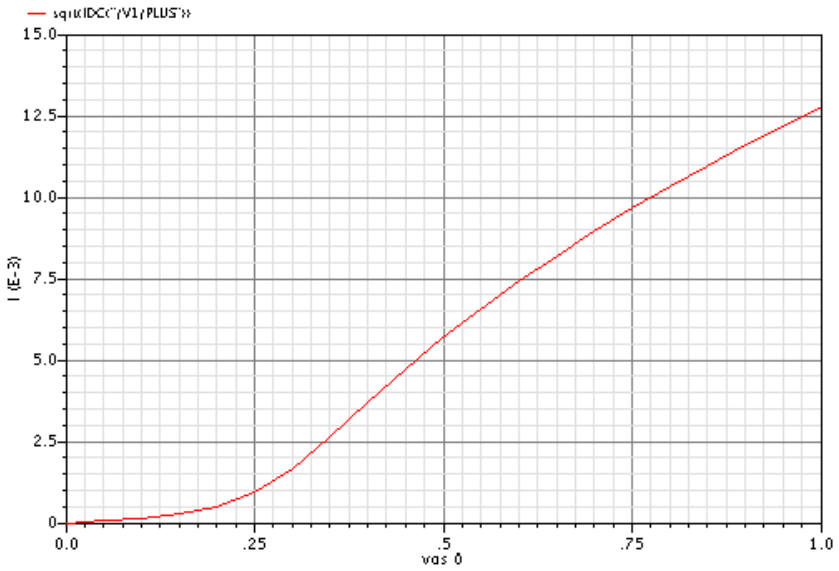

Figure 11: Threshold voltage for the TT corner *NMOS*1*V*

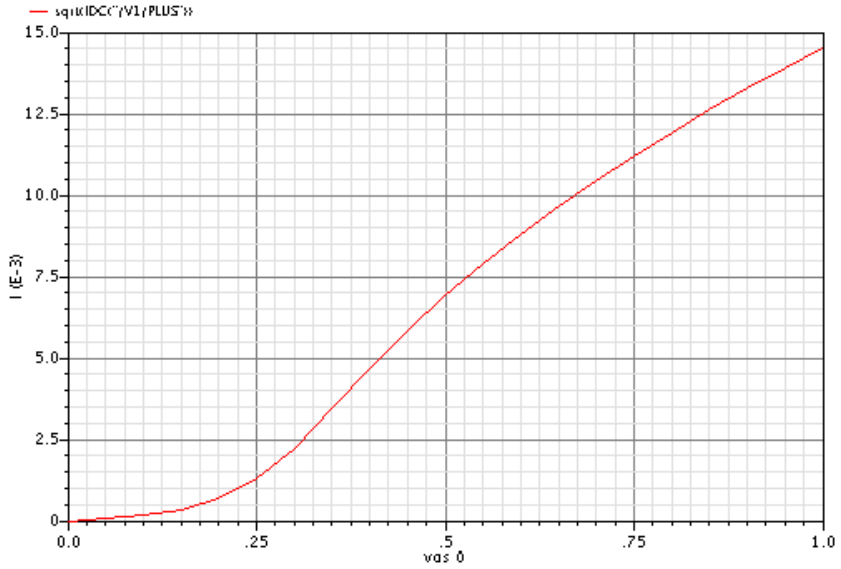

Figure 12: Threshold voltage for the FF corner *NMOS1V*

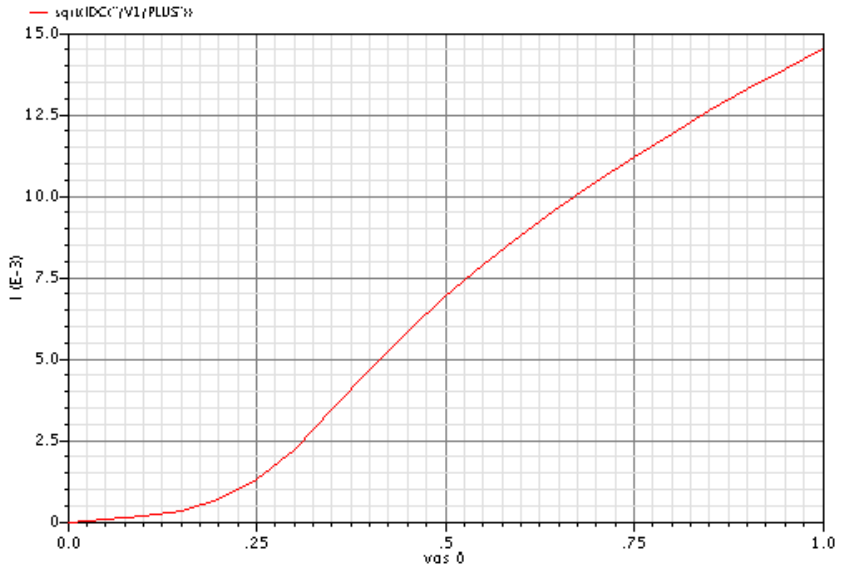

Figure 13: Threshold voltage for the FS corner *NMOS1V*

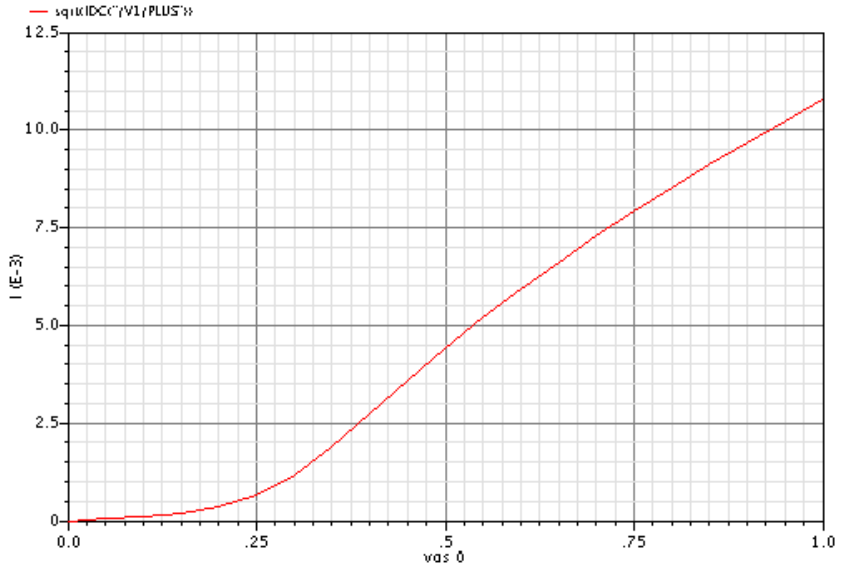

Figure 14: Threshold voltage for the SS corner *NMOS1V*

5.4 Threshold voltage determination for *NMOS2V*

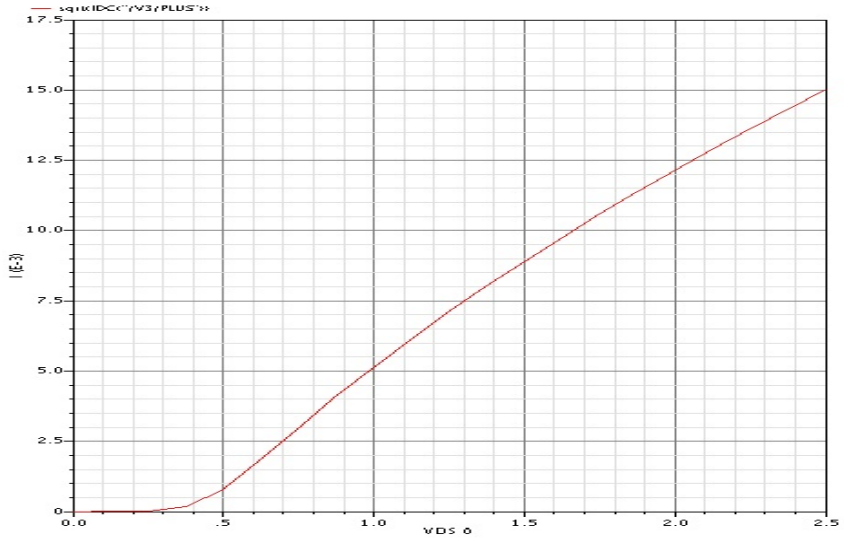

Figure 15: Threshold voltage for the FF corner *NMOS2V*

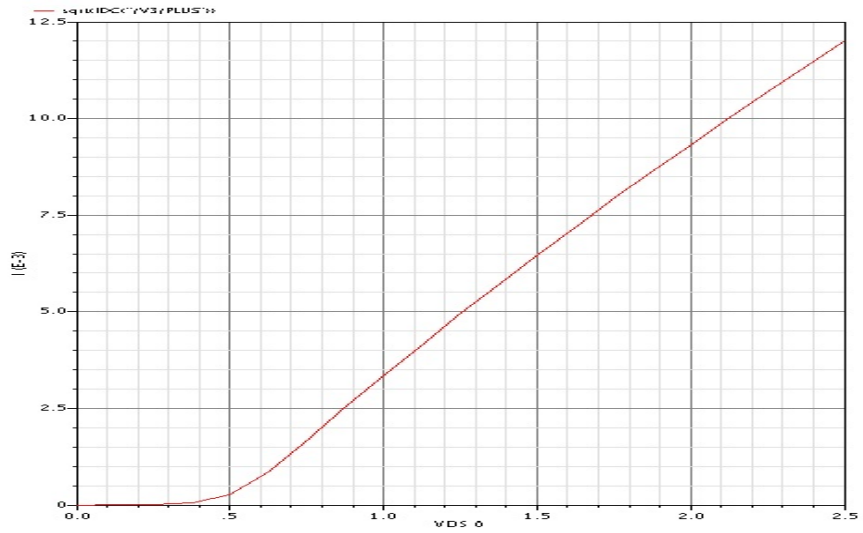

Figure 16: Threshold voltage for the SS corner *NMOS2V*

MOS Model	Design Corner	Threshold voltage(in V)
NMOS1V	*TT*	0.2
NMOS1V	*FF*	0.2
NMOS1V	*FS*	0.2
NMOS1V	*SS*	0.2
NMOS2V	*FF*	0.45
NMOS2V	*SS*	0.45

Table 2: Threshold voltages for different types of MOS

6 Conclusion

It is found that current increases with the speed of the transistor models. Saturation drain current (I_{Dsat}) is maximum for FF (Fast-Fast) design corner and minimum for SS (Slow-Slow) design corner.

But the threshold voltages do not change significantly with the variation in design corners. To find the threshold voltage we had to extrapolate the linear portion of the $\sqrt{I_D}$ vs. V_{GS} curve to get the x-axis intercept as there was sub-threshold conduction.

For the high nominal voltage MOS transistors (*nmos*2*v* and *pmos*2*v*) the current and threshold voltages ate greater than those of lower nominal voltage MOS transistors (*nmos*1*v* and *pmos*1*v*).

References

[1] Neil H. E. Weste, David Harris and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective," Third Edition, Chapter 2, Section 2, Pearson Education, 2005

[2] Robert F. Pierret, "Semiconductor Device Fundamentals," First Edition, Part 3, Chapter 17, Section 2, Pearson Education, 2006