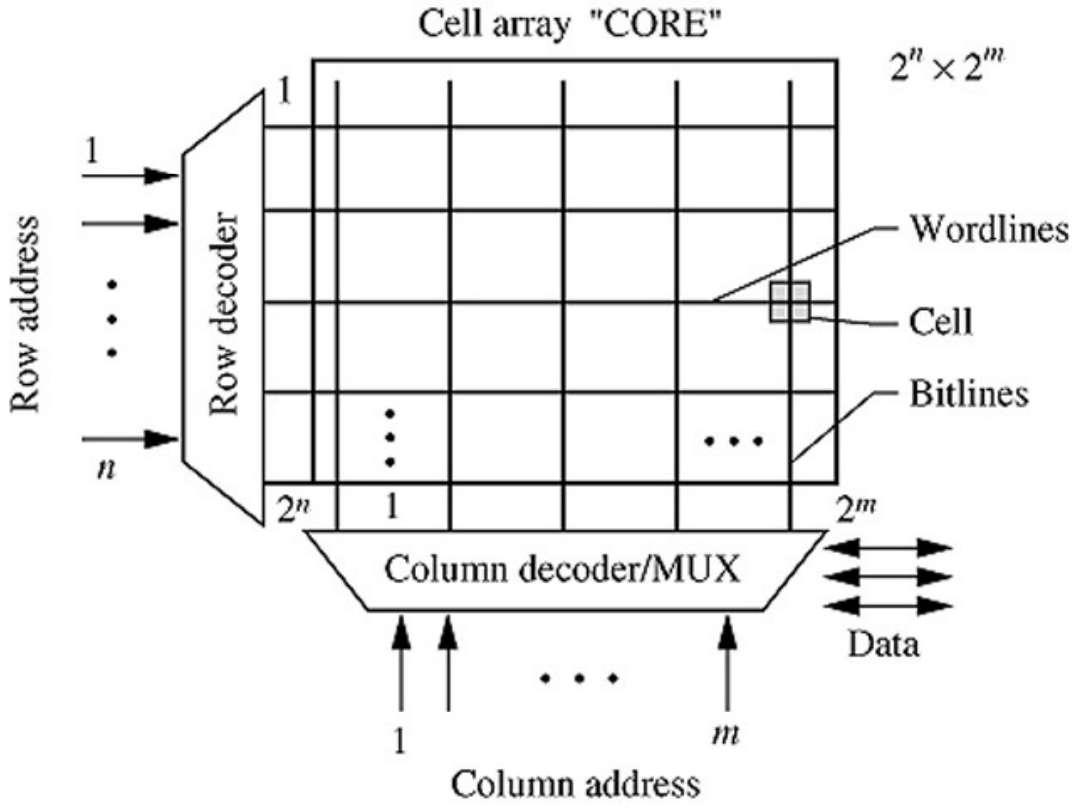
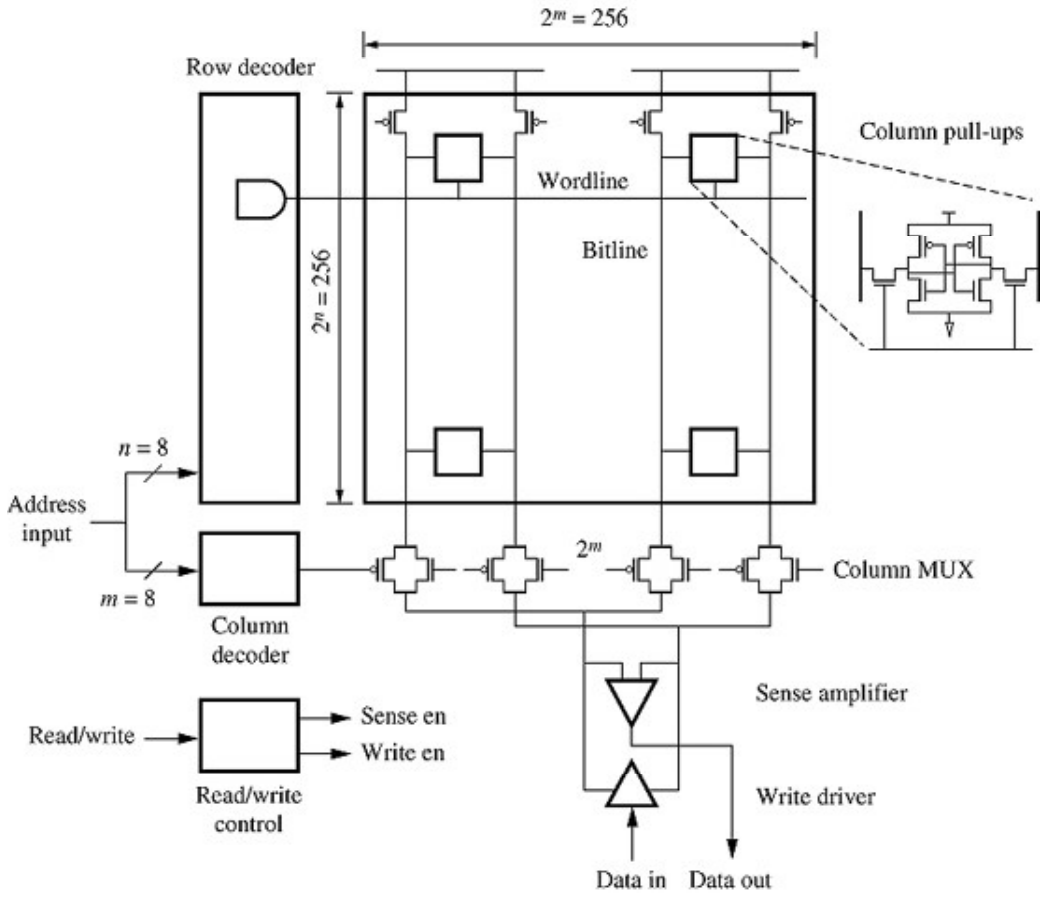
Memory organization

- Random access
- Wordline, bitline, cell



Architecture of memory design

- N-bit decoder for X and Y
- Peripheral circuits



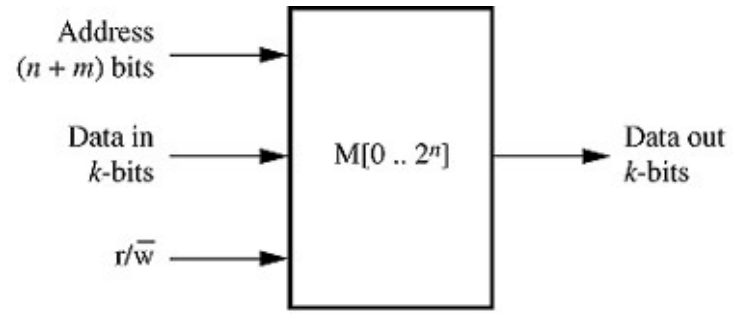
Types of memory

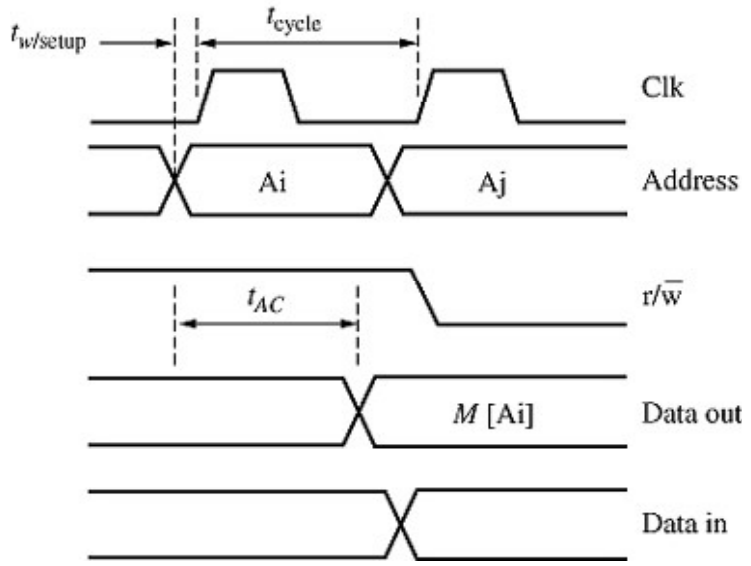
- Random-access memory (RAM)
- SRAM and DRAM

- Read-only memory (ROM), nonvolatile memory
- Mask-programmed ROM
- Programmable ROM
- Erasable programmable ROM
- Flash memory
- Ferroelectric RAM (FRAM)

Memory timing

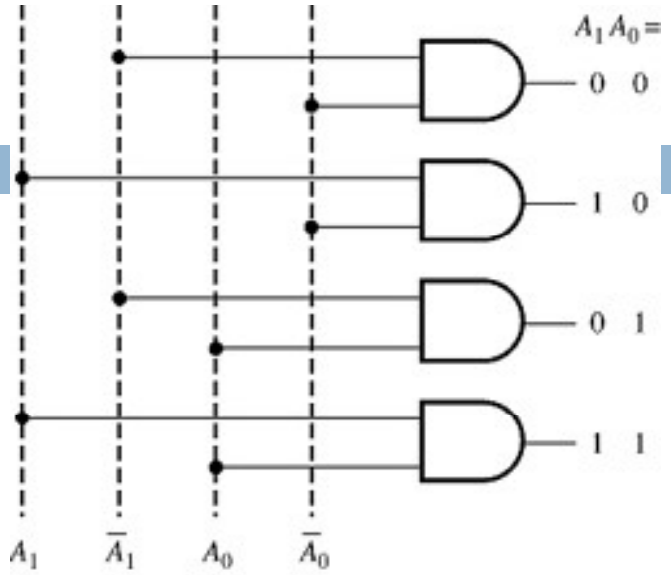
- Read access time (tac)
- Cycle time (tcycle)
- Set-up time (tset-up)



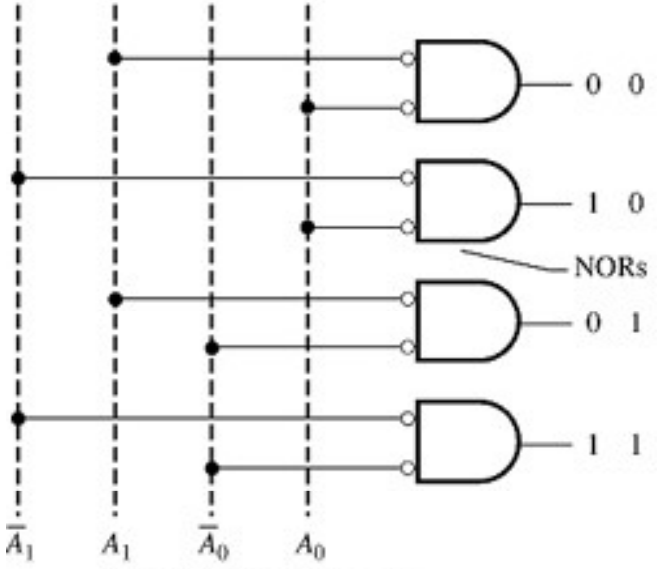


Decoders

- Nand or nor can be used
- Cascaded gate is more general than n-input gate
- Pre-decoding and main-decoding

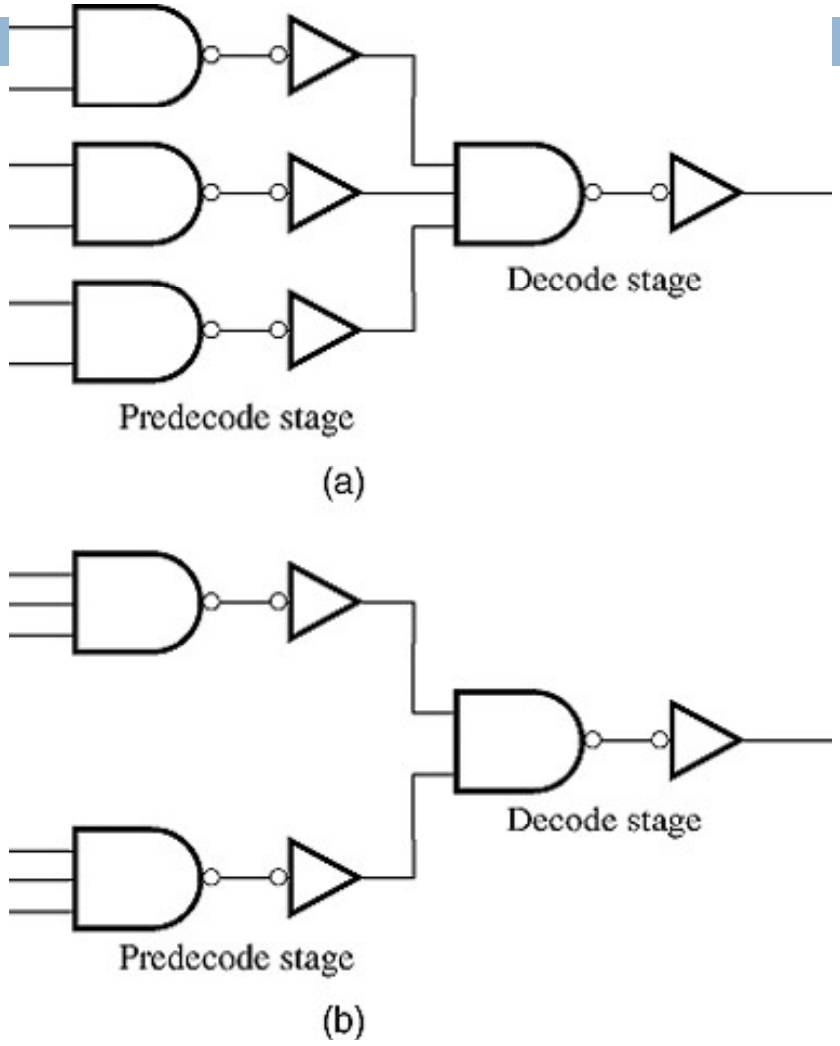


(a) AND-based decoder



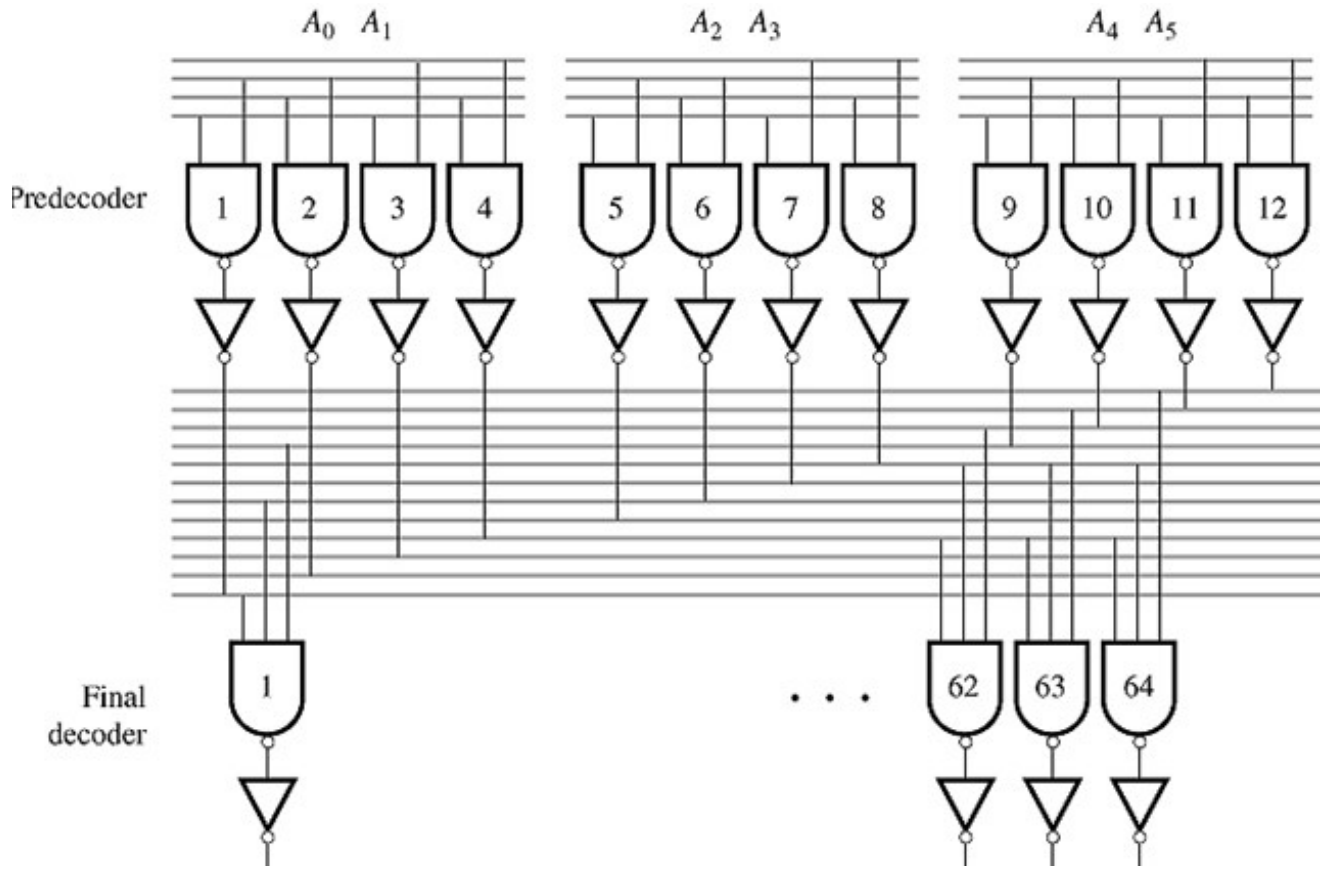
(b) NOR-based decoder

Predecoder configurations

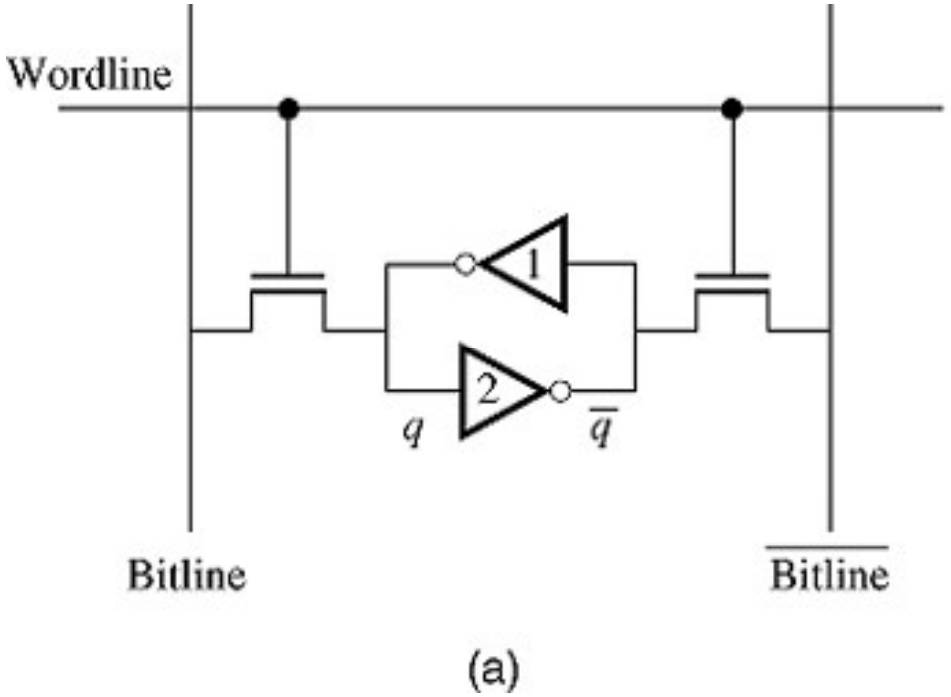


Structure of two-level decoder

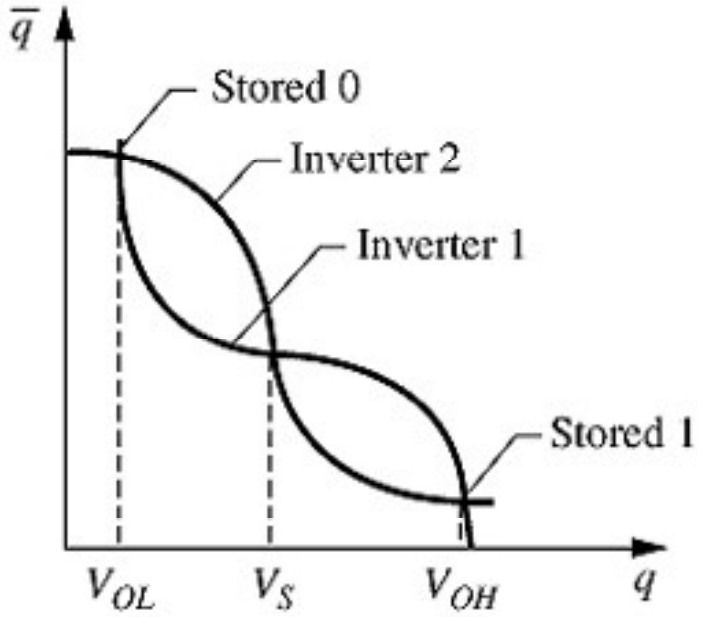
- 6-bit address



Static RAM cell

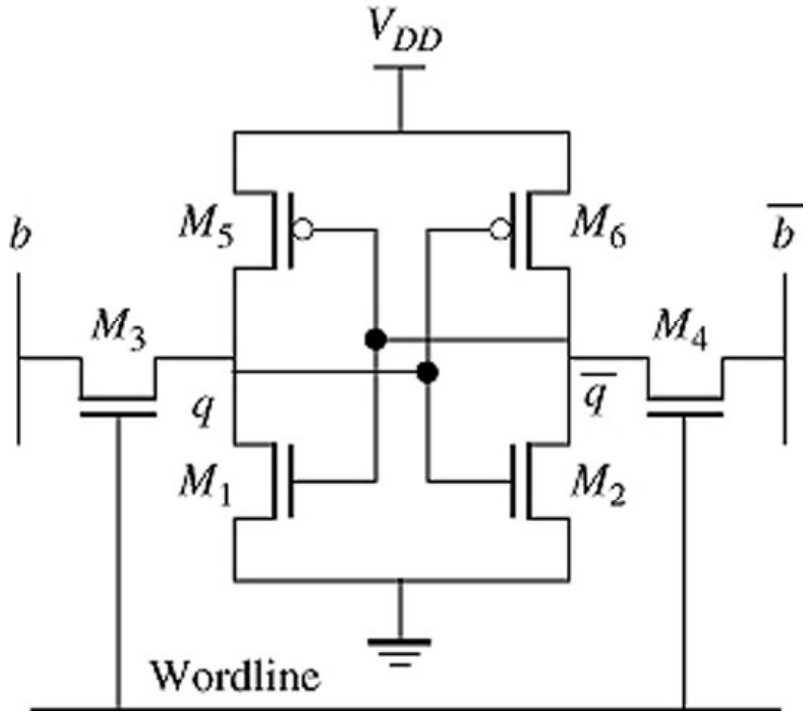


(a)



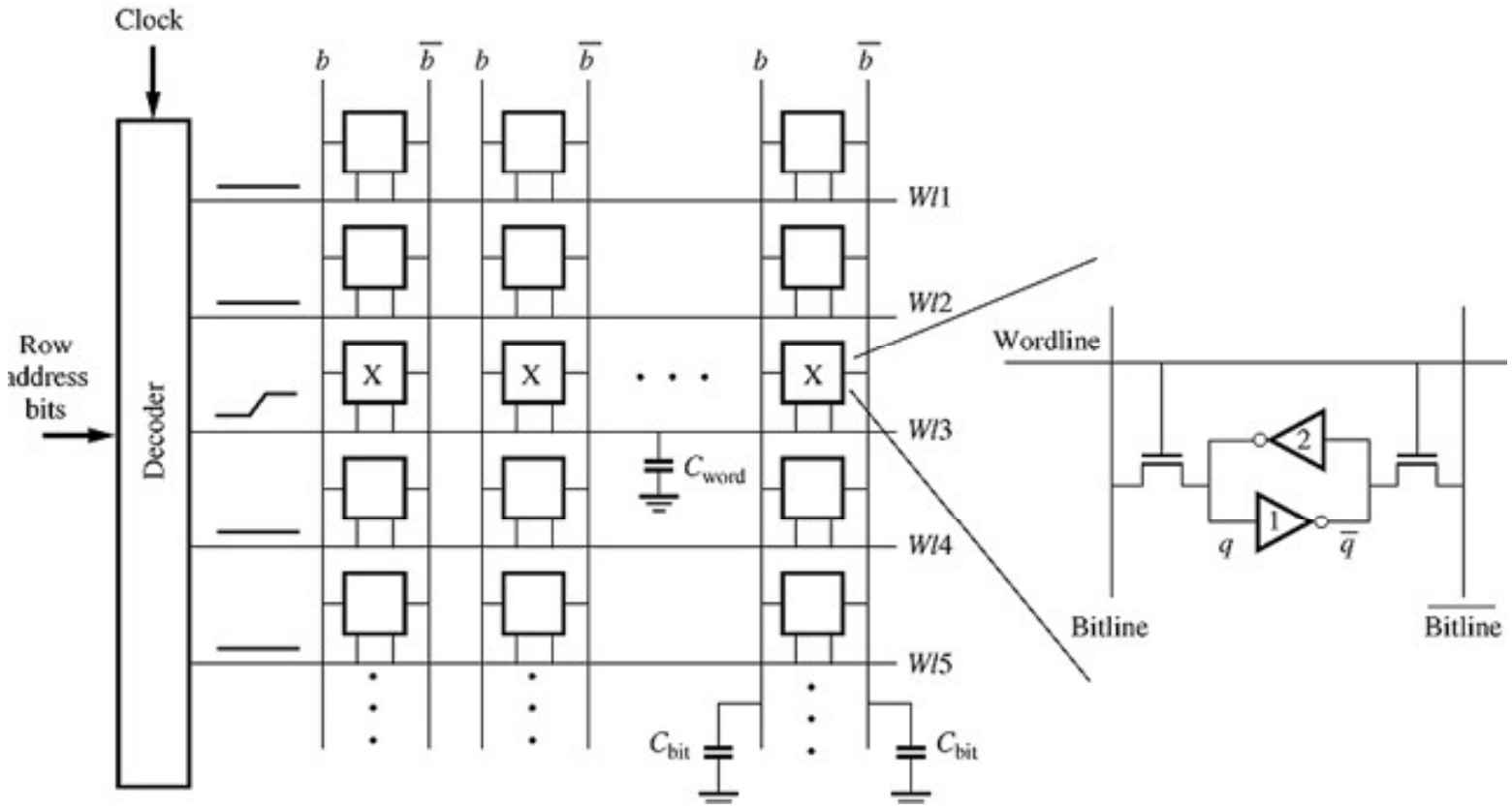
(b)

6 transistor SRAM cell



Wordline and bitline configuration

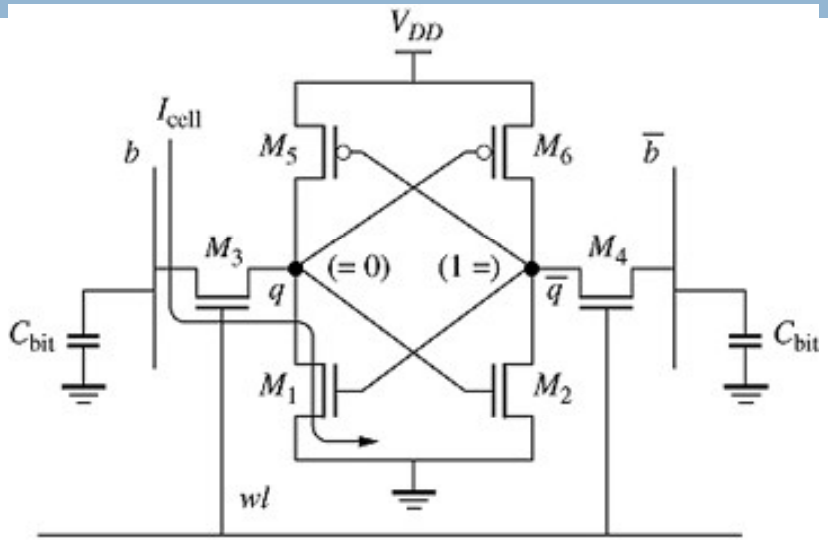
Cword=(2*gate cap+wire cap) * # of cells in row
Cbit = (source/drain cap+wire cap+contact cap) * # of cells in column



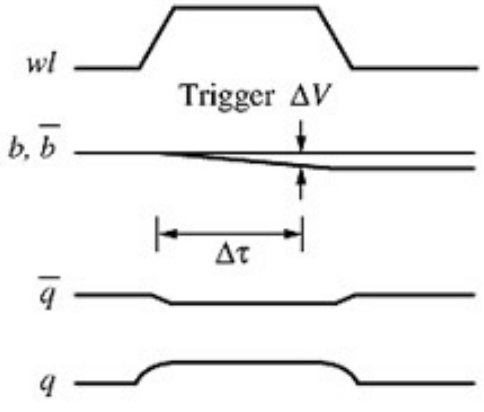
Read operation

W1/W3=1.5

Think of tradeoff between M3 and M1



(a)

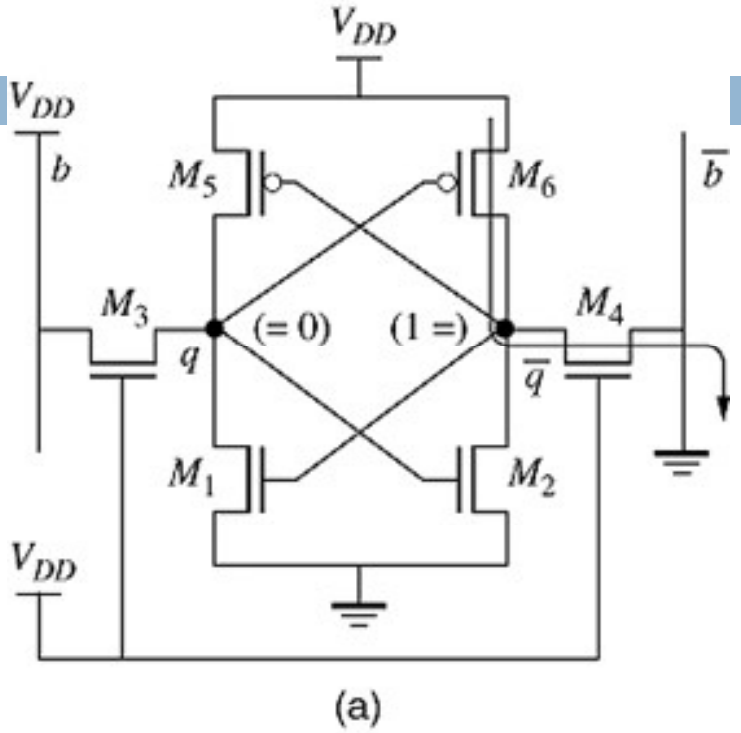


(b)

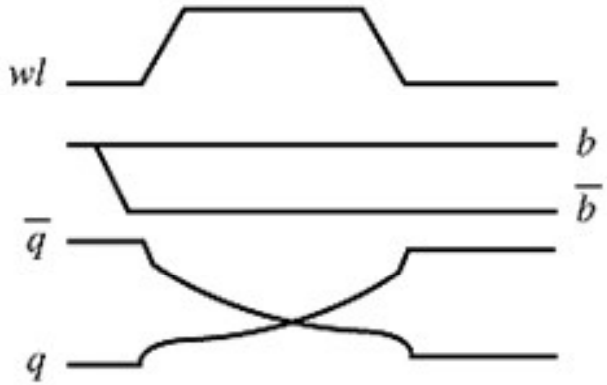
Write operation

W4/W6=1.5

Think of tradeoff between M4 and M6

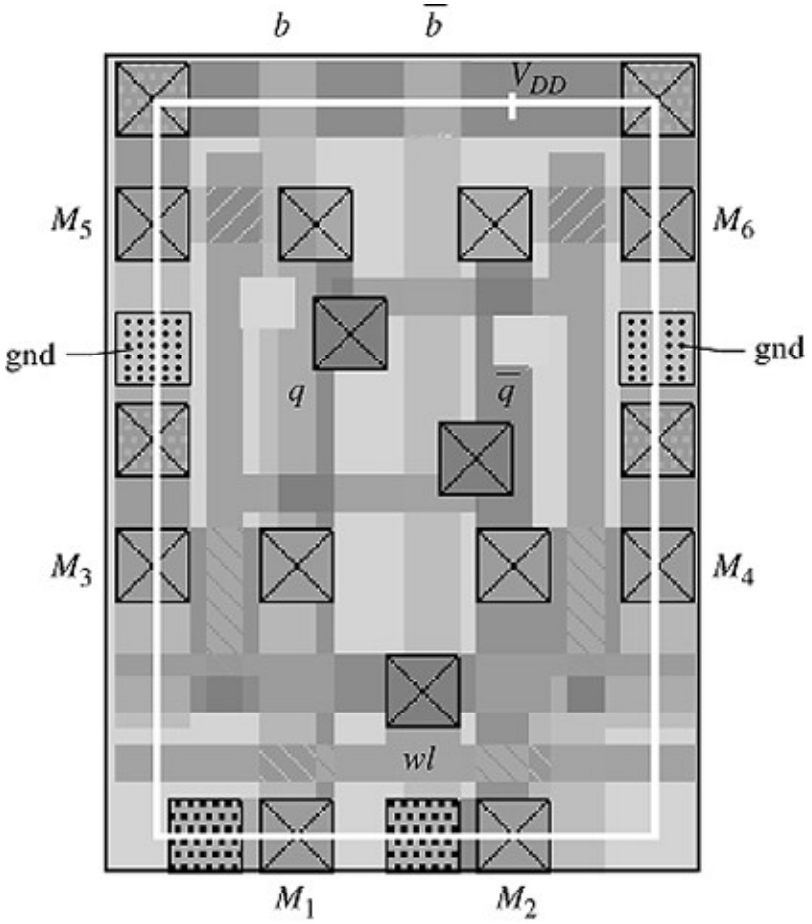


(a)

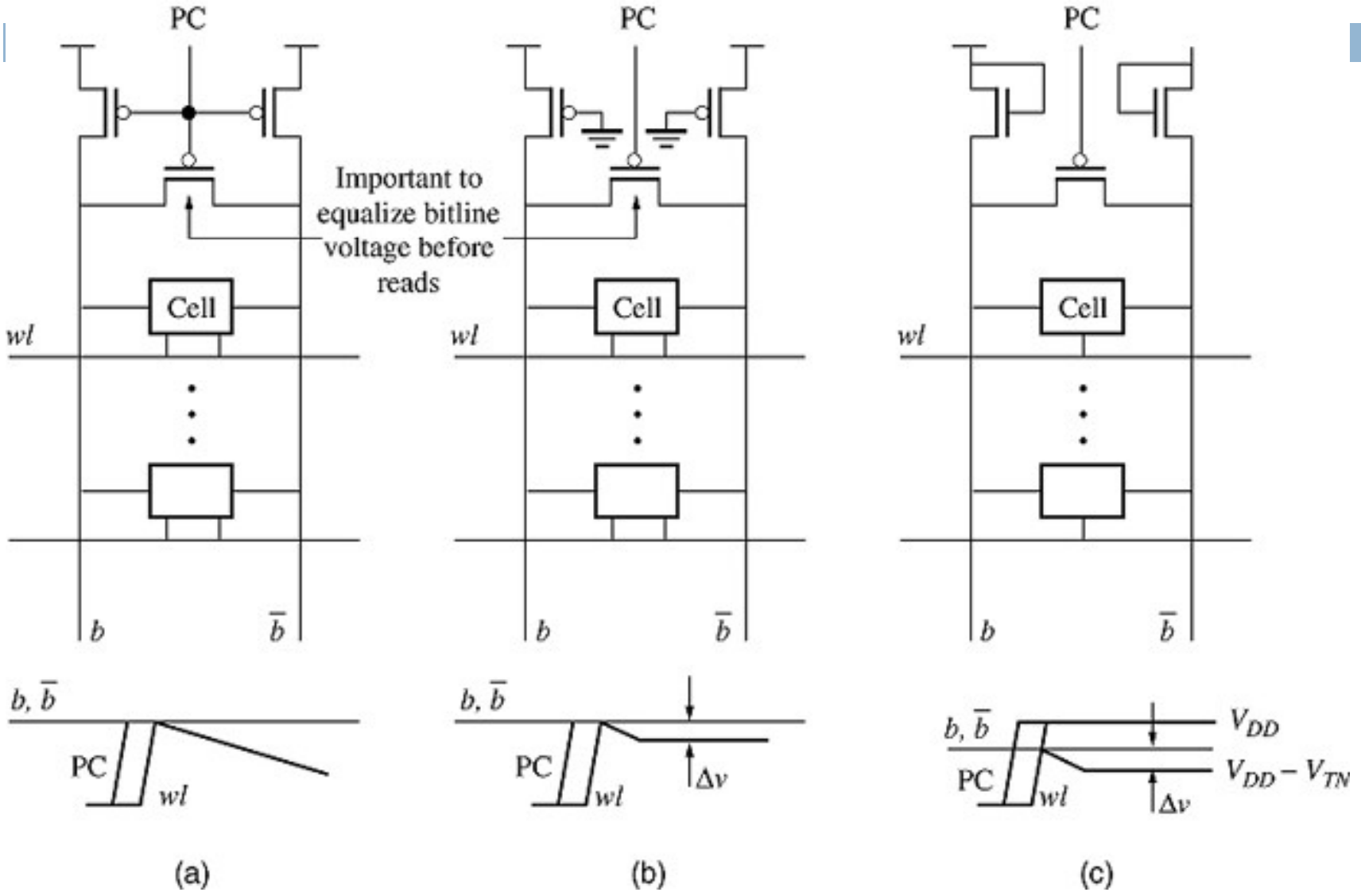


(b)

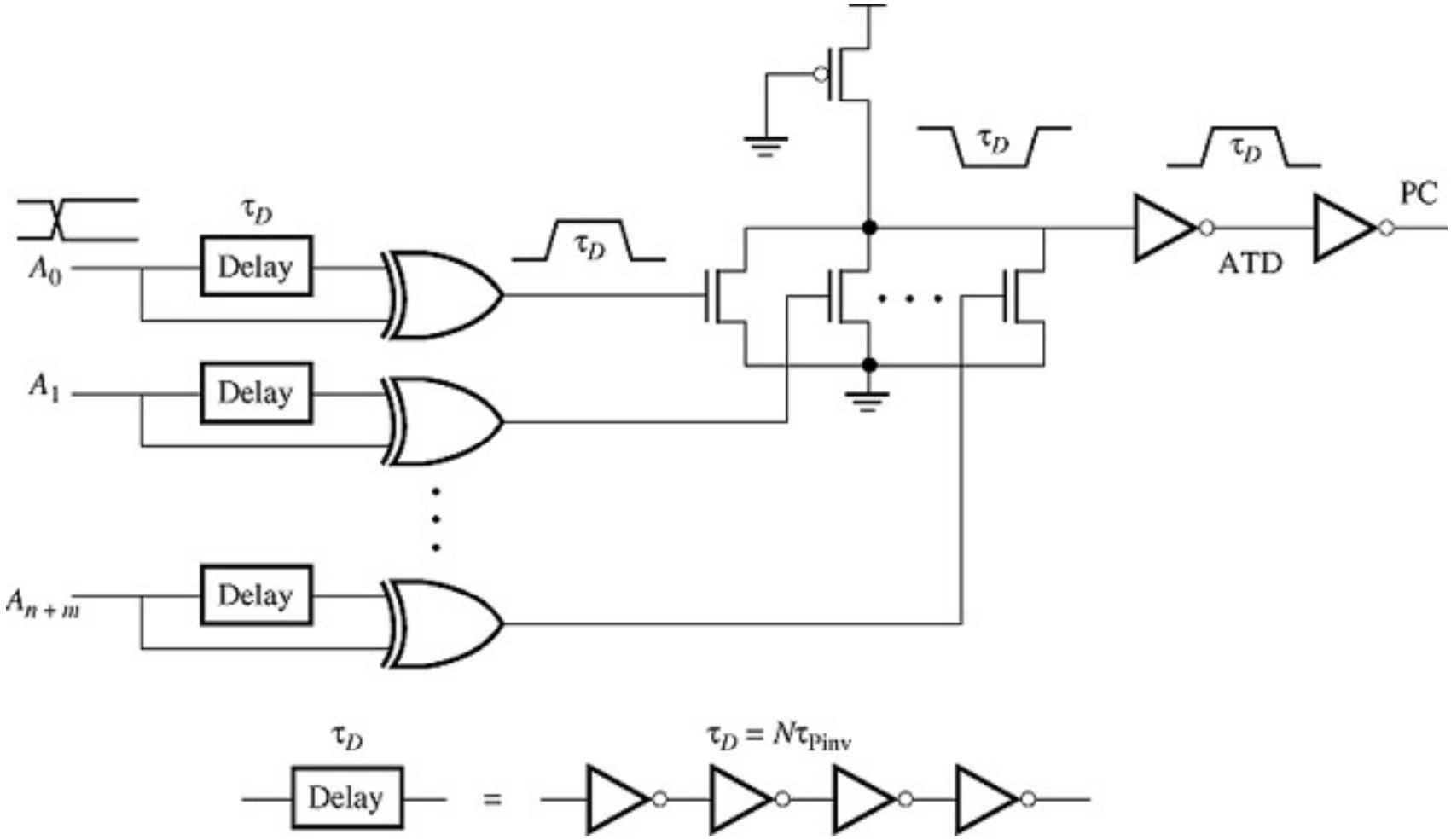
Cell layout



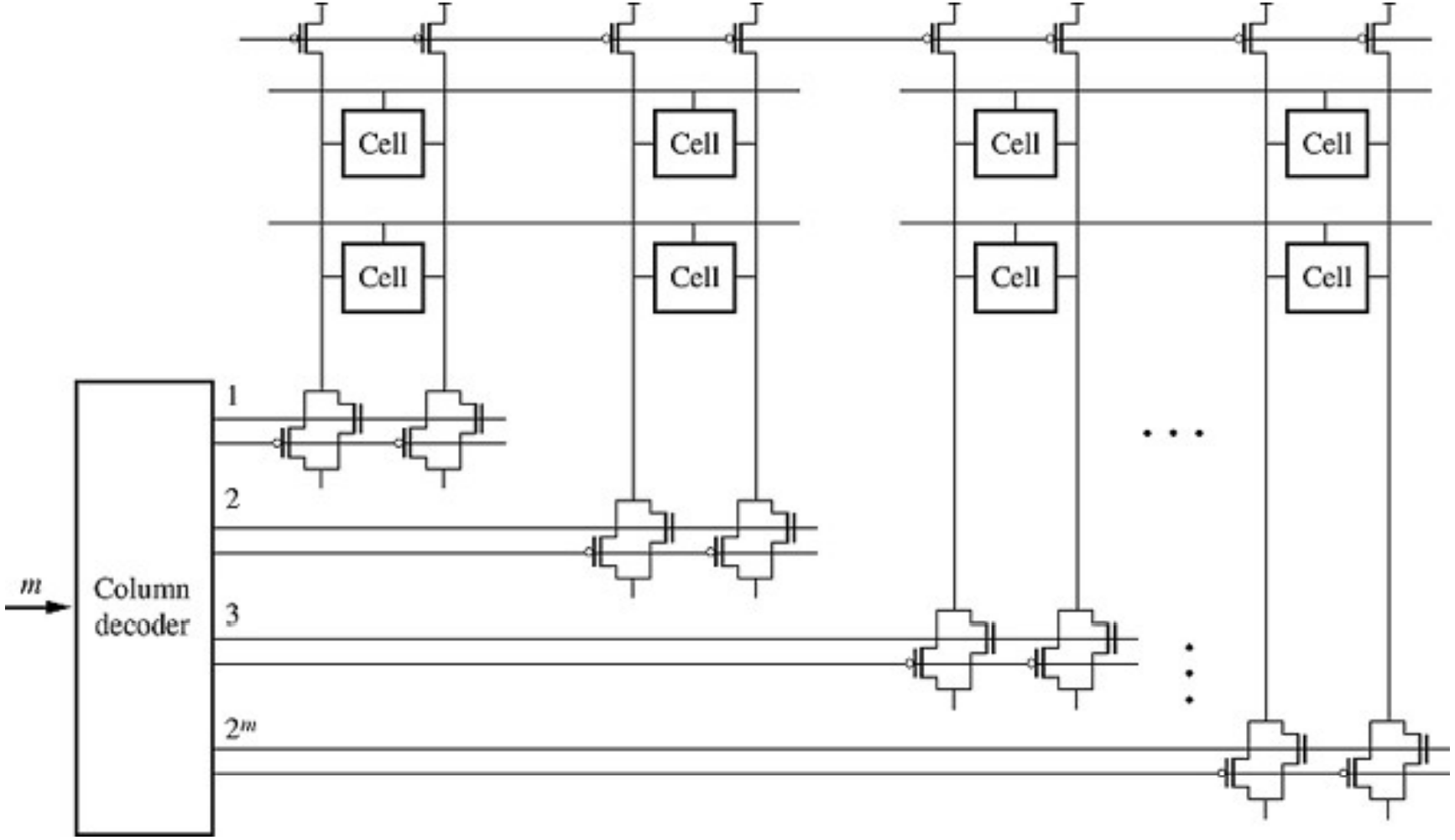
Column pull-up configurations



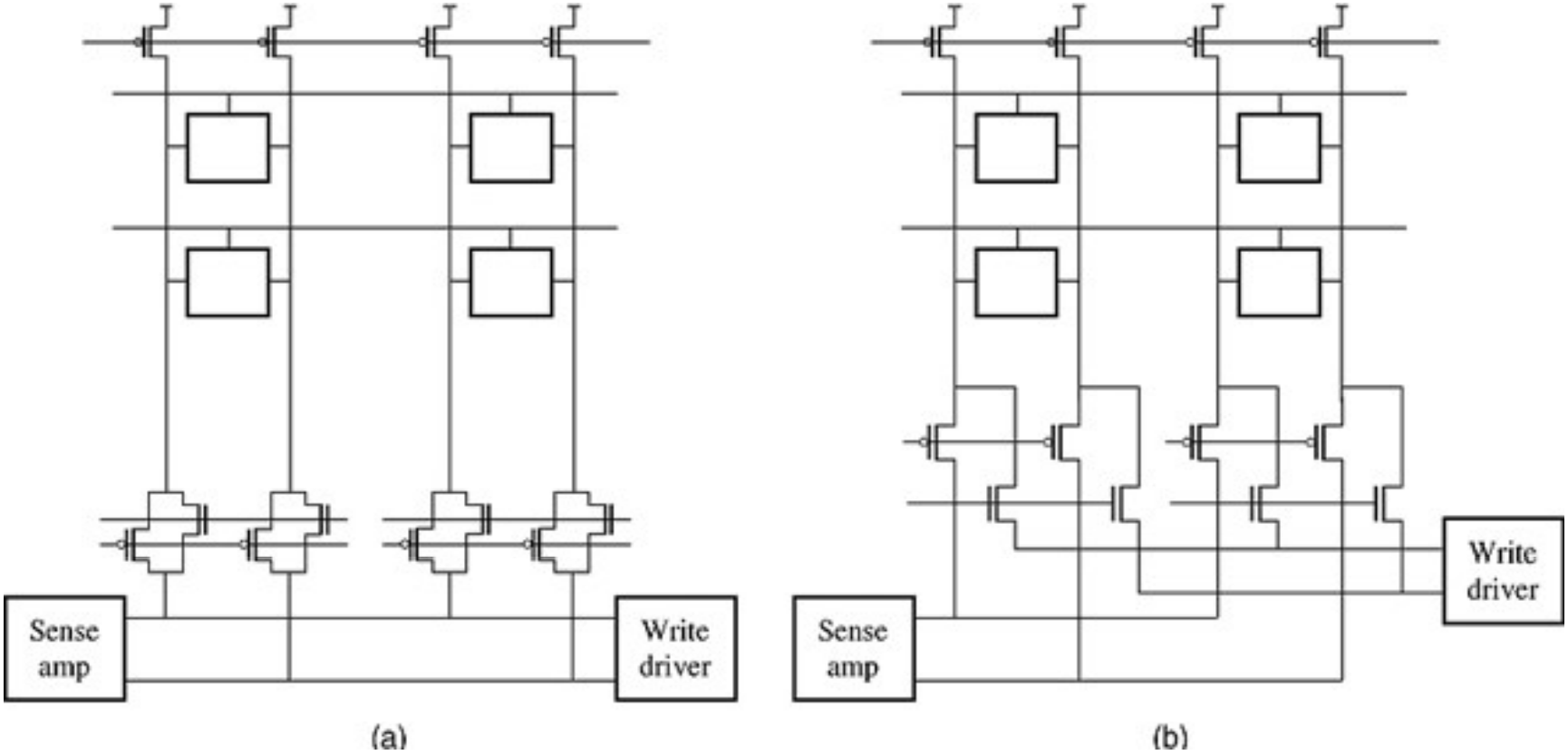
Address transition detection (ATD)



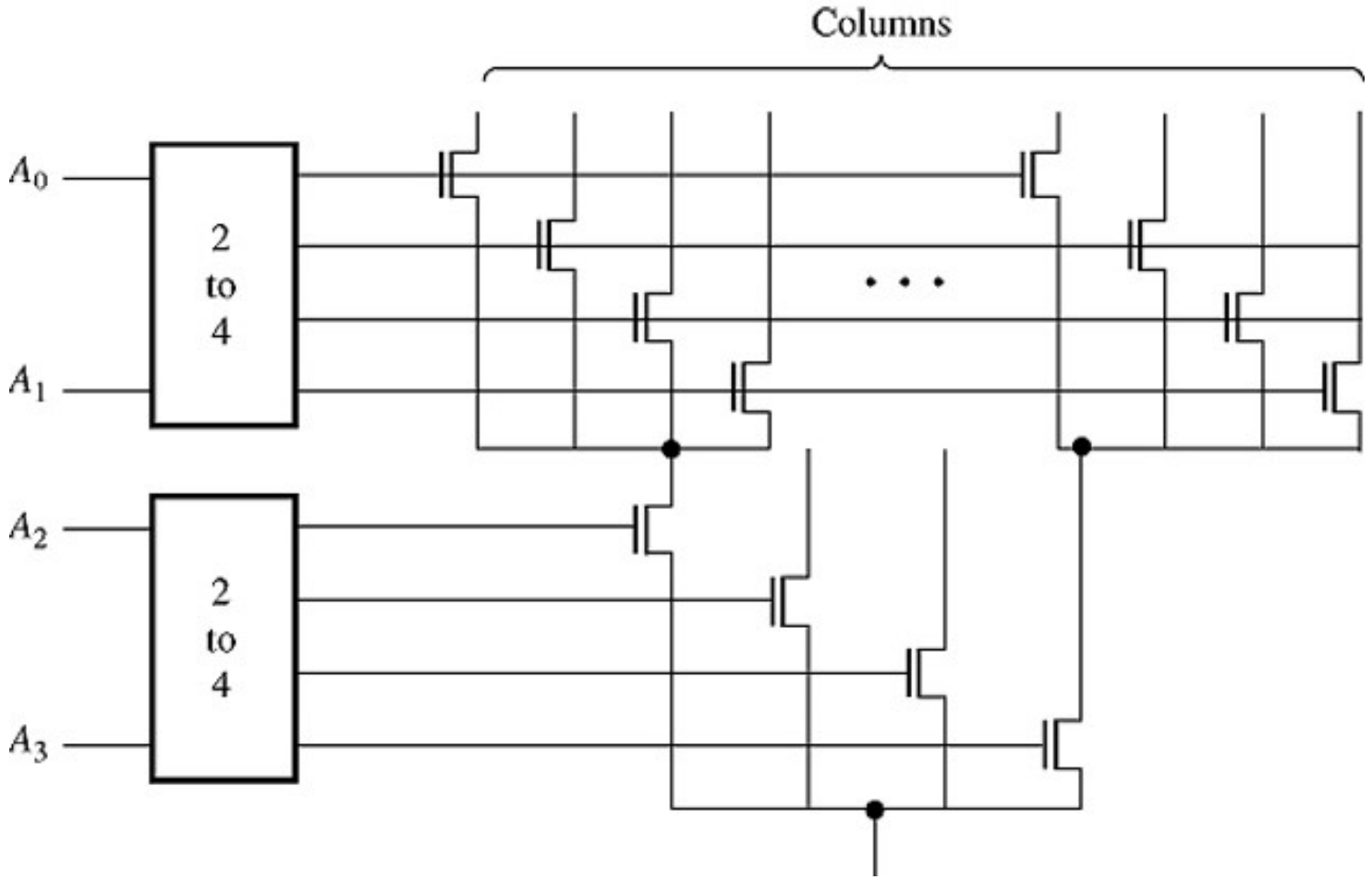
Column decoding and multiplexing



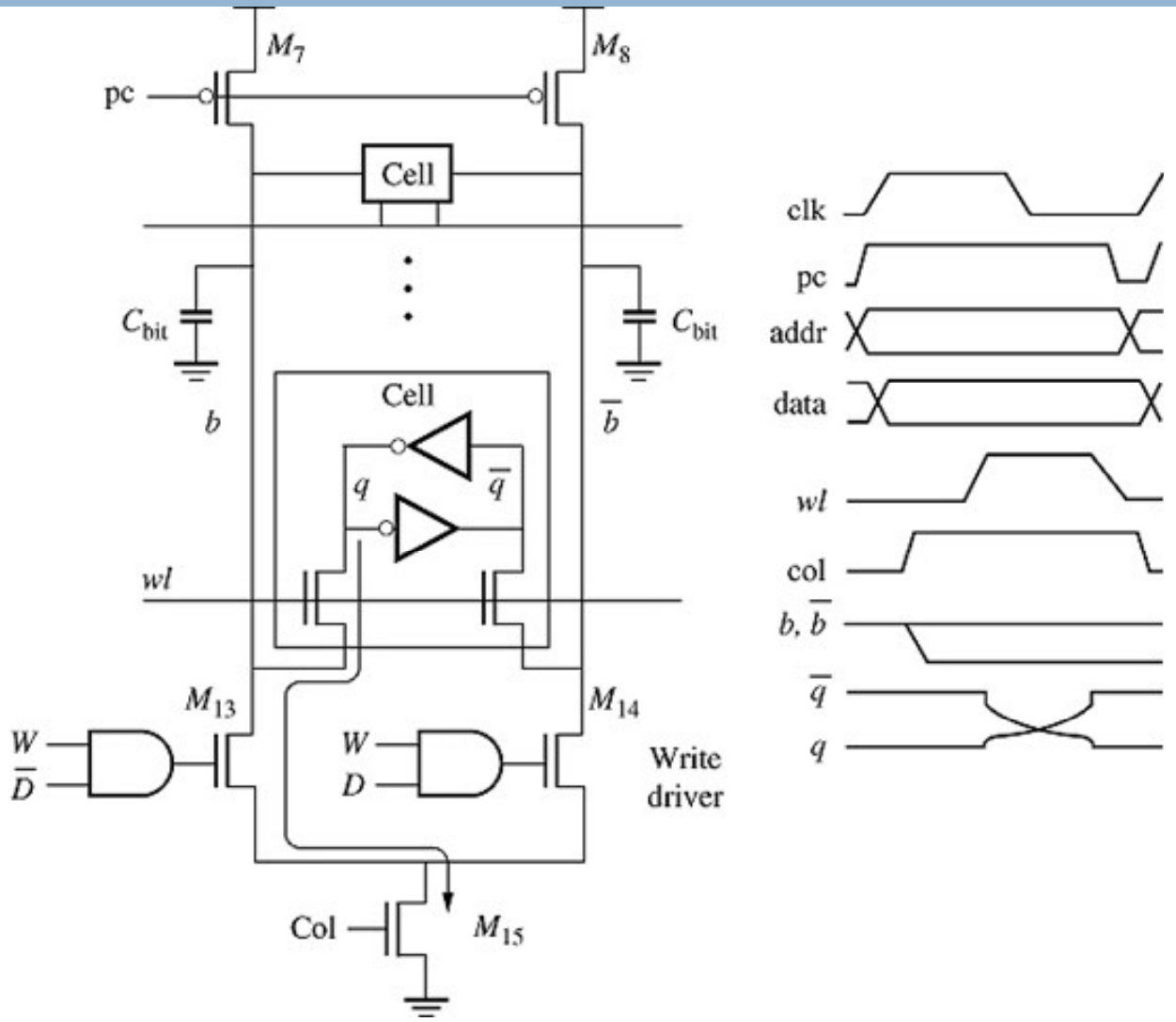
Column selection



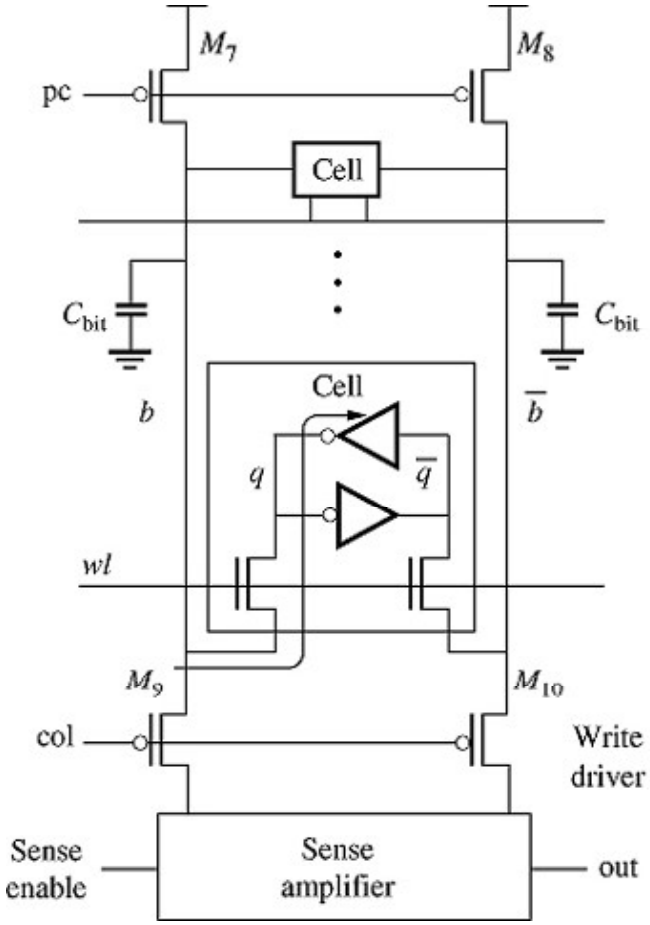
Two-level tree decoder for a 4-bit column address

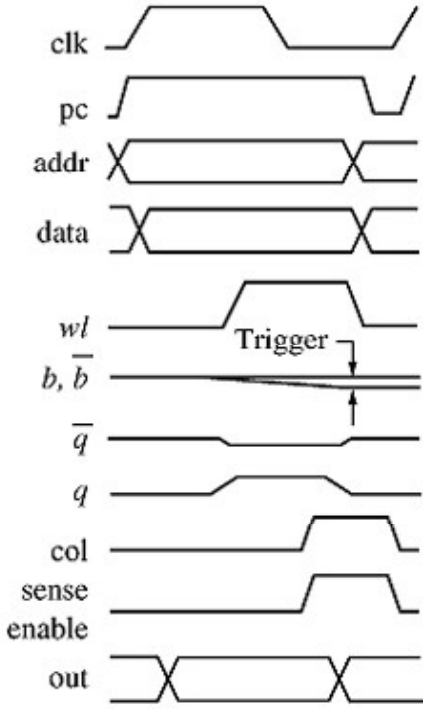


Write circuit

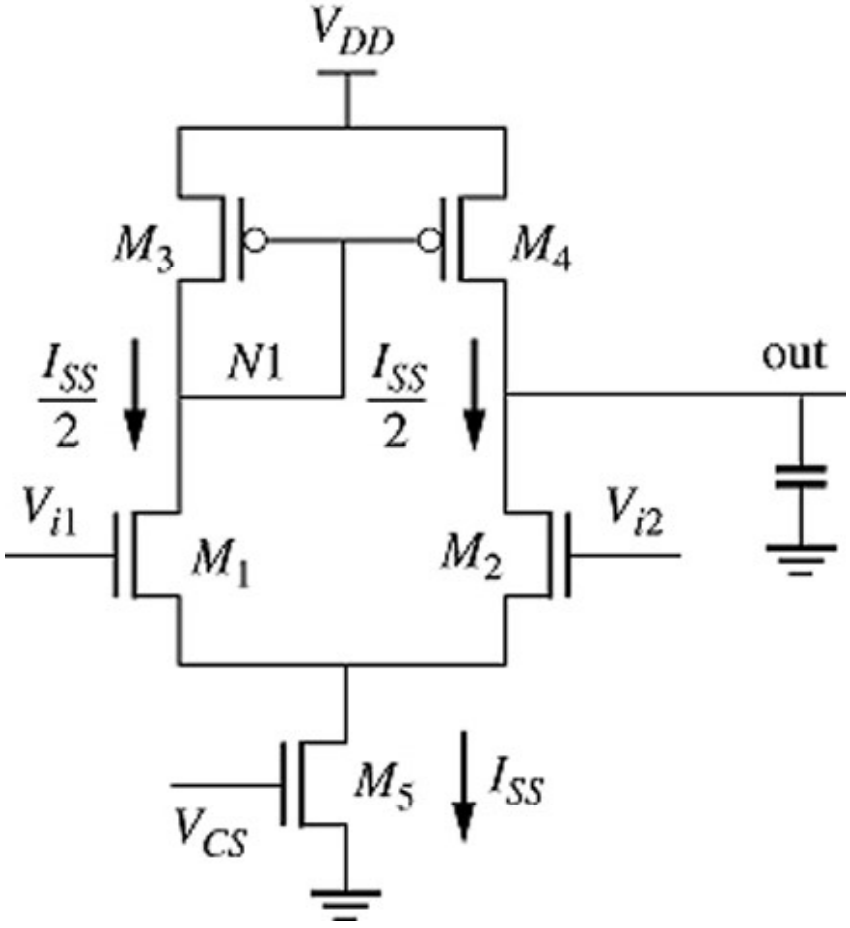


Read circuit

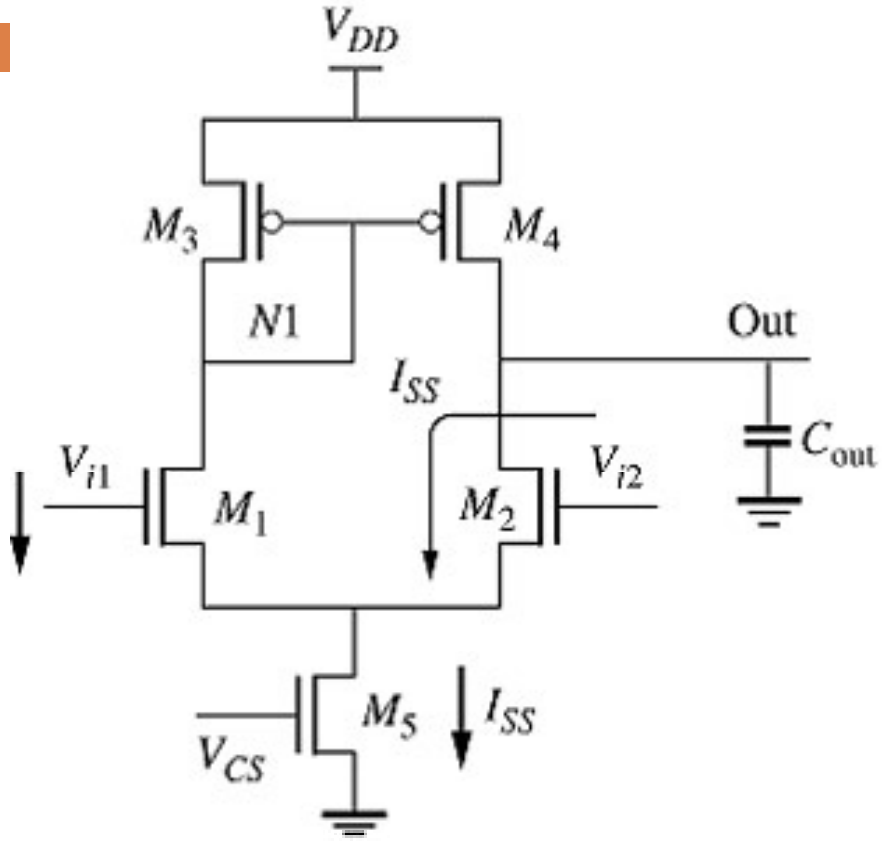




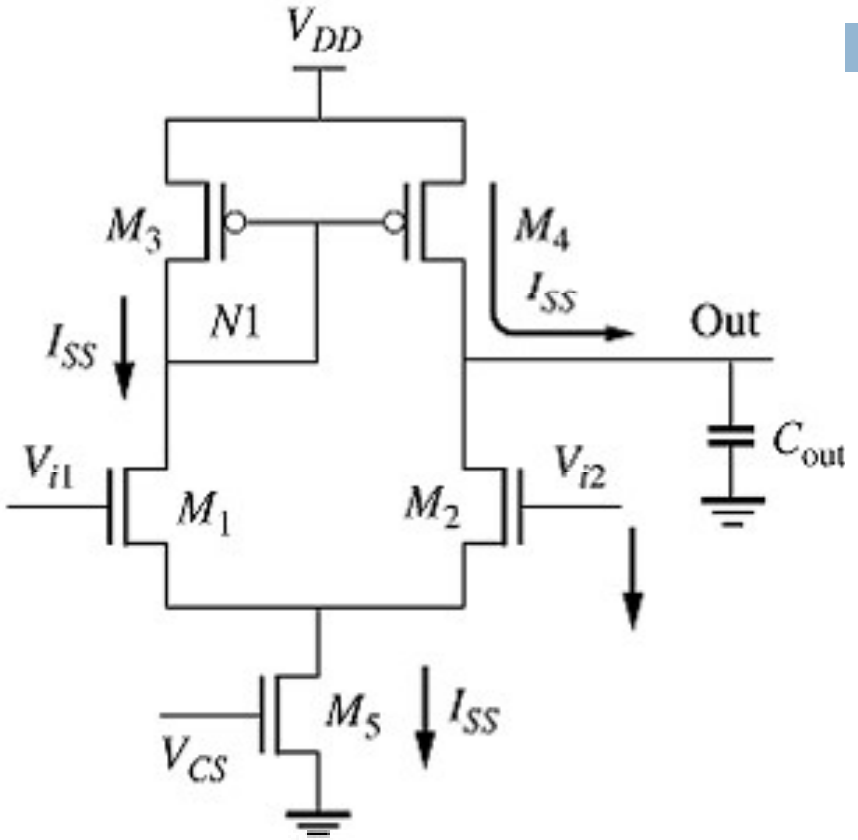
Differential voltage sense amp



Detecting 0 or 1

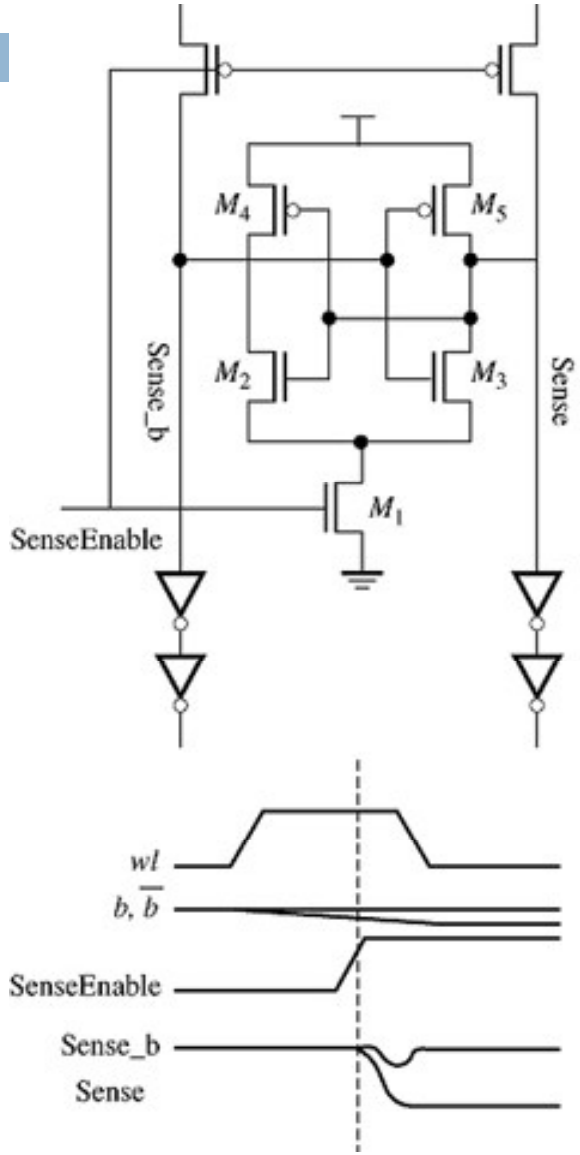


(a) Discharging output

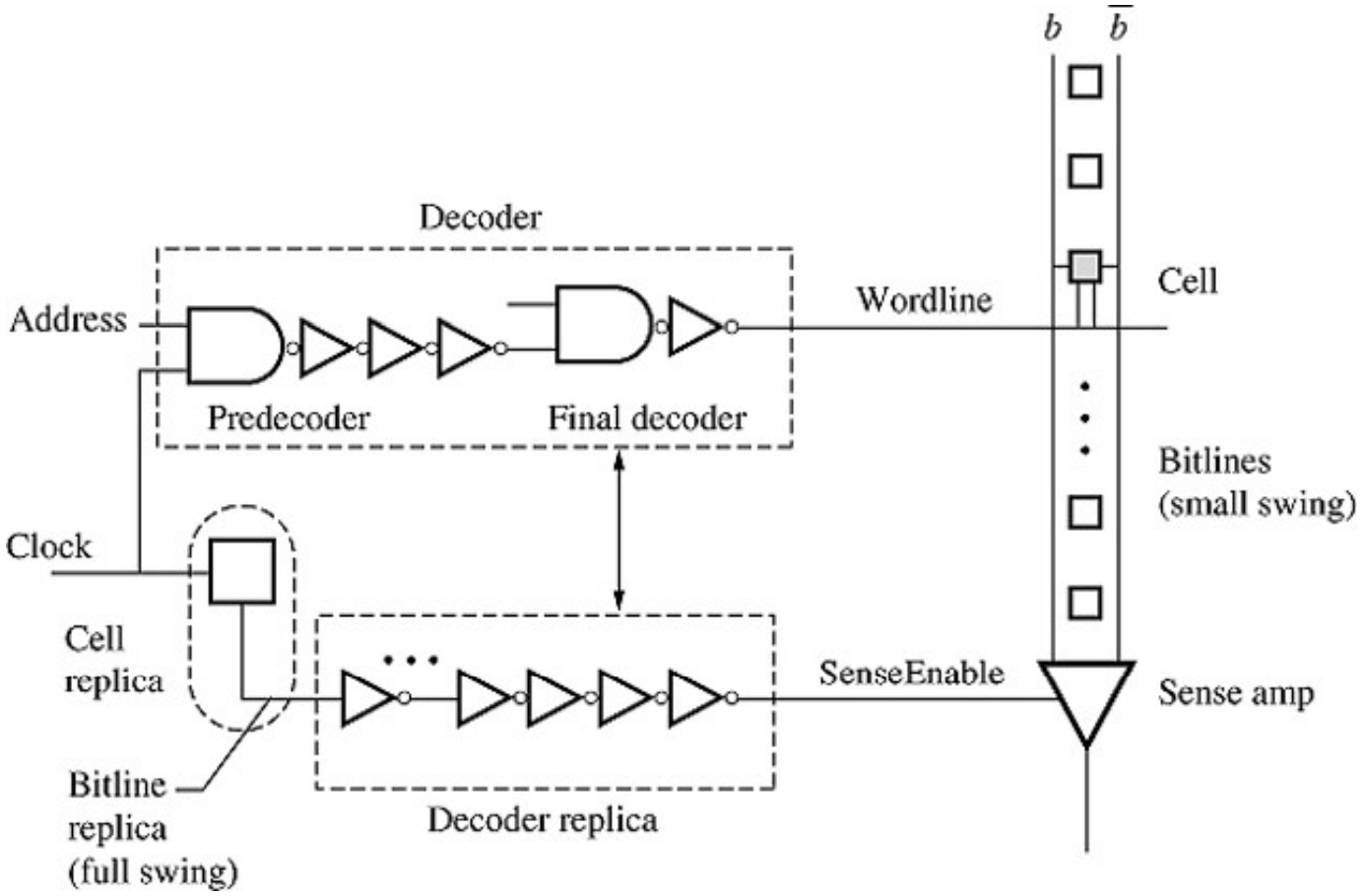


(b) Charging output

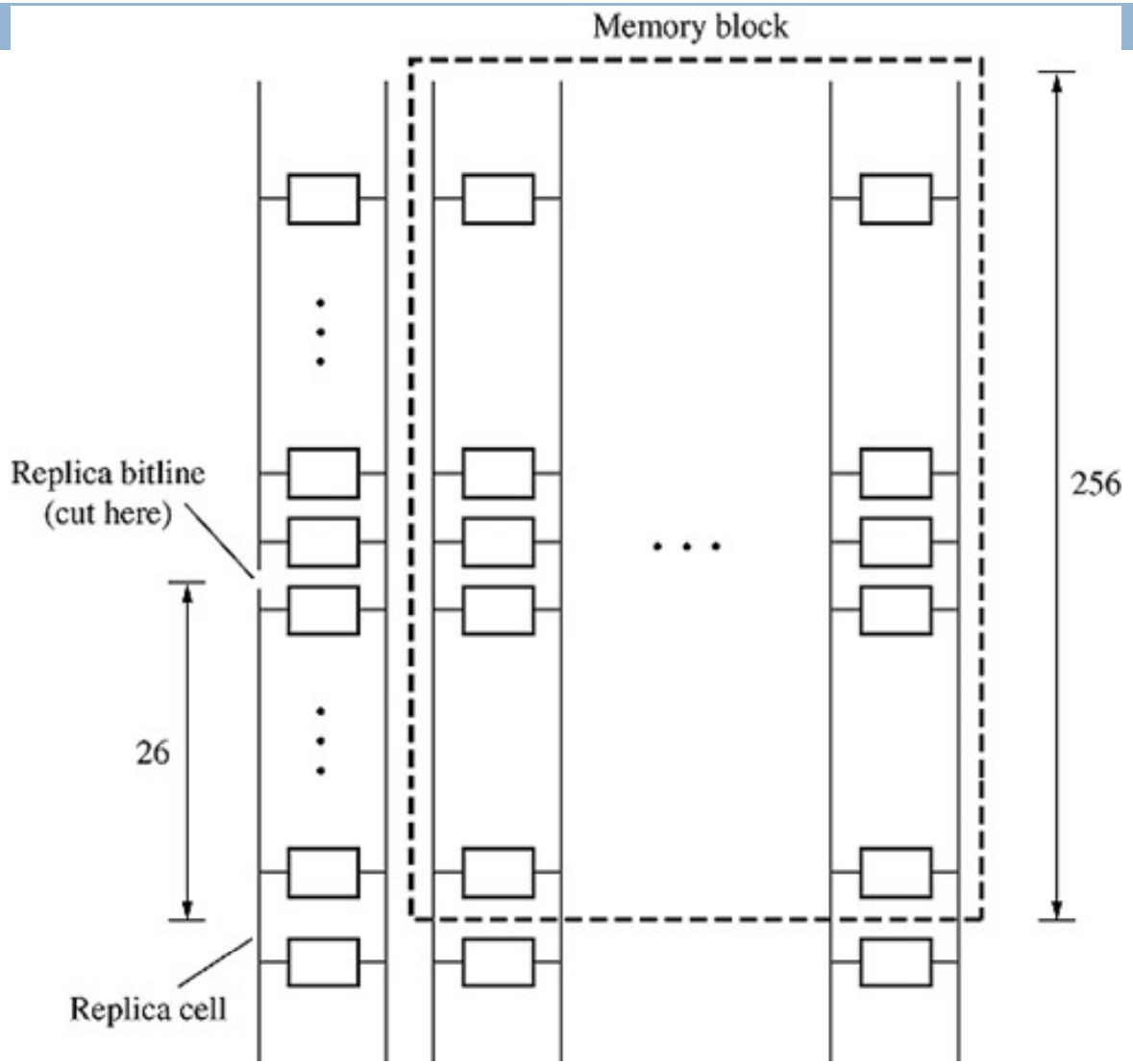
Latch-based sense amplifier



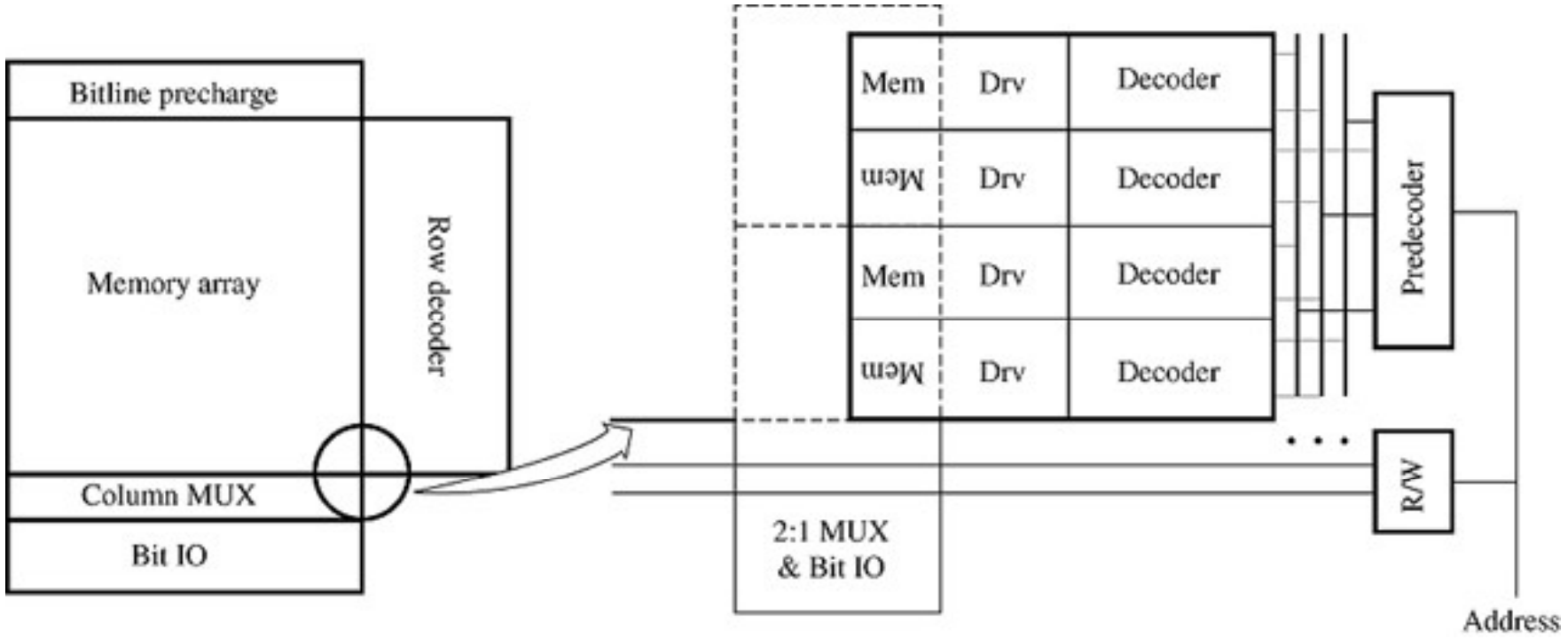
Replica circuit for sense amplifier clock enable



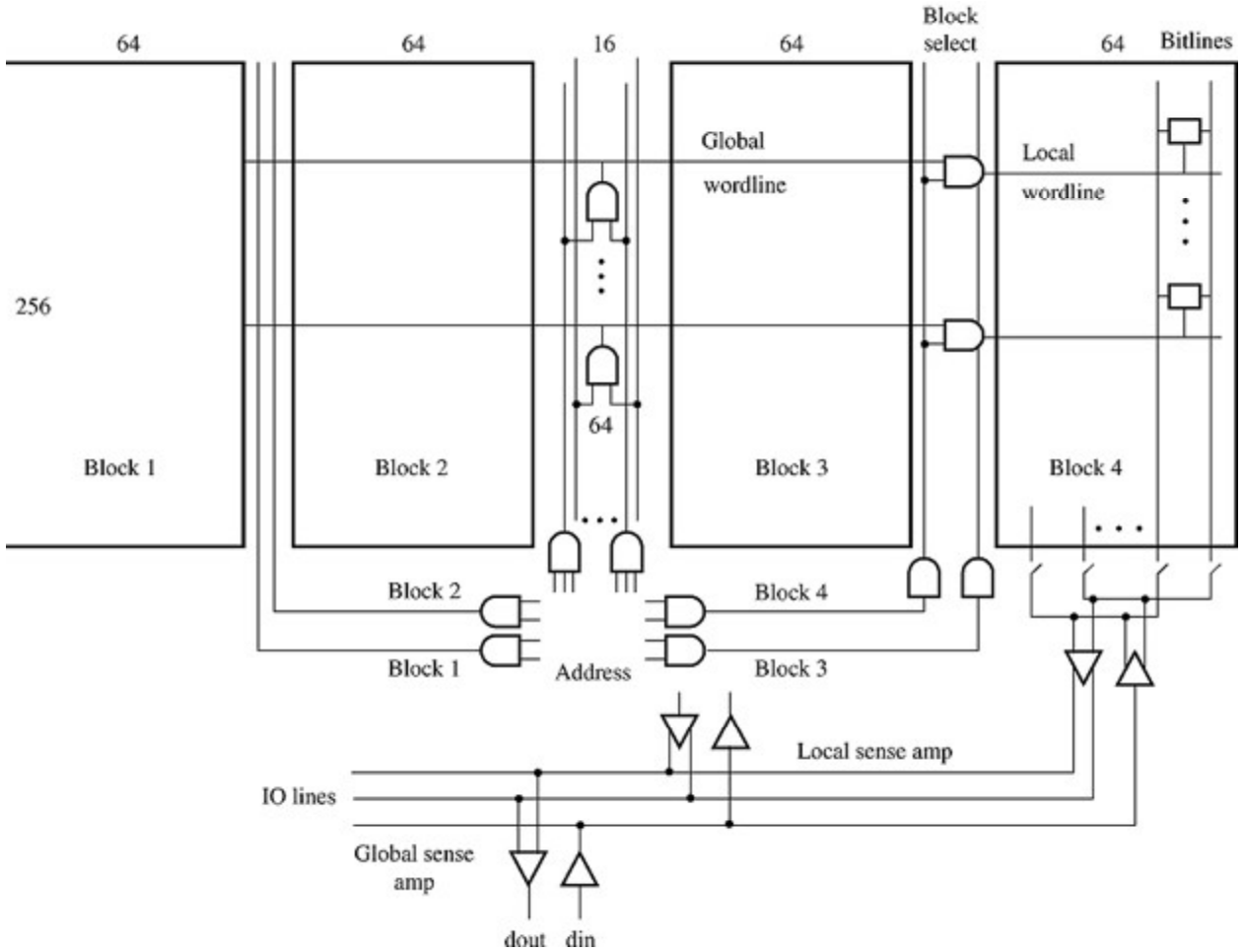
Replica cell design



Memory architecture



Divided wordline to reduce power and delay



Bitline partitioning to reduce delay