Modified SET D-Flip Flop Design for Low-Power VLSI Applications

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Abstract— **Low power device design is now a vital field of research due to increase in demand of portable devices. This research paper proposes the modified Single Edge Triggered (SET) D-flip flop design for the portable applications. Design is tested for various substrate bias voltages in sub-threshold region to opt for better design. Design comparison between previously reported design and modified design is performed at 65nm and 45nm to show technology independence. Comparative simulation results show that area and power efficient SET D-FF design is better choice for portable applications.**

Keywords- SET D-FF, Portable Applications, Single Edge Triggered, Sub-threshold Region design.

I. INTRODUCTION (HEADING 1)

The latest advances in mobile battery-powered devices such as the Personal Digital Assistants (PDA) and mobile phones have set new goals in digital VLSI design. The mobile devices require high speed and low power consumption and thus power-delay product plays important role in the designing of VLSI circuits. The operation of low frequency circuits in the sub-threshold region stands out as the optimal method of power reduction [1]. Sub-threshold current of a MOSFET transistor occurs when the gate-to-source voltage (V_{GS}) of a transistor is lower than its threshold voltage (V_{TH}). When V_{GS} is larger than V_{TH}, majority carriers are repelled from the gate area of the transistor and a minority carrier channel is created. This is known as *strong-inversion*, as more minority carriers are present in the channel than majority carriers. When V_{GS} is lower than V_{TH}, there are less minority carriers in the channel, but their presence comprises a current and the state is known as *weak-inversion*. In standard CMOS design, this current is a sub-threshold parasitic leakage, but if the supply voltage (V_{DD}) is lowered below V_{TH}, the circuit can be operated using the sub-threshold current with ultra-low power consumption.

Sub-threshold circuit operation is driven by currents much weaker than standard strong-inversion circuits, and so is characterized by longer propagation delays and limited to lower frequencies. Due to the exponential dependency on the value of V_{TH}, sub-threshold circuits are very sensitive to process variations and temperature fluctuation. These, and other factors, have to be taken into consideration when designing circuits for sub-threshold operation. One of the most complex, power consuming and indispensable components is the Flip-Flop (FF) among the various building blocks in digital designs. About 30%-70% of the total power in the system is dissipated due to clocking network, and the flip-flops [2]. The logic gate delays in a clock period is reducing by 25% per generation in high-performance microprocessors, and is approaching value of 10% or below beyond 0.13μm technology [3]. As a result, latency of the flip-flops or latches is becoming larger portion of the cycle time. Several FF designs have been proposed for power reduction. Although many of these methods have been shown to considerably reduce the power consumption, they are not necessarily suitable for operation in the sub-threshold region. In addition, some of these designs require a large number of transistors for implementation, resulting in a large area, not necessarily suitable for small, low-priced systems.

Two type of flip flops are found in literature – single edge triggered (SET) and double edge triggered (DET). The simplest flip flop design is single edge-triggered, sampling data on only one clock edge (either on rising or falling clock edge). The SET flip-flops are usually configured as Master-Slave configuration. Several single edge-triggered D flip-flop designs were proposed [4, 5] in the past to reduce either power or area or delay. Considerable research has been done to optimize the area, power and delay and always there is a trade-off among the three [1, 6]. Other type of flip-flop is double edge triggered which samples data on both clock edges. DET flip-flops have lower energy requirement (~ 20%) than set flip-flop. Double-edge triggered flip-flops suffer performance degradation when compared to their single-edge counterparts, due to more complex design and the fact that most of the complexity increase affects the signal propagation along the critical path [10]. Flip-flops can be static and dynamic in nature. Dynamic FF produces faulty logic levels when clock is removed because of charge leakage from the output node capacitances. Static FF on the other hand maintains their output state even if clock is removed [7].

Threshold voltage of the transistor plays significant role in controlling the leakage current. Threshold voltage of the transistor depends on the biasing of the transistor. Considerable work has been done to control the leakage current by substrate biasing technique and in turn to reduce the power dissipation [8, 9].

The negative edge triggered static SET D-FF design [11] is modified by using substrate biasing technique. The STGB and LVSB Designs are compared [12] and STGB design was found better. Here the STGB, LVSB and NBB designs are compared. The overall area of the design is reduced by optimizing the W/L ratio of the transistors. Designs are tested and compared in 65nm and 45 nm technology to prove its technology independence.

The rest of the paper is organized as follows: In Section II, we briefly describe the various designs of the SET D flip-flop designs discussed in this paper. In Section III, we presented the simulations and results and we draw the conclusions in Section V.

II.　SET D FLIP-FLOP DESIGNS

Conventional 16- transistor SET D flip-flop operates either at rising edge or falling edge of the clock. For the correct operation of the flip-flop, the input value has to be maintained constant just before setup time (t_{setup}) and just after hold time (t_{hold}) of the triggering edge of the clock. The circuit in the figure 1 shows a conventional 16-transistor SET D flip-flop [1, 6]. In this figure, master and slave sections are demarcated by dashed vertical line. A PMOS transistor is used in the feedback path as it leads to a more compact layout than using a NMOS transistor. In high noise environment, pass transistors may be replaced with transmission gates.
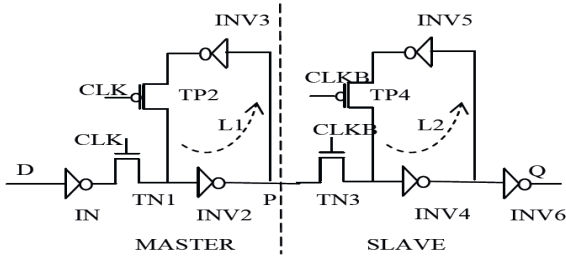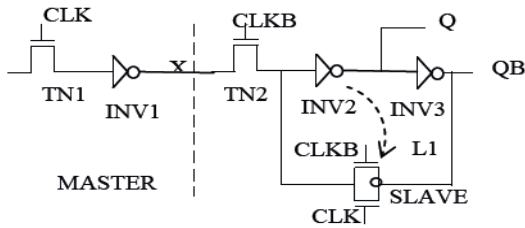

Figure 1. Conventional SET D-flip flop [1].

Figure 2. Ten-transistor SET D-flip flop [11].

Transistor	Aspect Ratio (W/L)
TN1	22 / 0.6
INV1 – NMOS	22 / 0.6
INV1 – PMOS	22 / 0.6
TN2	22 / 0.6
INV2 – NMOS	22 / 0.6
INV2 – PMOS	22 / 0.6
INV3 – NMOS	2 / 0.6
INV3 – PMOS	2 / 0.6
TG – NMOS	2 / 0.6
TG – PMOS	2 / 0.6

The design of 10-transistor negative edge triggered SET D flip-flop [11] is shown in figure 2. In this design the feedback circuit of the master section is removed and in slave section, feedback loop consists of transmission gate. When clock level is 'HIGH', master latch is functional and the inverse of the data is stored to an intermediate node X. When the clock is goes to 'LOW' logic level, the slave latch consisting of transistor TN2 and regenerative feedback loop L1 becomes functional and produces data at the output Q and QB. The SET D flip-flop maintains the logic level even if clock is permanently grounded (stopped), proves that it is static in nature. The aspect ratios of the transistors involved in the SET D flip-flop design are given in the table I. The aspect ratios of the transistors involved in regenerative feedback are made weak to provide weak feedback. In comparison to the conventional SET D flip-flop the ten-transistor SET D flip-flop is advantageous because of reduced transistor count. The circuit becomes dynamic in nature if the transmission gate is removed from the feedback loop.

This paper aims the modification of the 10-transistor design to reduce the overall area and power consumption such that the design becomes better applicable for the low power applications. To continue with this, the design is first modified by changing the substrate connections. Figure 3 shows Low Voltage Swapped Body (LVSB) [9] bias 10-tramsistor design. In this design, substrate of all PMOS transistor are connected to ground and substrate of all NMOS transistors are connected to the supply voltage (V_{dd}). In this type of substrate connection, bulk voltage is less than the source voltage ($V_B < V_S$). As a result, all devices receive an amount of forward body bias equal to V_{dd}. Figure 4 shows Sub Threshold Grounded Body (STGB) bias 10-tramsistor design [13]. In this design, substrate of all NMOS and PMOS transistors are connected to ground. This type of substrate connection reduces the complexity of the design. All the NMOS transistors are at no body bias condition and all PMOS are at forward body bias condition. STGB design is less sensitive towards supply and ground noise than LVSB design. The substrate of the MOSFET is connected to the source and thus the V_{SB} of the MOS transistor is always at zero voltage and thus it is known as No Body Bias (NBB) condition. In NBB connection, threshold voltage of the MOSFET transistor is always constant. Figure 5 shows No Body Bias (NBB) 10 – transistor negative edge triggered SET D flip-flop.
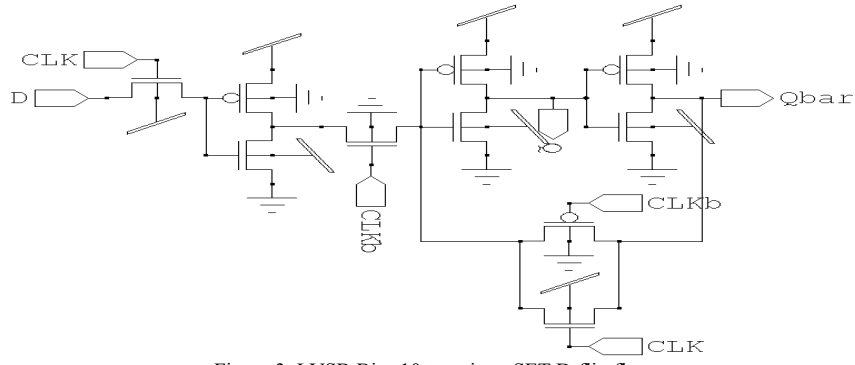
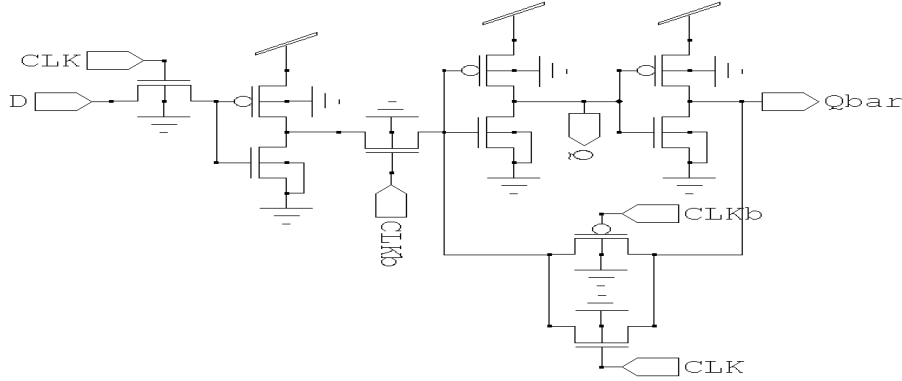Figure 3. LVSB Bias 10-transistor SET D-flip flop

Figure 4. Sub-Threshold Grounded Body (STGB) [8] Bias 10-transistor SET D-flip flop
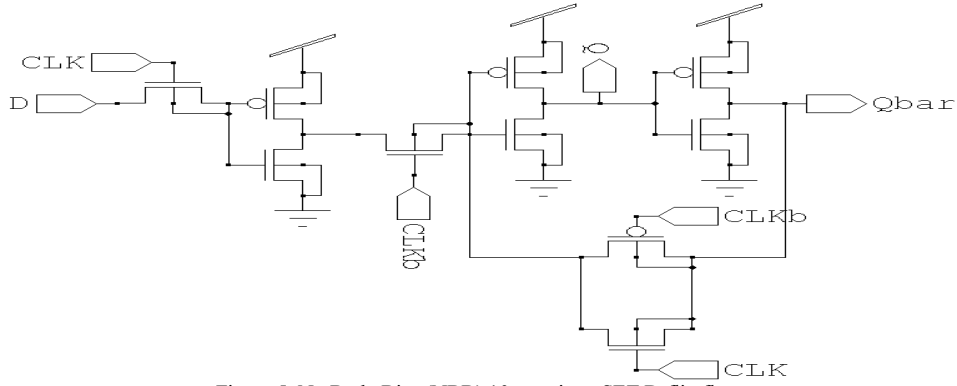

Figure 5. No Body Bias (NBB) 10-transistor SET D-flip flop

III. SIMULATION AND ANALYSIS

The 10-transistor and 16-transistor SET D flip-flop designs are tested in 65nm technology using tanner tools v12.6. Table II gives the comparison result of the two designs. From the table II, it is clear that the power and delay and thus the power-delay product of the 10-transistor design is better than the conventional 16-transistor design. Also the design superiority of 10-transistor over 16-transistor SET D flip-flop design is proved earlier [11] Thus further the 10-transistor SET D flip-flop design will be considered in the paper.

TABLE II. COMPARISON OF 16-TRANSISTOR AND 10-TRANSISTOR SET D FLIP-FLOP.

S. no.	SET Flip flop	Power	delay	Power-delay product
1.	16-transistor	2.53e-8	5.23e-5	1.32e-13
2.	10-transistor	3.28e-9	5.13e-6	1.68e-15

During the simulation and calculation, the designs are tested in 65 nm and 45 nm technologies to prove their technology independence. First the data in 65 nm is compared and then the data in 45 nm is taken to show the design superiority of one over others. Designs are compared by taking the temperature, frequency and supply voltage as a parameters.
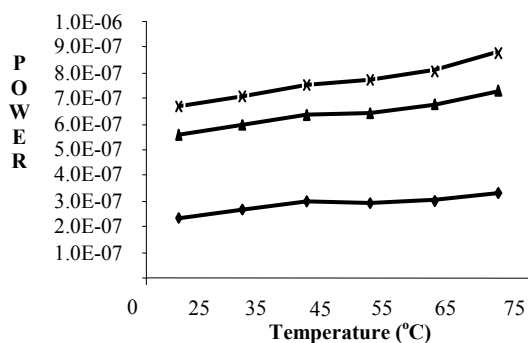
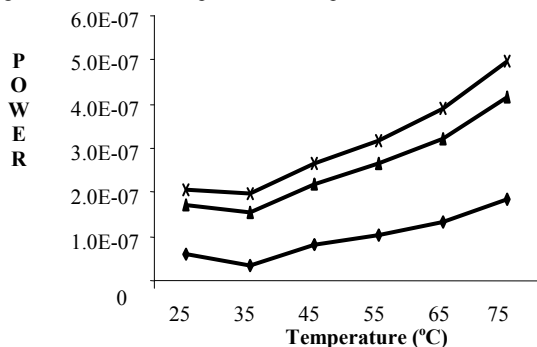Figure 6. Power Consumption with Temperature at 65 nm technology.

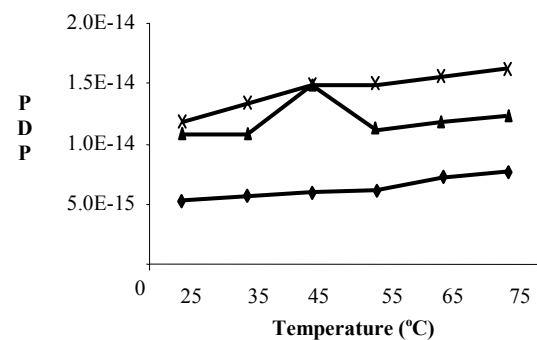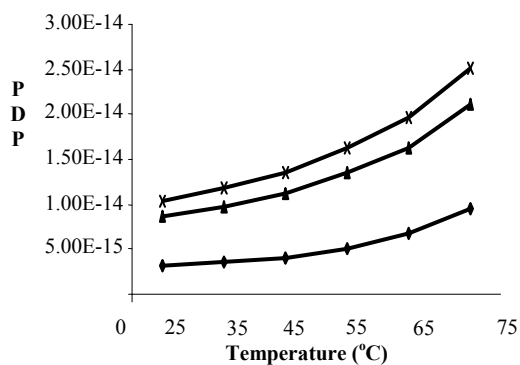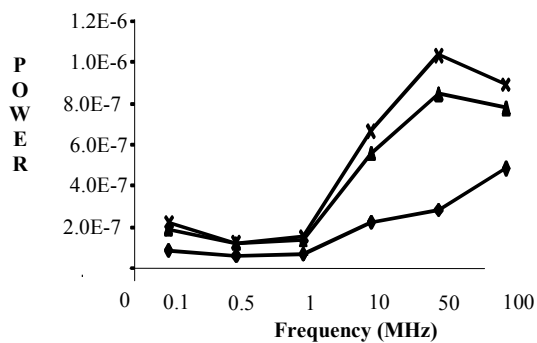Fig.10 Power Consumption at various frequencies in 65 nm technology

Figure 7. Power Consumption with Temperature at 45 nm technology

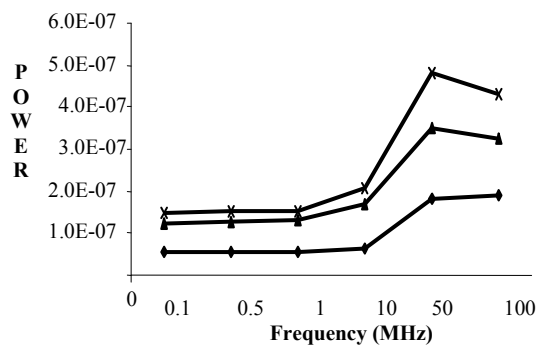Figure 11. Power Consumption at various frequencies in 45 nm technology
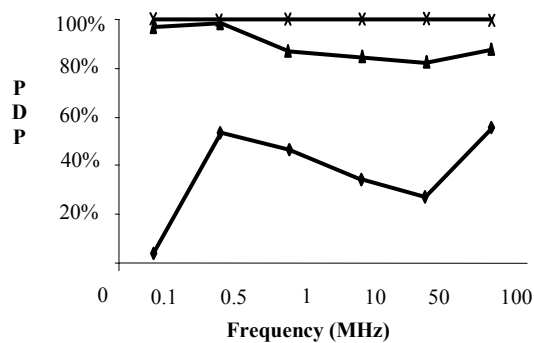

Figure 8. Power-Delay Product with Temperature at 65 nm technology

Figure 12. Power-Delay Product at various frequencies in 65nm technology in percentage scale

Figure 9. Power-Delay Product with Temperature at 45 nm technology

Figure 13. Power-Delay Product at various frequencies in 45nm technology in percentage scale

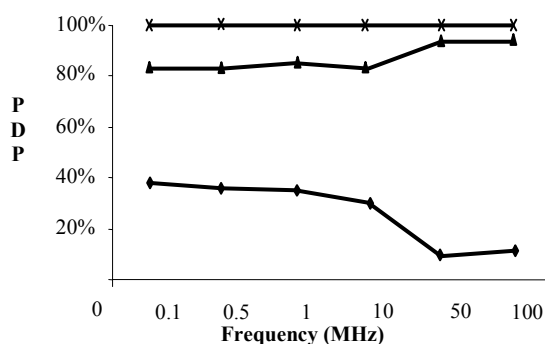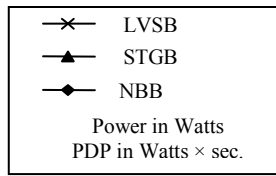| | LVSB |
	STGB
	NBB
Power in Watts	
PDP in Watts × sec.	

Figure 14. Legends

Figure 6 and 7 shows the power consumption comparison of the LVSB, STGB and NBB biased designs at 65 nm and 45 nm technology. It is clear that the No-Body bias design shows less power consumption than the contending LVSB and STGB designs at all the values of the temperature. Similar results can be viewed for the Power-Delay Product (PDP) from the figure 8 and 9. Thus at 65 nm and 45 nm technology, where channel lengths of the MOSFET are taken 70 nm and 50nm respectively, the power consumption and PDP of the NBB design is less and hence the temperature sustainability of the NBB design is better. As shown in the figure 10 and 11, the power consumption by the NBB design is always less than the STGB and LVSB design at all the frequencies ranging from 0.1 MHz to 100 MHz. The power delay product of STGB and NBB are drawn with respect to LVSB in figure 12 and 13. The power-delay product of the STGB design is on an average 10% less than the LVSB design but the NBB design shows 63% improvement than the LVSB design and 53% than the STGB design (figure 12) in 65 nm technology. In 45 nm technology, STGB design shows 13% improvement and NBB design shows 61% reduction in power delay product than the LVSB biased design (figure 13).Figure 14 shows the legends used from figure 6 – 13.

Earlier proposed design [11] with the reported aspect ratio and No Body Biasing is compared with the LVSB, STGB and NBB design with W/L ratio 2. From the table III and IV, it is clear that the LVSB, STGB and NBB designs at W/L = 2 are showing less power consumption than the earlier proposed design with the reported aspect ratio and No-Body Biasing. NBB design with W/L = 2 shows less power consumption among all the designs, so it is better choice for low power VLSI design.

TABLE III. COMPARISON OF VARIOUS SET D FLIP-FLOP DESIGNS IN 65NM TECHNOLOGY.

Design	Power Consumption (Watts)
LVSB	1.238054e-008
STGB	1.179902e-008
Earlier Design [11] with NBB	1.044951e-007
NBB	7.287432e-009

TABLE IV. COMPARISON OF VARIOUS SET D FLIP-FLOP DESIGNS IN 45NM TECHNOLOGY.

Design	Power Consumption (Watts)
LVSB	8.994676e-009
STGB	8.584484e-009
Earlier Design [11] with NBB	3.501623e-008
NBB	6.498465e-009

IV. CONCLUSION

In low power applications area and power consumption by the device are the main technological aspects to prefer a design over the other contending designs. The NBB design of SET D flip-flop shows better performance in terms of power dissipation and area among designs discussed in present research article. This design is tested in 65nm and 45nm technology, thus it is also technology independent. Hence NBB design of negative edge triggered static SET D-FF design is suitable for portable application, as it is more area and power efficient.

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