VLSI DESIGN FLOW

SYSTEM IDEA

SYSTEM LEVEL VERIFICATION

IDENTIFYING SUB-BLOCKS

BOTTOM-UP (FULL CUSTOM)

TOP-DOWN (STANDARD CELL)

SUB-BLOCK SCHEMATIC

RTL CODE (HDL)

STRUCTURAL CODE (HDL)

TRANSISTOR LEVEL SIMULATION

TARGET LIBRARY

LOGIC SYNTHESIS &TARGET LIBRARY MAPPING

SCHEMATIC CAPTURE

LAYOUT

GATE LEVEL NETLIST

EXTRACTION

DIGITAL SIMULATION

LAYOUT vs SCHEMATIC CHECK (LVS)

PLACEMENT&ROUTING (STANDARD CELLS)

POST-LAYOUT SIMULATION

POST-LAYOUT SIMULATION

PLACEMENT&ROUTING (TOP LEVEL)

TOP LEVEL VERIFICATION

TAPE-OUT

PROTOTYPING

TEST

FABRICATION

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