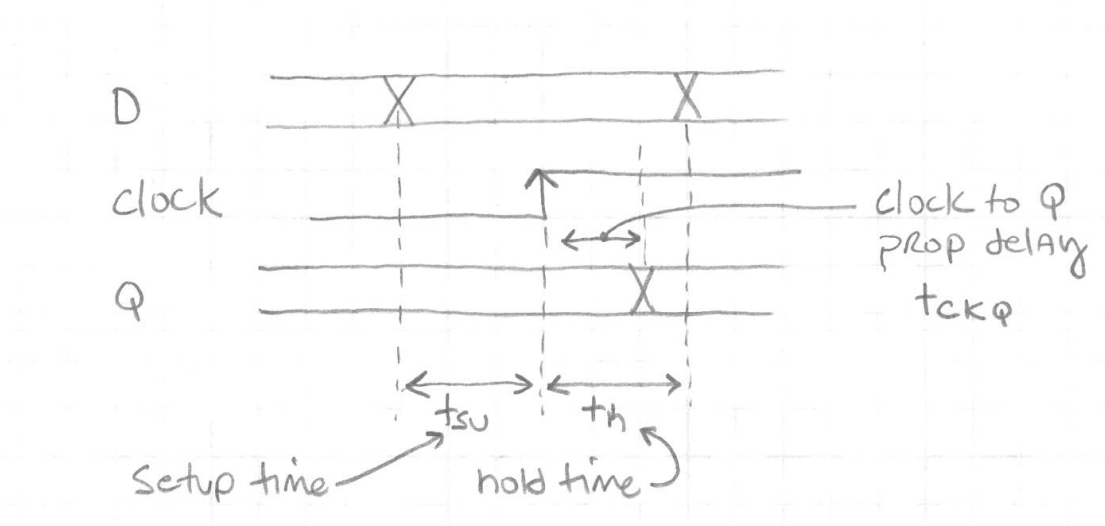
Review of Flip Flop Setup and Hold Time

- Considering D-type edge-triggered, Flip Flops (FF's) khắt khe
- Just before and just after the clock edge, there is a critical time region where the D input must not change.



- The region just before the clock edge is called *setup time* (t_{su})
- The region just after the clock edge is called *hold time* (t_h)

Review of Flip Flop Setup and Hold Time

- Every FF has minimum required values for t_{su} and t_h.
- Usually found in the data sheet or .lib file.
- From saed90nm_typ_ht.lib:

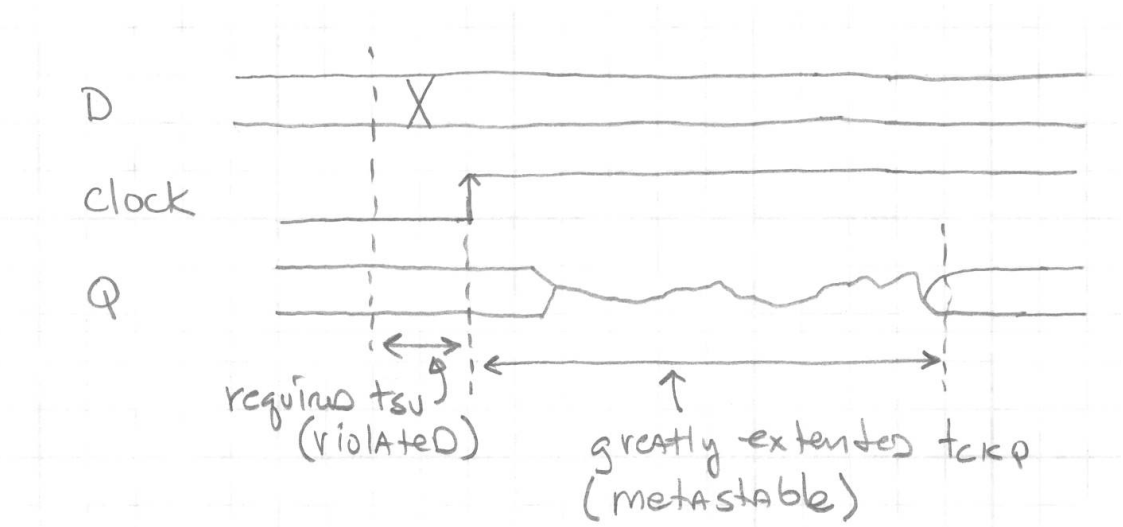
```
cell(AODFFARX2) {
  pin(D) {
   timing() {
     timing_type     : setup_rising;
     related_pin     : "CLK";
     fall_constraint(vio_0_7_7) {
     values( " 0.129318, 0.130474, 0.134615, 0.143814, 0.164042, 0.205415, 0.275800",\
             " 0.126790, 0.128403, 0.132544, 0.141743, 0.161972, 0.203344, 0.273730",\
     rise_constraint(vio_0_7_7) {
     values( " 0.181503, 0.183574, 0.188631, 0.198288, 0.216227, 0.246614, 0.286787",\
             " 0.178975, 0.181046, 0.186103, 0.195759, 0.213699, 0.243627, 0.284258",\
     ............
   timing() {
     timing_type     : hold_rising;
     related_pin     : "CLK";
     fall_constraint(vio_0_7_7) {
     values( " -0.073929, -0.075542, -0.079683, -0.088882, -0.108653, -0.146363, -0.206220",\
             " -0.071858, -0.073471, -0.077155, -0.086354, -0.106582, -0.144293, -0.204150",\
     ............
```

Review of Flip Flop Setup and Hold Time

- FFs in ASIC libraries have t_{su}'s about 3-10x the t_{pd} of a 1x inverter.
- They have t_h's ranging from about negative 1 x the t_{pd} of an inverter to positive 1-2x the t_{pd} of the same inverter.
- t_{su} and t_h vary strongly with temperature, voltage and process.
- t_{su} and t_h are functions of the G_{bw} of the FF transistors.

Review of Flip Flop Setup and Hold Time

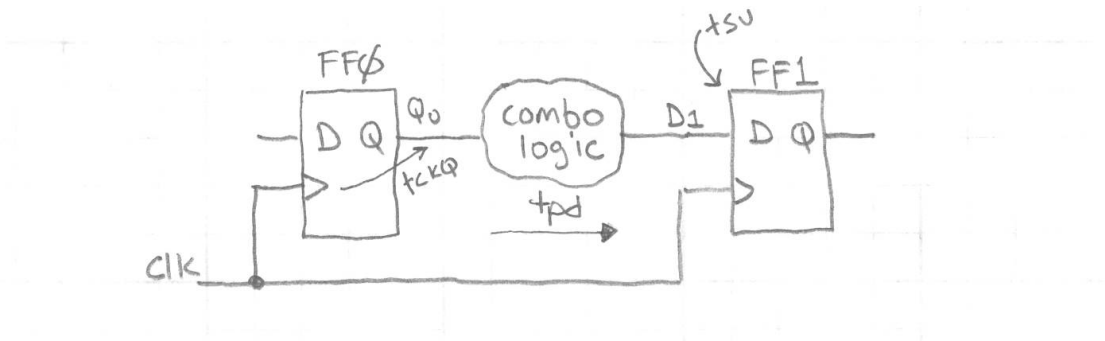
- If the D input changes within the t_{su} and t_h window, Q may:
  - Follow D correctly
  - Follow D incorrectly
  - Assume a metastable state for an indeterminate time followed by a transition to logic 1 or logic 0.



- For correct operation, D inputs must be stable for a t_{su} prior to clock and stay stable for a t_h afterwards.

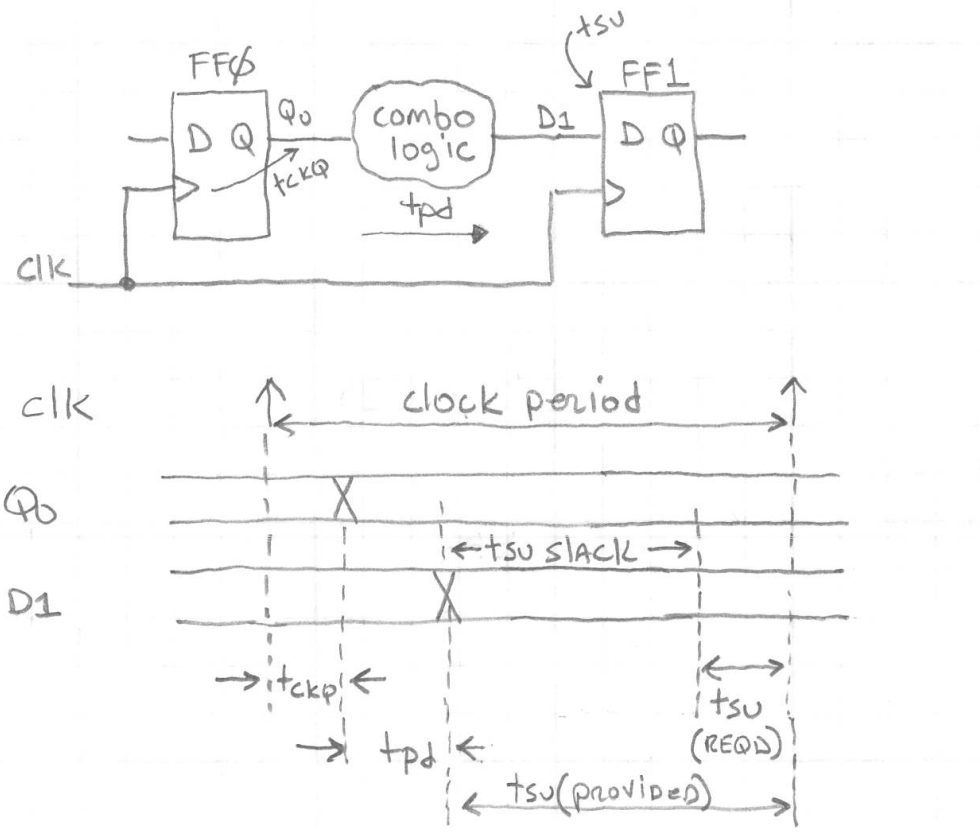
Review of Flip Flop Setup and Hold Time

- Synchronous circuit minimum cycle time is effected by setup time.
- Between clock edges, the path between two FFs is composed of:
  - clock to Q delay of FF0 (t_{ckq})
  - propagation delay through combo logic (t_{pd})
  - the required setup time (t_{su}) of FF1
- t_{ckq} and t_{pd} are both delays. t_{su} is a constraint of FF operation.



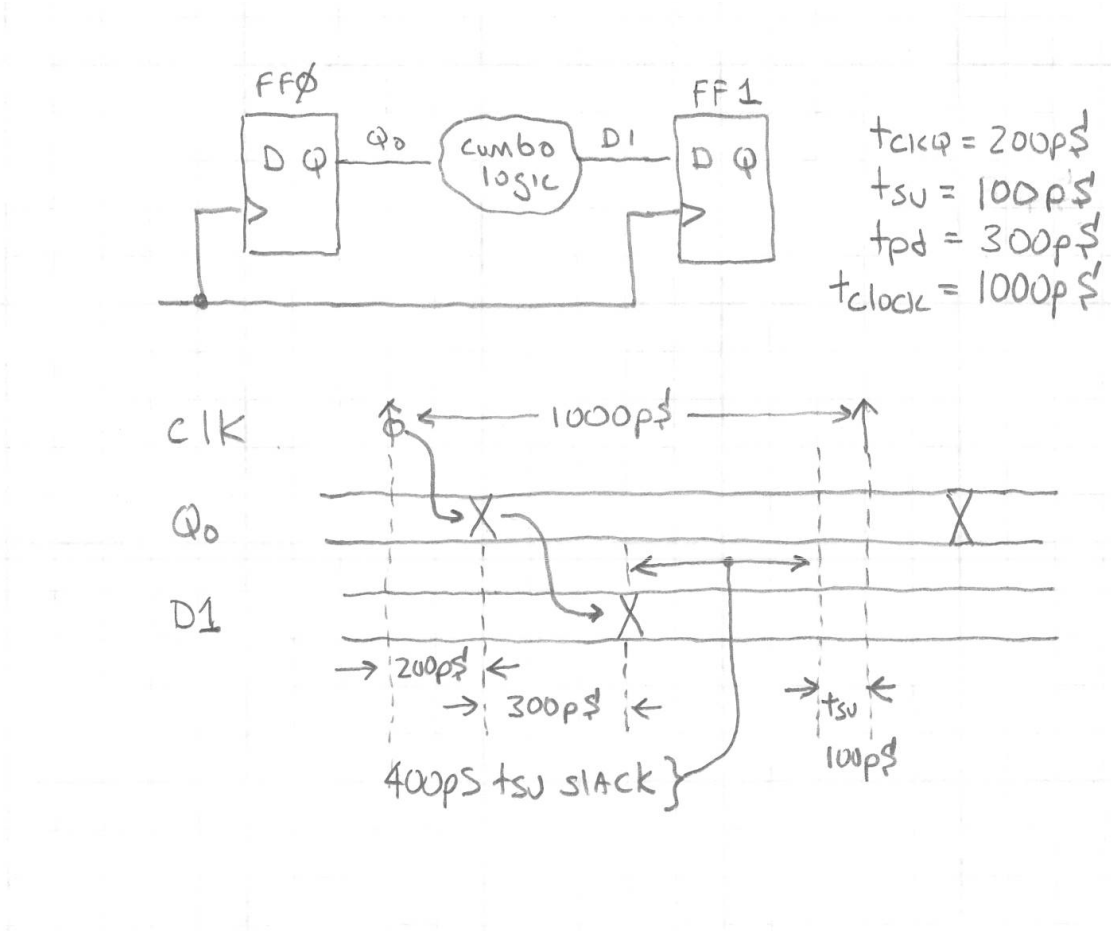
Review of Flip Flop Setup and Hold Time

- The circuit provides setup time as a function of the clock period, t_{ckq} and combo logic delay t_{pd}.
- The FF requires a specified t_{su} to operate correctly.
- The difference between the two is called *setup time slack*.
  - setup time slack = (provided setup time) - (required setup time)
  - We always want positive slack.



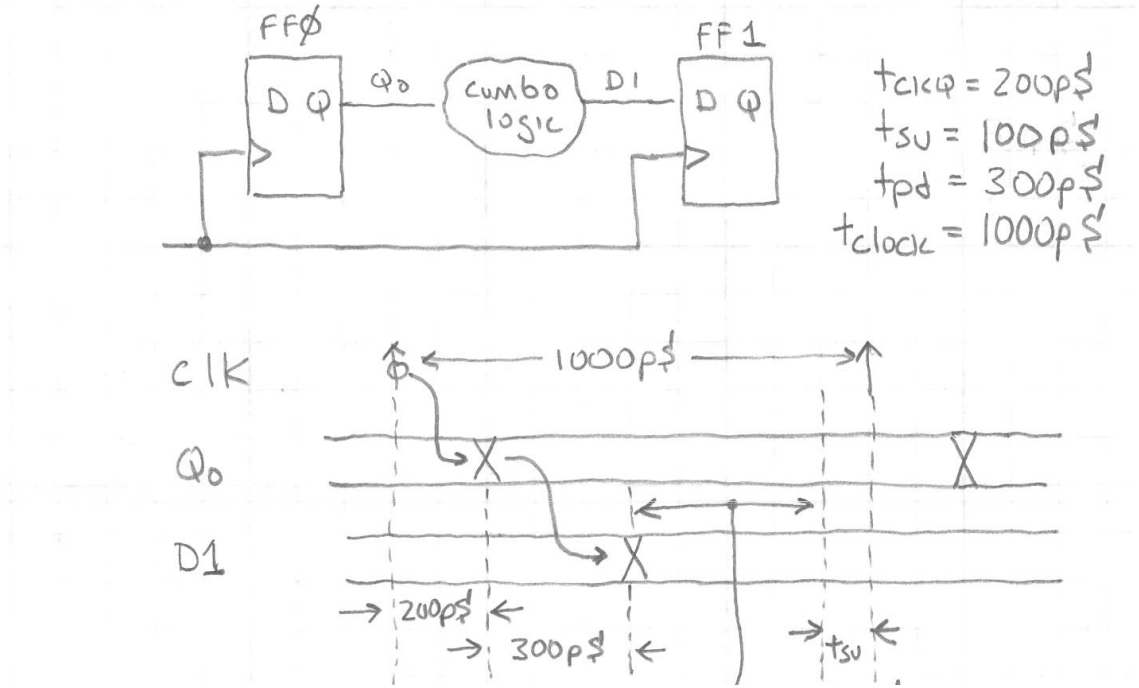
Review of Flip Flop Setup and Hold Time

- An example: find the setup slack



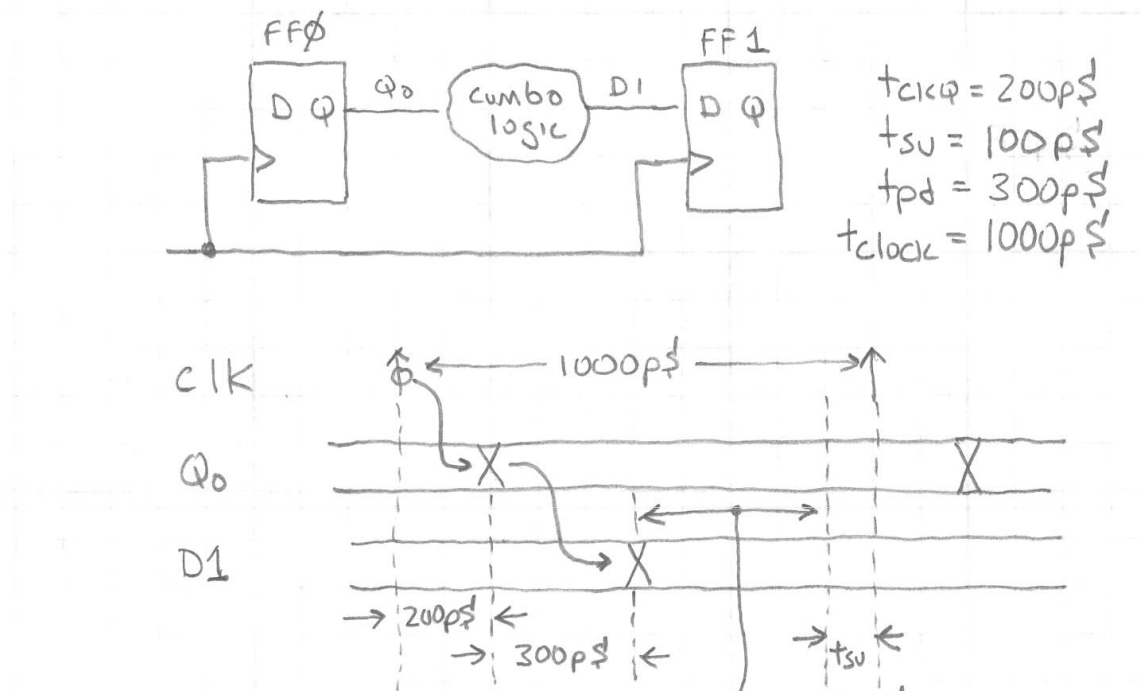
Review of Flip Flop Setup and Hold Time

- What is the minimum cycle time for the circuit?



Review of Flip Flop Setup and Hold Time

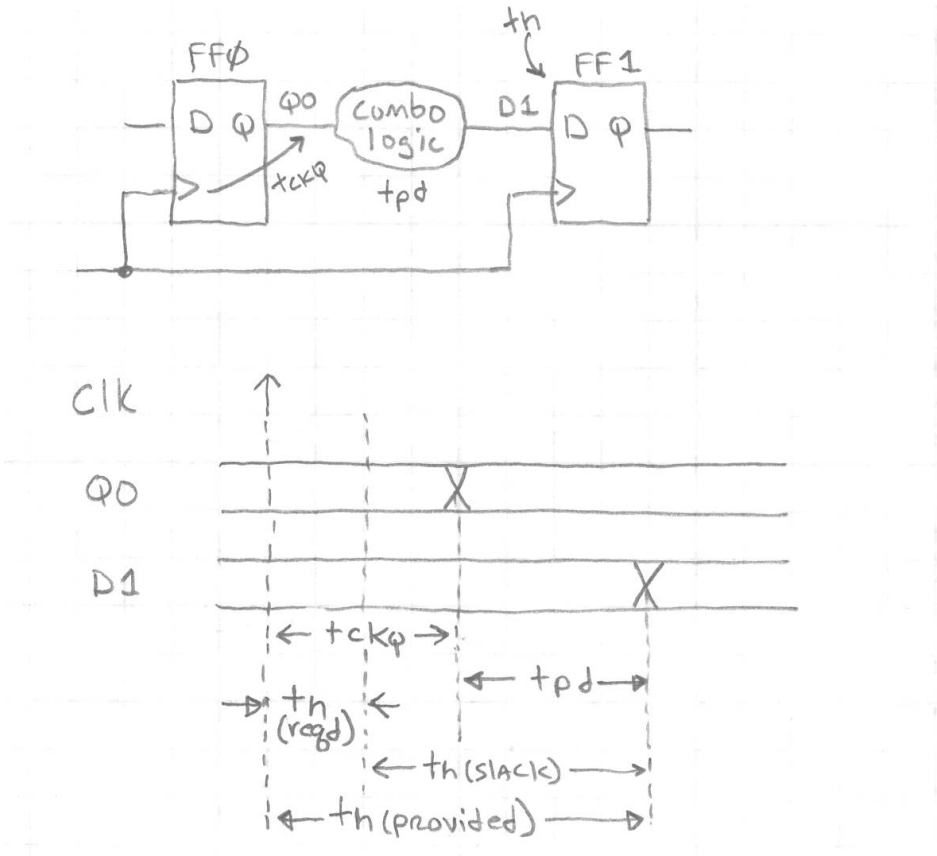
- What is the minimum cycle time for the circuit?



- minimum cycle time
  $= t_{ckq} + t_{pd} + t_{su}$
  $= 200 + 300 + 100$
  $= 600pS$

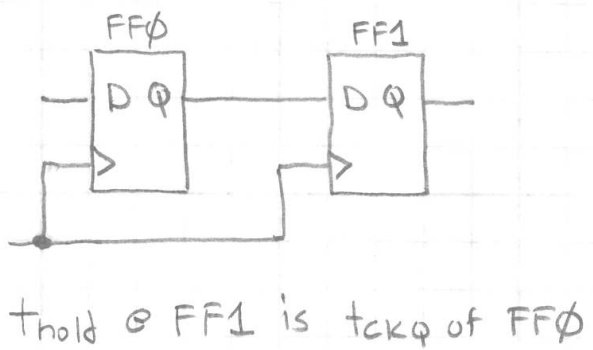
Review of Flip Flop Setup and Hold Time

- Hold time is the amount of time that FF0's old data must persist at the D input of FF1 after the clock edge.
- FF's have a specified minimum hold time.
- The circuit provides hold time to the FF of $(t_{ckq} + t_{pd})$.
- Hold time slack = (hold time provided - hold time required)



Review of Flip Flop Setup and Hold Time

- Worst case hold time scenario: FFs directly connected D-to-Q.
- In this case, the provided hold time is the t_{ckq} of the previous FF.
- This places a restriction on FF timing such that $t_{ckq} > t_h$

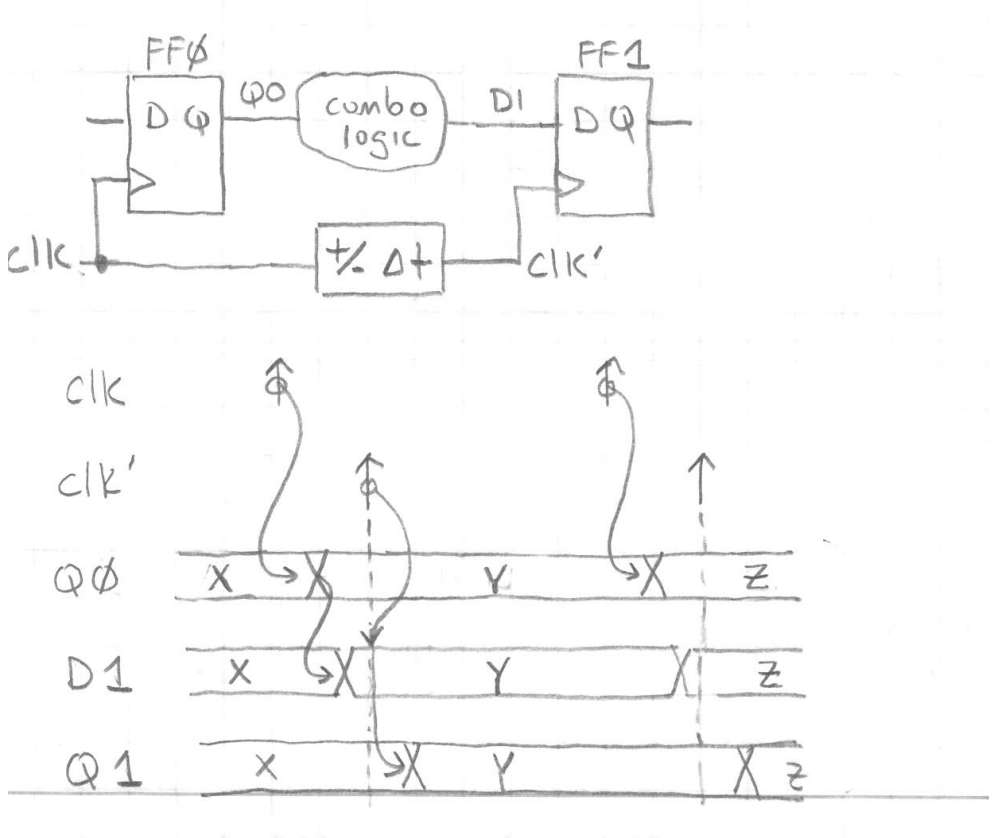


Review of Flip Flop Setup and Hold Time

- So far, we have looked at FF timing assuming an ideal clock.
- Each FF "saw" the clock edge at exactly the same time.
- In reality, this does not happen.
  - Interconnect metal length to FF clock pins differs slightly.
  - Some FFs have differing capacitance at their clock pins.
  - The t_{pd} of the clock tree buffers will be effected by differing temperature and voltage across the die. These effects are dynamic and cannot be determined apriori.

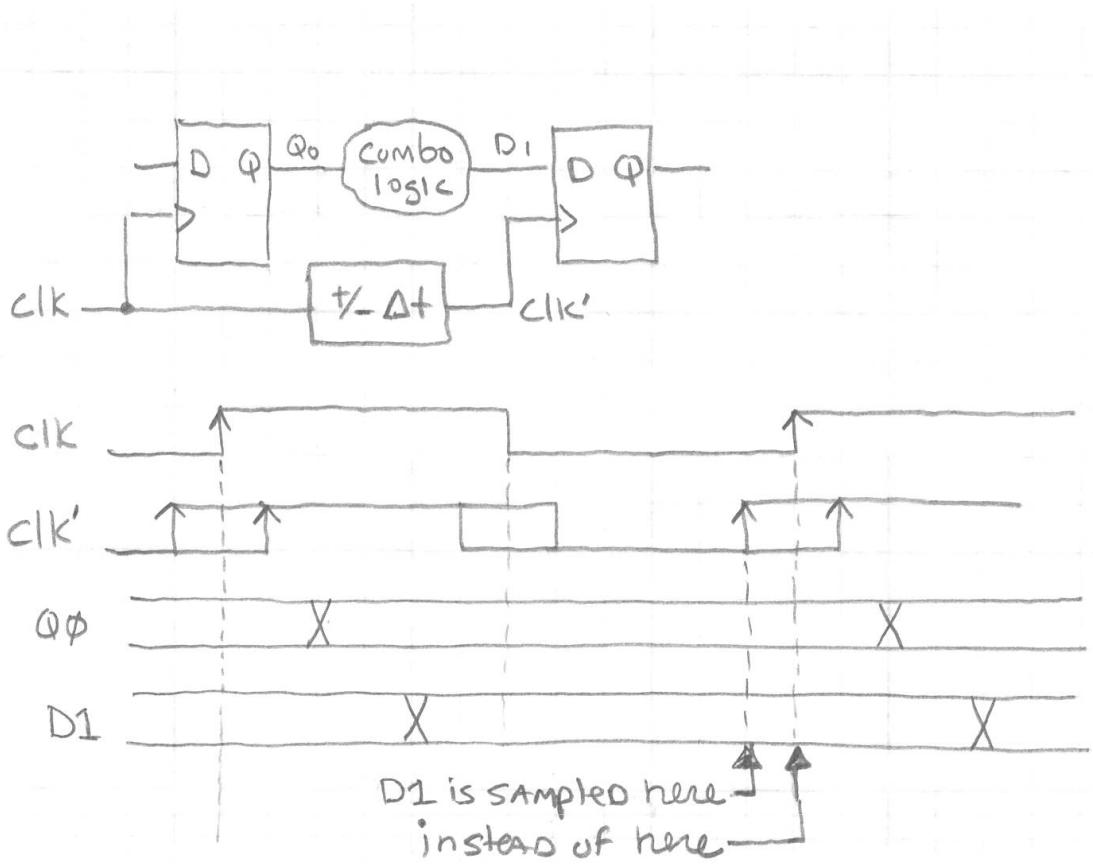
Review of Flip Flop Setup and Hold Time

- Imperfections in clock arrival time are called *clock skew*.
- If clock skew causes clock to arrive later at FF1 than FF0, data "leapfrogs" past FF1.



Review of Flip Flop Setup and Hold Time

- If clock skew casues clock to arrive earlier at FF1 than FF0, data has less time to reach FF1.
- This requires the clock period must be lengthened over what it could have been without skew.
- i.e., the system is slower.



Review of Flip Flop Setup and Hold Time

- The presence of skew simply takes away directly from any slack (setup or hold) that may exist.
- A more complete picture of setup and hold slack would be:
  - setup slack = (cycle_time - t_{ckq} - t_{pd} -t_{su}) - clock_skew
  - hold slack = (t_{ckq} + t_{pd} -t_h) - clock_skew
- We can get more setup slack by slowing down a system.
- There is nothing you can do to fix hold time slack after fabrication!