Short Quiz on Timers

Due Mar 6 at 2:35pm **Points** 20 **Questions** 20
Available Mar 6 at 2pm - Mar 6 at 2:35pm 35 minutes **Time Limit** 30 Minutes

Instructions

Choose the best answer from the choices.

This quiz was locked Mar 6 at 2:35pm.

Attempt History

	Attempt	Time	Score
LATEST	Attempt 1	16 minutes	16 out of 20

ⓘ Correct answers are hidden.

Score for this quiz: **16** out of 20
Submitted Mar 6 at 2:25pm
This attempt took 16 minutes.

Partial

Question 1 — 0.5 / 1 pts

Which of the following will happen when TMR1 = CCPR1 (match)?

- [ ] An overflow interrupt is generated.
- [ ] RC2 will be high, low or unchanged.
- [ ] RA0 will be high, low or unchanged.
- [x] Match interrupt is generated.

Question 2

1 / 1 pts

What is a prescaler?

- A ratio between oscillator frequency to the actual clock of the timer.
- None of the choices.
- A ratio of the source clock to the actual clock of the timer.
- A ration of the source clock to the instruction clock cycle.

Question 3

1 / 1 pts

What should be the value of PR2 if a 1000Hz signal is generated by the PWM module? Assume F_{OSC} = 4MHz and Timer2 prescaler value of 1:16.

- 61
- 15
- 62
- 250

Question 4

1 / 1 pts

Which of the following timers does not generate an interrupt upon overflow?

- Timer0

- CCP Module
- Timer2
- Timer1

Question 5

1 / 1 pts

Which of the following is true for the capture module?

- The value of TMR1 is copied to CCPRx when an event happens at RC2.
- The value of CCPRx is copied to Timer1 when an event happens at RC2.
- None of the choices.
- The value of Timer1 is compared to CCPRx when an event happens at RC2.

Incorrect

Question 6

0 / 1 pts

If the duty cycle of the output signal generated by the CCP module is 60% at 1000Hz, what should be the value for the CCP1CON<5:4>? Assume F_{OSC} = 4MHz and Timer2 prescaler value of 1:16.

- 00_2
- 10_2
- 01_2

- ◉ 11_2

Question 7

1 / 1 pts

What is the event when the timer transition from FFh to 00h?

- ○ Underflow
- ○ Interrupt
- ○ Event
- ◉ Overflow

Question 8

1 / 1 pts

Given an F_{OSC} of 4MHz and a prescaler of 1:8, what is the timeout of Timer1 from 0000h to FFFFh?

- ○ 0.2621 s
- ◉ 0.52423 s
- ○ 0.0262 s
- ○ 0.0524 s

Incorrect

Question 9

0 / 1 pts

If the duty cycle of the output signal generated by the CCP module is 60% at 1000Hz, what should be the value for the CCPR1L? Assume F_{OSC} = 4MHz and Timer2 prescaler value of 1:16.

- 00101100_2
- 00100101_2
- 10010110_2
- 00100101_2

Question 10

1 / 1 pts

Match the bits to its correct description.

TMR1IE	Timer1 interrupt enable
TMR2IF	Timer2 interrupt flag bit
TMR1ON	Timer1 enable bit
TMR1CS	Timer clock soure selec

Question 11

1 / 1 pts

When a capture event happens at RC2, which register the value of TMR1 is copied to?

- T1CON
- PR2
- TMR2
- CCPR1

Question 12

1 / 1 pts

True or False: When TMR2 = PR2, an interrupt will generated if enabled.

- True
- False

Question 13

1 / 1 pts

Match the registers to its correct description.

TMR1	Timer1 register
T1CON	Timer1 control register
CCP1CON	CCP1 control register
PR2	period register

Incorrect

Question 14

0 / 1 pts

What is the event when the timer transitions from 0000h to FFFFh?

- ○ Underflow
- ○ Match
- ◉ Overflow
- ○ Interrupt

Question 15

1 / 1 pts

Which of the following timers are count up?

- ☑ Timer1
- ☐ PR2
- ☑ Timer2
- ☑ Timer0

Question 16

1 / 1 pts

What is a duty cycle?

- ◉ The percentage of the period where the signal is 'high' or 'on'.

- The percentage of the period where the signal is 'low' or 'off'.
- The percentage of the frequency where the signal is 'high' or 'on'.
- The sum of the Ton and Toff.

Question 17

1 / 1 pts

Given an F_{OSC} of 4MHz and a prescaler of 1:4, what should be the value of PR2 if a match interrupt is generated every 2 ms?

- 750
- 1000
- (selected) None of the choices.
- 500

Partial

Question 18

0.5 / 1 pts

Which of the following registers are used for the PWM resolution?

- CCP2CON<5:4>
- (checked) CCP1CON<5:4>
- CCPR2L
- (checked) CCPR1L

Question 19

1 / 1 pts

Match the registers to its correct description.

TMR2ON	Timer2 enable bit
PEIE	Peripheral interrupt enal
TMR2IE	Timer2 interrupt enable
GIE	Global interrupt enable b

Question 20

1 / 1 pts

True or False: PEIE bit should be set '0' inorder for Timer1 and Timer2 interrupts to work.

- True
- False

Quiz Score: **16** out of 20