Short Quiz on Timers

Due Mar 6 at 2:35pm **Points** 20 **Questions** 20

Available Mar 6 at 2pm - Mar 6 at 2:35pm 35 minutes Time Limit 30 Minutes

Instructions

Choose the best answer from the choices.

This quiz was locked Mar 6 at 2:35pm.

Attempt History

	Attempt	Time	Score
LATEST	Attempt 1	16 minutes	16 out of 20

! Correct answers are hidden.

Score for this quiz: 16 out of 20

Submitted Mar 6 at 2:25pm

This attempt took 16 minutes.

Partial

Question 1	0.5 / 1 pts
Which of the following will happen when TMR1 = CCPR1 (ma	atch)?
An overflow interrupt is generated.	
RC2 will be high, low or unchanged.	
RA0 will be high, low or unchanged.	
Match interrupt is generated.	
Water interrupt is generated.	

Question 2	1 / 1 pts
What is a prescaler?	
A ratio between oscillator frequency to the actual clock of the till	mer.
None of the choices.	
A ratio of the source clock to the actual clock of the timer.	
A ration of the source clock to the instruction clock cycle.	

Question 3	1 / 1 pts
What should be the value of PR2 if a 1000Hz signal is generated PWM module? Assume F_{OSC} = 4MHz and Timer2 prescaler value.	•
© 61	
O 15	
O 62	
O 250	

Question 4	1 / 1 pts
Which of the following timers does not generate an interrupt upon overflow?	on
○ Timer0	

CCP Module		
Timer2		
Timer1		

Which of the following is true for the capture module? The value of TMR1 is copied to CCPRx when an event happens at RC2. The value of CCPRx is copied to Timer1 when an event happens at RC2. None of the choices. The value of Timer1 is compared to CCPRx when an event happens at RC2.

Incorrect

Question 6 0 / 1 pts

If the duty cycle of the output signal generated by the CCP module is 60% at 1000Hz, what should be the value for the CCP1CON<5:4>? Assume $F_{OSC} = 4M$ Hz and Timer2 prescaler value of 1:16.

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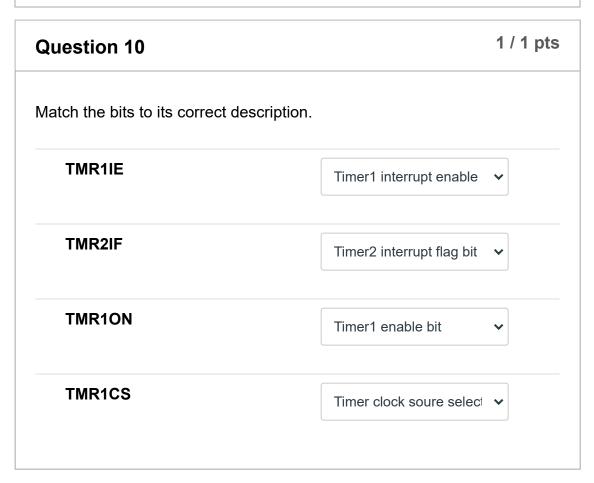
Question 7	1 / 1 pts
What is the event when the timer transition from FFh to 00h?	
Underflow	
Interrupt	
Event	
Overflow	

Question 8	1 / 1 pts
Given an F _{OSC} of 4MHz and a prescaler of 1:8, what is the time Timer1 from 0000h to FFFFh?	out of
○ 0.2621 s	
● 0.52423 s	
O.0262 s	
○ 0.0524 s	

Incorrect Question 9 0 / 1 pts

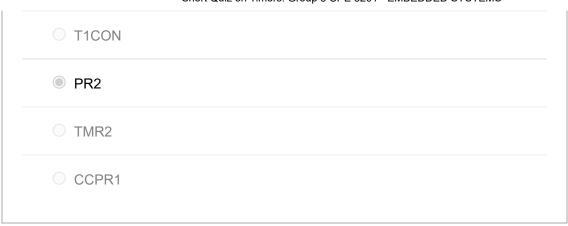
If the duty cycle of the output signal generated by the CCP module is 60% at 1000Hz, what should be the value for the CCPR1L? Assume F_{OSC} = 4MHz and Timer2 prescaler value of 1:16.

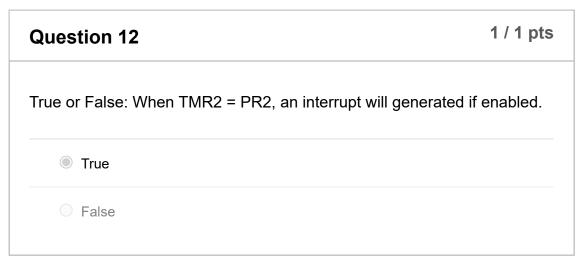
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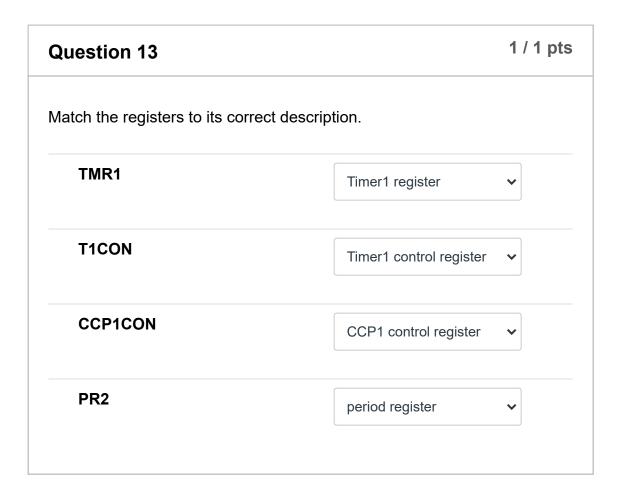


Question 11 1/1 pts

When a capture event happens at RC2, which register the value of TMR1 is copied to?







Incorrect

Question 14	0 / 1 pts
What is the event when the timer transitions from 0000h to FFF	Fh?
Underflow	
Match	
Overflow	
○ Interrupt	

Question 15	1 / 1 pts
Which of the following timers are count up?	
☑ Timer1	
PR2	
☑ Timer2	
☑ Timer0	

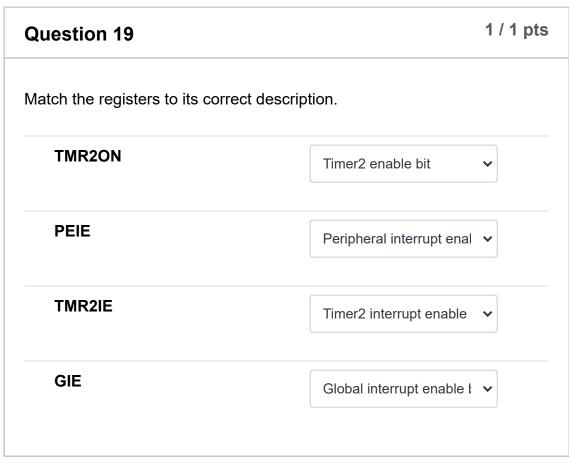
Question 16	1 / 1 pts
What is a duty cycle?	
The percentage of the period where the signal is 'high' or 'on'.	

	he percentage of the period where the signal is 'low' or 'off'.
О ТІ	ne percentage of the frequency where the signal is 'high' or 'on'.
ОТ	he sum of the Ton and Toff.

Given an F_{OSC} of 4MHz and a prescaler of 1:4, what should be the value of PR2 if a match interrupt is generated every 2 ms? 750 1000 None of the choices.

Partial

Which of the following registers are used for the PWM resolution? CCP2CON<5:4> CCP1CON<5:4> CCPR2L CCPR1L



Question 20	1 / 1 pts
True or False: PEIE bit should be set '0' inorder for Timer1 and interrupts to work.	d Timer2
O True	
False	

Quiz Score: 16 out of 20