



University of San Carlos | Department of
COMPUTER ENGINEERING

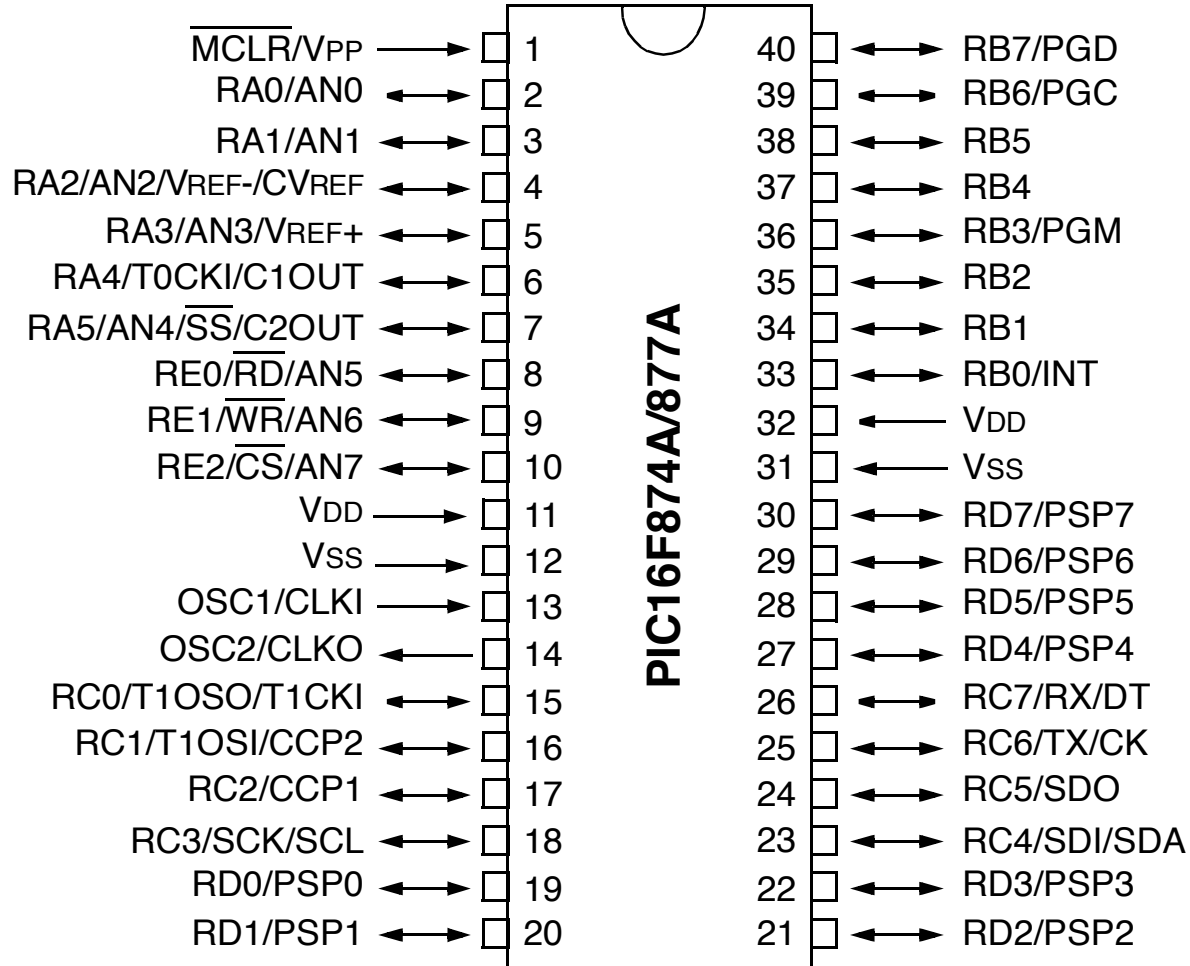
CpE 3201
Embedded Systems

Introduction to Embedded Systems

About PIC16F877A

- Mid-range 8-bit MCU from Microchip
- Shares the same architecture as PIC16F84A as well as other MCU in the PIC16FXX series
- Has a larger program memory about 8x the one in the PIC16F84A
- More I/O ports which is deal for multiple I/O interfacing

40-Pin PDIP



High Performance RISC CPU

- Only 35 single - word instructions to learn
- All single - cycle instructions except for program branches, which are two-cycle
- Operating speed: DC – 20M Hz clock input
DC – 200 ns instruction cycle
- Up to 8K x 14 words of Flash Program Memory,
Up to 368 x 8 bytes of Data Memory (RAM), Up to 256
x 8 bytes of EEPROM Data Memory
- Pinout compatible to other 28-pin or 40/44-pin
PIC16CXXX and PIC16FXXX microcontrollers

Peripheral Features

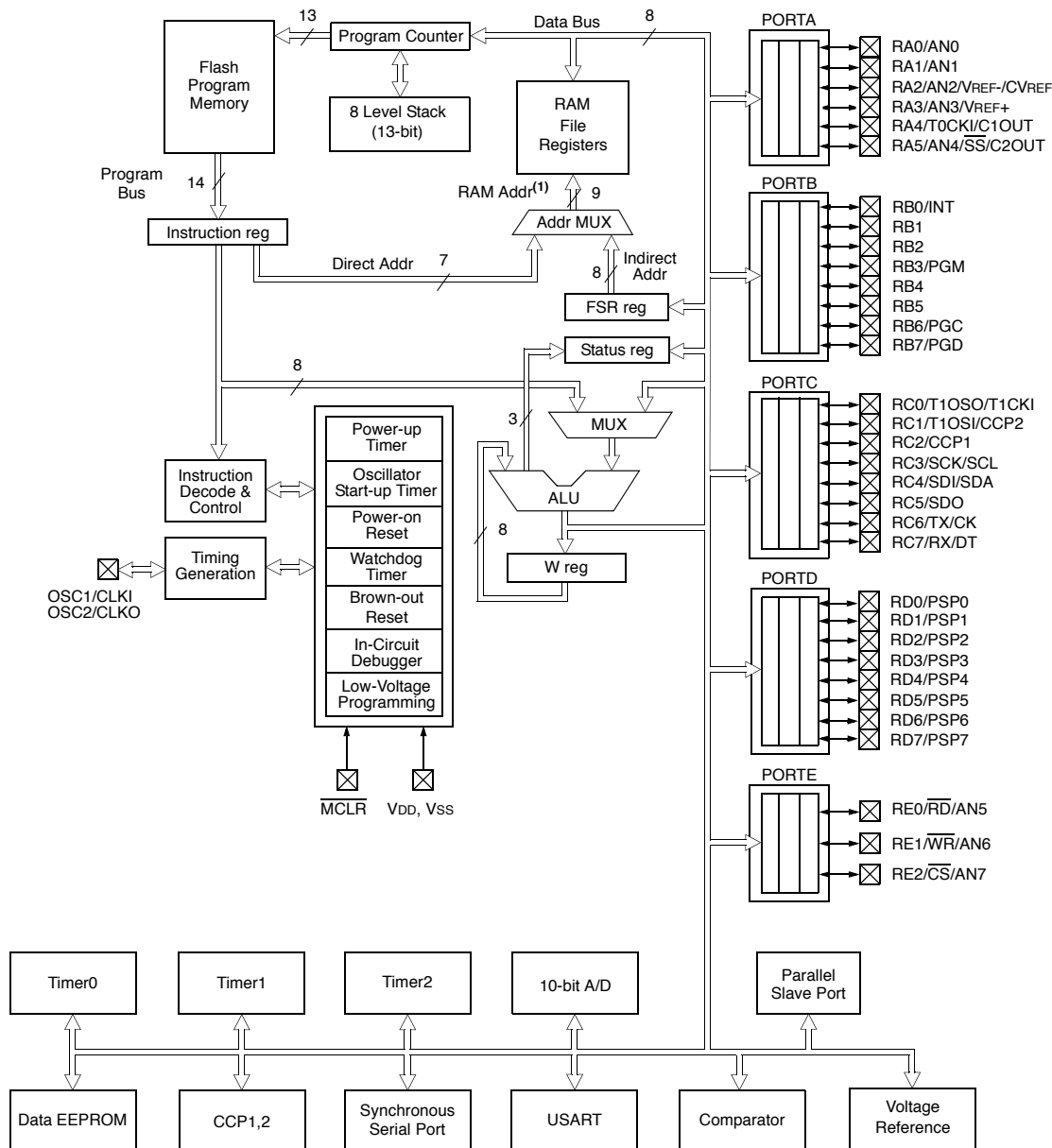
- **Timer0:** 8-bit timer/counter with 8-bit prescaler
- **Timer1:** 16-bit timer/counter with prescaler, can be incremented during Sleep via external crystal/clock
- **Timer2:** 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules (CCP)
 - Capture is 16-bit, max. resolution is 12.5 ns
 - Compare is 16-bit, max. resolution is 200 ns
 - PWM max. resolution is 10-bit

Peripheral Features

- Synchronous Serial Port (SSP) with SPI™ (Master mode) and I2C™ (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection
- Parallel Slave Port (PSP) – 8 bits wide with external RD, WR and CS controls (40/44-pin only)
- Brown-out detection circuitry for Brown-out Reset (BOR)

Analog Features

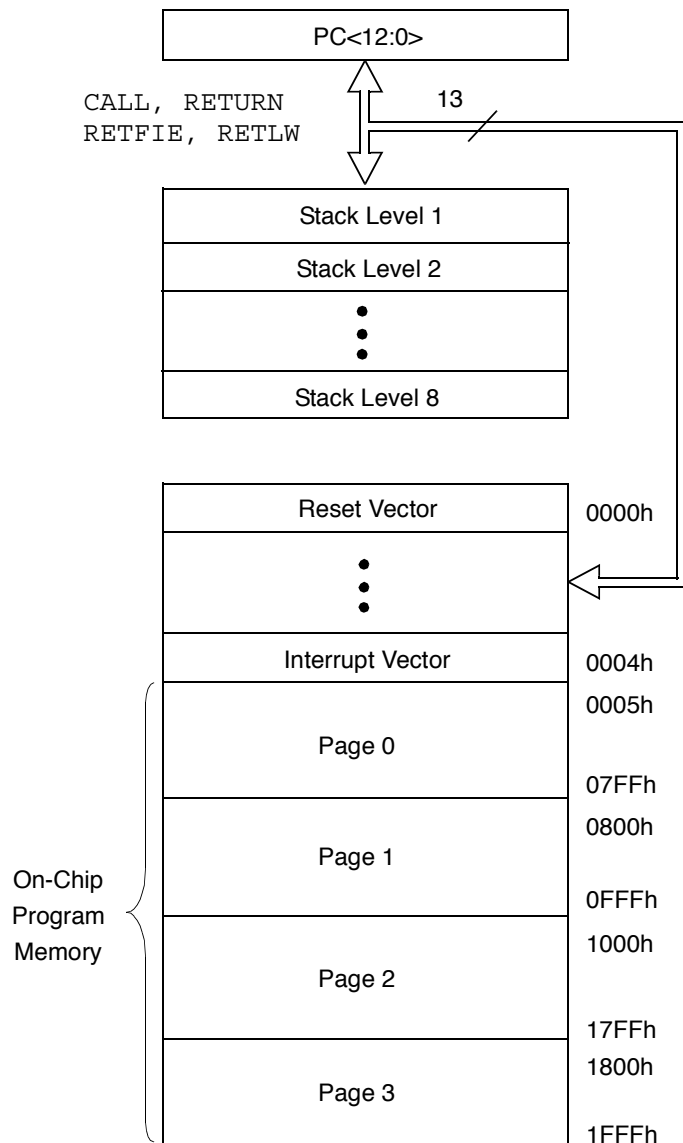
- 10-bit, up to 8-channel Analog-to-Digital Converter (A/D)
- Brown-out Reset (BOR)
- Analog Comparator module with:
 - Two analog comparators
 - Programmable on-chip voltage reference (VREF) module
 - Programmable input multiplexing from device inputs and internal voltage reference
 - Comparator outputs are externally accessible



Block Diagram of PIC16F87xx

Memory Organization

- There are three memory blocks in each of the PIC16F87XA devices
- The program memory and data memory have separate buses so that concurrent access can occur



Program Memory Map & Stack

Data Memory Organization

- The data memory is partitioned into multiple banks which contain the General Purpose Registers and the Special Function Registers. Bits RP1 (Status<6>) and RP0 (Status<5>) are the bank select bits.

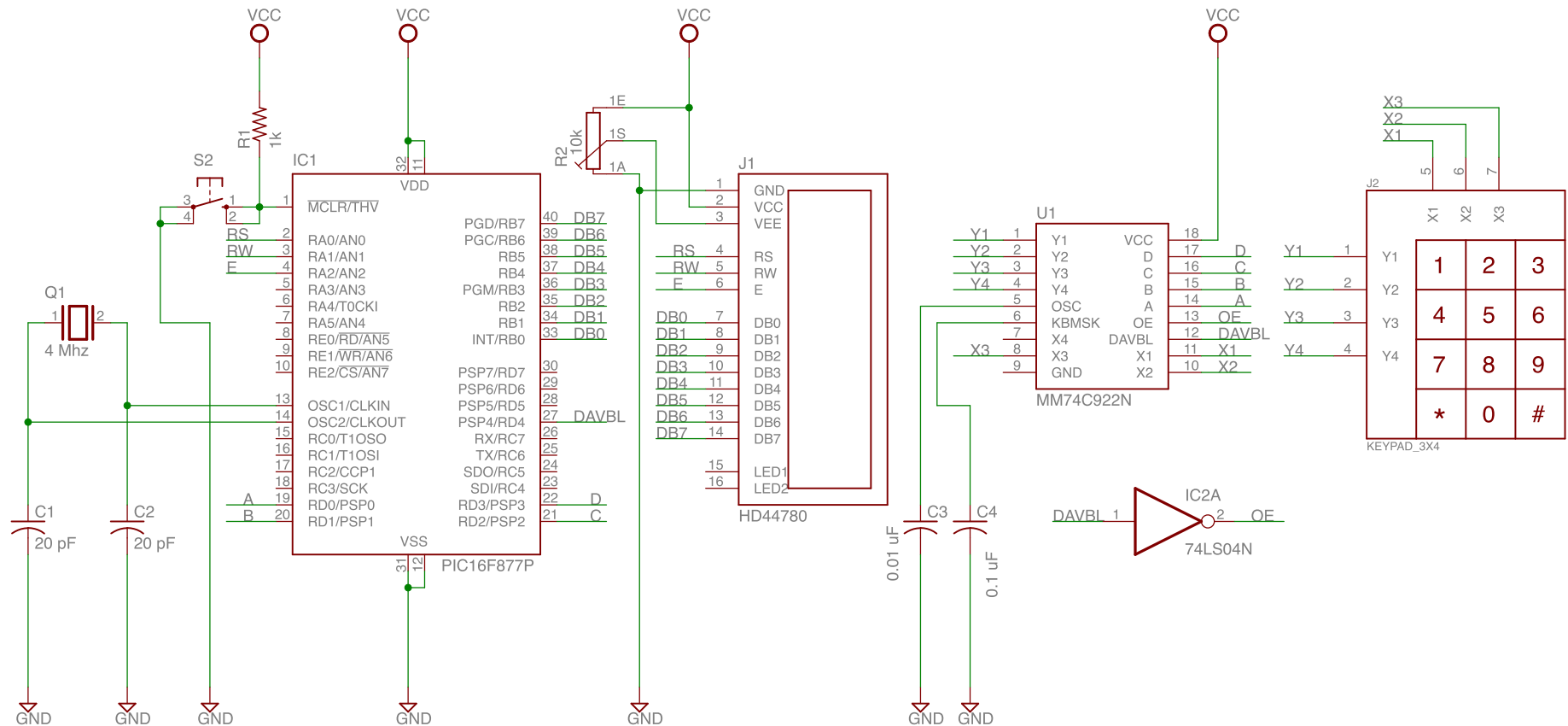
RP1:RP0	Bank
00	0
01	1
10	2
11	3

File Address		File Address		File Address		File Address	
Indirect addr. ^(*)	00h	Indirect addr. ^(*)	80h	Indirect addr. ^(*)	100h	Indirect addr. ^(*)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h		107h		187h
PORTD ⁽¹⁾	08h	TRISD ⁽¹⁾	88h		108h		188h
PORTE ⁽¹⁾	09h	TRISE ⁽¹⁾	89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDATA	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved ⁽²⁾	18Eh
TMR1H	0Fh		8Fh	EEADRH	10Fh	Reserved ⁽²⁾	18Fh
T1CON	10h		90h	General Purpose Register 16 Bytes	110h	General Purpose Register 16 Bytes	190h
TMR2	11h	SSPCON2	91h		111h		191h
T2CON	12h	PR2	92h		112h		192h
SSPBUF	13h	SSPADDD	93h		113h		193h
SSPCON	14h	SSPSTAT	94h		114h		194h
CCPR1L	15h		95h		115h		195h
CCPR1H	16h		96h		116h		196h
CCP1CON	17h		97h		117h		197h
RCSTA	18h	TXSTA	98h		118h		198h
TXREG	19h	SPBRG	99h		119h		199h
RCREG	1Ah		9Ah		11Ah		19Ah
CCPR2L	1Bh		9Bh		11Bh		19Bh
CCPR2H	1Ch	CMCON	9Ch		11Ch		19Ch
CCP2CON	1Dh	CVRCON	9Dh		11Dh		19Dh
ADRESH	1Eh	ADRESL	9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
General Purpose Register 96 Bytes	20h	General Purpose Register 80 Bytes	A0h	General Purpose Register 80 Bytes	120h	General Purpose Register 80 Bytes	1A0h
			EFh		16Fh		1EFh
			F0h		170h		1F0h
		accesses 70h-7Fh		accesses 70h-7Fh		accesses 70h - 7Fh	
Bank 0	7Fh	Bank 1	FFh	Bank 2	17Fh	Bank 3	1FFh

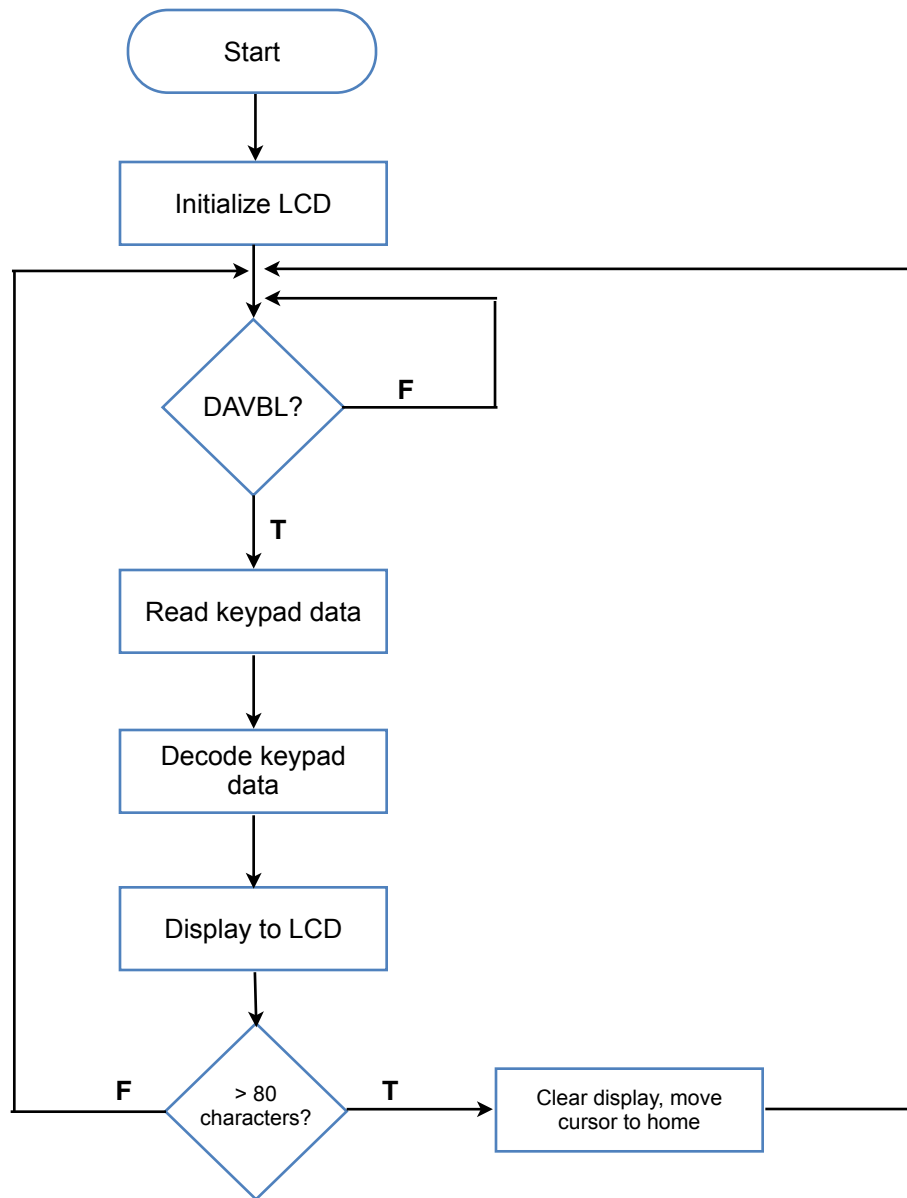
Register File Map of PIC16F87xx

Design Example

- An 5x7-dot LCD and a 3x4 numeric keypad is interfaced to the PIC16F877A MCU. The LCD will display the key pressed to LCD. Once the display is full, the display automatically clears and moves the cursor to the home position and continues.



PIC16F877A interfaced with LCD and keypad



Super loop solution to problem

C programming

LCD Functions

```
void Inst_Ctrl (unsigned char INST)
{
    PORTB = INST;           // load instruction to PORTB
    RA0 = 0;                // set RS to 0 (instruction reg)
    RA1 = 0;                // set RW to 0 (write)
    RA2 = 1;                // set E to 1
    delay(1);               // 1 ms delay (estimate)
    RA2 = 0;                // set E to 0 (strobe)
}
```


C programming

LCD Functions

```
void Data_Ctrl (unsigned char DATA)
{
    PORTB = DATA;           // load data to PORTB
    RA0 = 1;                 // set RS to 1 (data reg)
    RA1 = 0;                 // set RW to 0 (write)
    RA2 = 1;                 // set E to 1
    delay(1);                // 1 ms delay (estimate)
    RA2 = 0;                 // set E to 0 (strobe)
}
```

C programming

Delay Function

```
void delay (unsigned char MUL)
{
    unsigned char i,j;

    for (i=MUL; i != 0; i--)           // loop until i = 0
        for (j=0; j < 256; j++);      // loop until j = 0
}
```

* Approximate delay method. Adjust inner loop if necessary



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End of Lecture

References:

- PIC16F87XA Datasheet, Microchip Technology Inc., 2003.
- Ramesh S. Gaonkar. Fundamentals of Microcontrollers and Applications in Embedded Systems. Thomson Delmar Learning, 2007.