اعضای گروه : زهرا کمالی - دانیال ریاضتی

گزارش تمرین ۴ :

میخواهیم یک ضرب کننده n بیتی را با for generate بسازیم.

نیاز به یک ماژول full adder داریم.

```
--piade sazi fulladder
ENTITY F_Adder IS
    PORT( cin: IN std_logic;
          x: IN std_logic;
          y: IN std_logic;
          cout : OUT std_logic;
          s : OUT std_logic
    );
END F_Adder;

ARCHITECTURE fa OF F_Adder IS
BEGIN
    cout <= (x AND y) or (x AND cin) or (y AND cin);
    s <= x XOR y XOR cin;
END fa;
```

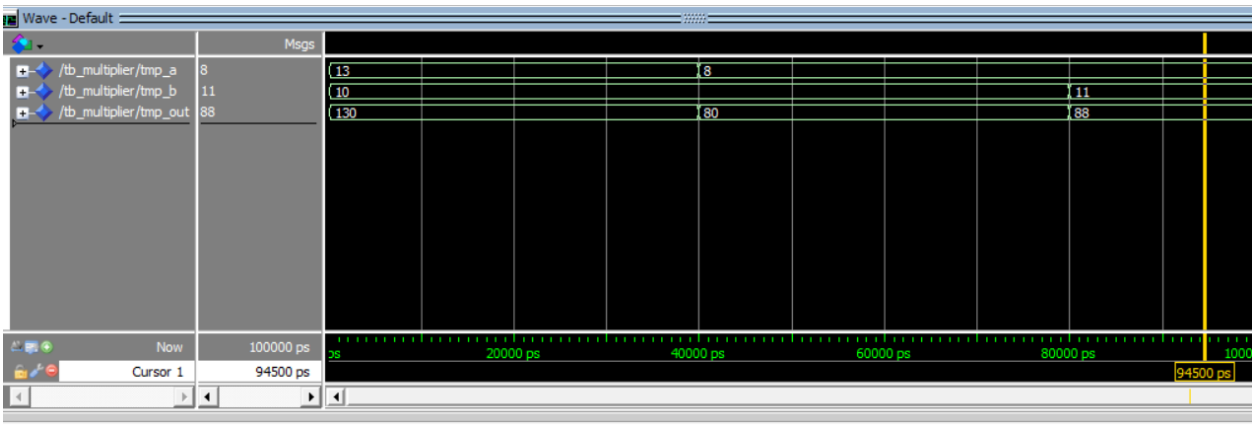
پورت های multiplier :

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY Multiplier IS
    GENERIC (SIZE: INTEGER:= 8);
    PORT (A: IN std_logic_vector (SIZE-1 DOWNTO 0);
          B: IN std_logic_vector (SIZE-1 DOWNTO 0);
          mult_out: OUT std_logic_vector (2*SIZE-1 DOWNTO 0)
    );
END Multiplier;
```

تست بنچ:

```
-- tb for mult

LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
use ieee.std_logic_arith.all;

ENTITY tb_Multiplier IS
 generic (SIZE: INTEGER:= 4);
END tb_Multiplier;

ARCHITECTURE tb OF tb_Multiplier IS
 COMPONENT Multiplier
 generic (SIZE: INTEGER:= 4);

 PORT(

        A :          IN  std_logic_vector(SIZE-1 DOWNTO 0);
        B :          IN  std_logic_vector(SIZE-1 DOWNTO 0);
        mult_out :   OUT std_logic_vector(2*SIZE-1 DOWNTO 0)

 );

 END COMPONENT;

 SIGNAL tmp_a : std_logic_vector(SIZE-1 DOWNTO 0) := (others => '0');
 SIGNAL tmp_b : std_logic_vector(SIZE-1 DOWNTO 0) := (others => '0');
 SIGNAL tmp_out : std_logic_vector(2*SIZE-1 DOWNTO 0);

BEGIN
    Mult1: Multiplier GENERIC MAP(4) PORT MAP(A=>tmp_a,B=>tmp_b,mult_out=>tmp_out);
    -- input 13 and 8 for a
    tmp_a <= X"D" , X"8" after 40 ns;

    -- input 10 and 11 for b
    tmp_b <= X"A" , X"B" after 80 ns;


END tb;
```

شبیه سازی:


Wave - Default
Msgs
/tb_multiplier/tmp_a
/tb_multiplier/tmp_b
/tb_multiplier/tmp_out
8
11
88
13
8
10
11
130
80
88
Now
100000 ps
Cursor 1
94500 ps
20000 ps
40000 ps
60000 ps
80000 ps
94500 ps