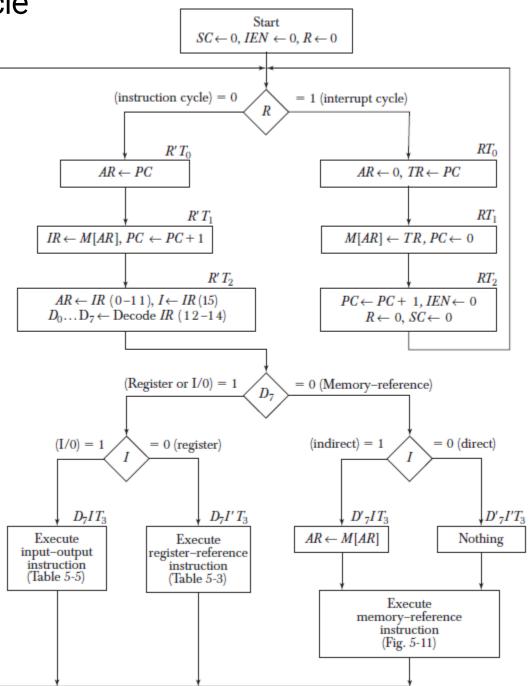
طراحی واحد کنترل کامپیوتر پایه

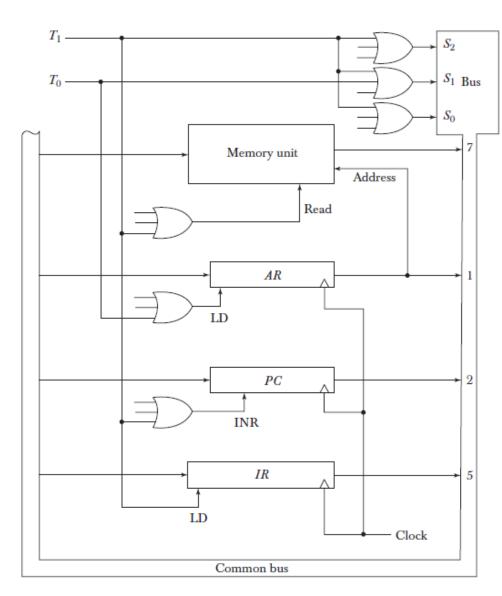
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Instruction Cycle



Fetch



$$R' T_0$$
: $AR \leftarrow PC$

- 1. Place the content of PC onto the bus by making the bus selection inputs $S_2S_1S_0$ equal to 010.
- 2. Transfer the content of the bus to AR by enabling the LD input of AR.

$$R'T_1$$
: $IR \leftarrow M[AR], PC \leftarrow PC + 1$

- 1. Enable the read input of memory.
- 2. Place the content of memory onto the bus by making $S_2S_1S_0 = 111$.
- 3. Transfer the content of the bus to IR by enabling the LD input of IR.
- 4. Increment PC by enabling the INR input of PC.

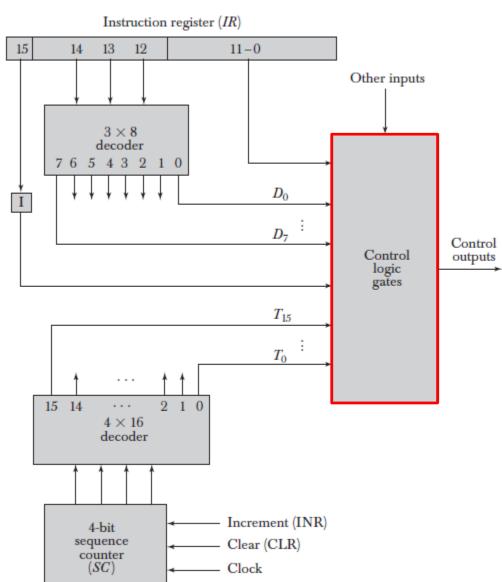
Control unit of basic computer

Inputs

- From two decoders, the I flip-flop, and bits 0 through 11 of IR.
- The other inputs to the control logic are: AC bits 0 through 15 to check if AC=0 and to detect the sign bit in AC(15); DR bits 0 through 15 to check if DR=0; and the values of the seven flip-flops

Outputs

- Signals to control the inputs of the nine registers
- Signals to control the read and write inputs of memory
- Signals to set, clear, or complement the flip-flops
- Signals for S2, S1, and S0 to select a register for the bus
- Signals to control the AC adder and logic circuit



$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		ontroi runctions and	1 Microoperations for the basic Computer
Decode RT_i : $D_c \leftarrow M[AR]$, $PC \leftarrow PC + 1$ $D_c \leftarrow, D_f \leftarrow Decode R(12-14)$, $AR \leftarrow IR(0-11)$. $I \leftarrow IR(15)$ Indirect $D_f T_i^c$: $AR \leftarrow M[AR]$ Interrupt: $T_c T_i^c T_i^c (IEN)(FGI + FGO)$: $R \leftarrow 1$ $RT_i^c \rightarrow RT_i^c \rightarrow$	P-t-l-	D'T.	AB . BC
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	retch	•	
Indirect $D_r^*IT_3$: $AR \leftarrow IR(b-11)$. $I \leftarrow IR(15)$ Interrupt: $T_0T_1^*T_2^*(IEN)[FGI + FGO]$: $R \leftarrow 1$ RT_3 : $AR \leftarrow 0$, $TR \leftarrow PC$ RT_3 : $AR \leftarrow 0$, $TR \leftarrow PC$ RT_3 : $M[AR] \leftarrow TR$, $PC \leftarrow 0$ RT_2 : $PC \leftarrow PC + 1$, $IEN \leftarrow 0$, $R \leftarrow 0$, $SC \leftarrow 0$ Memory-reference: AND D_0T_4 : $DR \leftarrow M[AR]$ D_1T_4 : $DR \leftarrow M[AR] \leftarrow PC$, $AR \leftarrow AR \leftarrow AR \leftarrow 1$ D_1T_4 : $DR \leftarrow M[AR] \leftarrow PC$, $AR \leftarrow AR \leftarrow 1$ D_1T_4 : $DR \leftarrow M[AR] \leftarrow PC$, $AR \leftarrow AR \leftarrow 1$ D_1T_4 : $DR \leftarrow M[AR] \leftarrow PC$, $AR \leftarrow AR \leftarrow 1$ D_1T_4 : $DR \leftarrow M[AR] \leftarrow DR$, if $(DR = 0)$ then $(PC \leftarrow PC + 1)$, $SC \leftarrow 0$ Register-reference: $D_1T_3 = r$ (common to all register-reference instruct ions $IR(0) = B_1$ ($i = 0, 1, 2,, 11$) $r: SC \leftarrow 0$ CLA rB_{11} : $AC \leftarrow 0$ CLA rB_{12} : $AC \leftarrow SA$	Dd.		
Interrupt: $R \leftarrow M[AR]$ Interrupt: $R \leftarrow M[AR]$ Interrupt: $R \leftarrow M[AR]$ $R \leftarrow M[A$	Decode	KI_2 :	
Interrupt: $T_0T_1^*T_2^*(IEN)(FGI + FGO)$: R_0^* : $AR \leftarrow 0$, $TR \leftarrow PC$ RT_1^* : $M[AR] \leftarrow TR$, $PC \leftarrow 0$ RT_2^* : $PC \leftarrow PC + 1$, $IEN \leftarrow 0$, $R \leftarrow 0$, $SC \leftarrow 0$ Memory-reference: AND $D_0T_2^*$: $DR \leftarrow M[AR]$ $D_1T_2^*$: $DR \leftarrow M[AR]$ $D_2T_2^*$: $AC \leftarrow AC + DR$, $E \leftarrow C_{out} \rightarrow SC \leftarrow 0$ LDA $D_1T_2^*$: $DR \leftarrow M[AR]$ $DR \leftarrow $	Indiana	D'IT.	
$ T_0T_1'T_2'(lEN)(FGI + FGO): RT_0: RX_0 - RX_0 -$	_	$D_7 II_3$:	$AK \leftarrow M[AK]$
$ RT_0: RT_1: M[AR] \leftarrow TR, \ PC \leftarrow 0 \\ RT_2: PC \leftarrow PC + 1, \ IEN \leftarrow 0, \ R \leftarrow 0, \ SC \leftarrow 0 \\ RT_2: PC \leftarrow PC + 1, \ IEN \leftarrow 0, \ R \leftarrow 0, \ SC \leftarrow 0 \\ Memory-reference: \\ AND $		ECO.	D . 1
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	$I_0I_1I_2$ (IEIV)(FGI $+$	*	
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$			•
$\begin{array}{cccccccccccccccccccccccccccccccccccc$			
AND $D_0T_4\colon D_0T_5\colon AC\leftarrow M/AR $ $D_0T_5\colon AC\leftarrow AC \land DR, SC\rightarrow 0$ ADD $D_1T_4\colon DR\leftarrow M AR $ $D_1T_5\colon AC\leftarrow AC \land DR, E\leftarrow C_{out}\rightarrow SC\leftarrow 0$ LDA $D_2T_5\colon AC\leftarrow AC, DR, SC\rightarrow 0$ STA $D_2T_5\colon AC\leftarrow DR, SC\rightarrow 0$ STA $D_2T_5\colon AC\leftarrow DR, SC\rightarrow 0$ BUN $D_4T_4\colon PC\leftarrow AR, SC\leftarrow 0$ BSA $D_5T_4\colon M AR \rightarrow PC, AR\leftarrow AR+1$ $D_5T_5\colon PC\leftarrow AR, SC\leftarrow 0$ ISZ $D_6T_4\colon DR\leftarrow M AR $ $D_6T_6\colon AR, SC\rightarrow 0$ Register-reference: $D_2TT_3=r \text{ (common to all register-reference instruct ions } RR(i)=R_i (i=0,1,2,\ldots,11)$ $r\colon SC\leftarrow 0$ CLA $rB_{11}\colon AC\leftarrow 0$ CLE $rB_{20}\colon E\leftarrow 0$ CMA $rB_{21}\colon AC\leftarrow AC$ CME $rB_{31}\colon AC\leftarrow AC$ CME $rB_{51}\colon AC\leftarrow AC$ CIIL $rB_{51}\colon AC\leftarrow AC$ CIIL $rB_{51}\colon AC\leftarrow AC$ CIIL $rB_{51}\colon AC\leftarrow AC+1$ SPA $rB_4\colon AC\leftarrow AC+1$ SPA $rB_4\colon AC\leftarrow AC+1$ SPA $rB_4\colon AC\leftarrow AC+1$ SPA $rB_4\colon AC\leftarrow AC+1$ SPA $rB_5\colon AC\leftarrow AC+1$	Memory-reference:	112.	$FC \leftarrow FC + 1$, $FEN \leftarrow 0$, $R \leftarrow 0$, $BC \leftarrow 0$
ADD $D_0 T_i: DR \leftarrow M[AR]$ $D_1 T_i: DR \leftarrow M[AR]$ $D_1 T_i: DR \leftarrow M[AR]$ $D_2 T_i: DR \leftarrow M[AR]$ $D_3 T_i: DR \leftarrow M[AR]$ $D_4 T_i: DR \leftarrow M[AR]$ $D_5 T_i: DR \leftarrow M[AR] \leftarrow AC, SC \leftarrow 0$ $D_6 T_6: M[AR] \leftarrow BC, AR \leftarrow AR + 1$ $D_6 T_6: DR \leftarrow M[AR]$ $D_6 T_6: DR \leftarrow M[AR]$ $D_6 T_6: DR \leftarrow DR + 1$ $D_6 T_6: DR \leftarrow DR + 1$ $D_6 T_6: DR \leftarrow DR + 1$ $D_6 T_6: M[AR] \leftarrow DR, \text{ if } (DR = 0) \text{ then } (PC \leftarrow PC + 1), SC \leftarrow 0$ $D_7 T_3 = r \text{ (common to all register-reference instruct ions } IR(i) = B_i (i = 0, 1, 2,, 11)$ $r: SC \leftarrow 0$ $CLA \qquad tB_{11}: AC \leftarrow 0$ $CLE \qquad tB_{16}: AC \leftarrow AC$ $CLE \qquad tB_{16}: AC \leftarrow AC$ $CMA \qquad tB_{5}: AC \leftarrow AC$ $CME \qquad tB_{5}: AC \leftarrow AC$ $CIL \qquad tB_{6}: AC \leftarrow Shl AC, AC (15) \leftarrow E, E \leftarrow AC (0)$ $CIL \qquad tB_{6}: AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15)$ $INC \qquad tB_{5}: AC \leftarrow AC + 1$ $SNA \qquad tB_{5}: If (AC (15) - 0) \text{ then } (PC \leftarrow PC + 1)$ $SNA \qquad tB_{5}: If (AC (15) - 0) \text{ then } (PC \leftarrow PC + 1)$ $SZA \qquad tB_{5}: If (AC (15) - 0) \text{ then } (PC \leftarrow PC + 1)$ $SZA \qquad tB_{5}: If (AC (15) - 1) \text{ then } (PC \leftarrow PC + 1)$ $Input-output: D_7 T_3 = p \text{ (common to all input-output instructions)}$ $IR(i) = B_i (i = 6, 7, 8, 9, 10, 11)$ $p: SC \leftarrow 0$ $INP \qquad pB_{11}: AC (0 - 7) \leftarrow INPR, FGI \leftarrow 0$ $OUT \qquad pB_{20}: OUTR \leftarrow AC (0 - 7), FGO \leftarrow 0$ $SKI \qquad pB_{5}: If (FGO - 1) \text{ then } (PC \leftarrow PC + 1)$ $SKO \qquad pB_{5}: If (FGO - 1) \text{ then } (PC \leftarrow PC + 1)$ $IEN \leftarrow 1$		D.T.	$DD \leftarrow M(AD)$
ADD $D_1T_i: DR \leftarrow M[AR]$ $D_1T_i: AC \leftarrow AC + DR, E \leftarrow C_{out} \rightarrow SC \leftarrow 0$ $D_2T_i: DR \leftarrow M[AR]$ $D_2T_i: DR \leftarrow M[AR]$ $D_2T_i: DR \leftarrow M[AR]$ $D_2T_i: DR \leftarrow M[AR] \leftarrow AC, SC \leftarrow 0$ $D_3T_i: M[AR] \leftarrow AC, SC \leftarrow 0$ $D_3T_i: M[AR] \leftarrow PC, AR \leftarrow AR + 1$ $D_2T_i: PC \leftarrow AR, SC \leftarrow 0$ $D_2T_i: DR \leftarrow M[AR]$ $D_2T_i: DR \leftarrow M[AR]$ $D_2T_i: DR \leftarrow DR + 1$ $D_2T_i: DR \leftarrow DR $	AND		
LDA $D_1T_i: DR \leftarrow M AR $ $D_2T_i: DR \leftarrow M AR $ $D_2T_i: AC \leftarrow DR, SC \leftarrow 0$ STA $D_3T_i: M AR \leftarrow AC, SC \leftarrow 0$ BUN $D_4T_i: PC \leftarrow AR, SC \leftarrow 0$ BSA $D_5T_i: M AR \leftarrow PC, AR \leftarrow AR + 1$ $D_5T_i: PC \leftarrow AR, SC \leftarrow 0$ BSA $D_5T_i: PC \leftarrow AR, SC \leftarrow 0$ ISZ $D_6T_i: DR \leftarrow M AR $ $D_6T_6: DR \leftarrow DR + 1$ $D_6T_6: M AR \leftarrow DR, \text{ if } (DR = 0) \text{ then } (PC \leftarrow PC + 1), SC \leftarrow 0$ Register-reference: $D_2TT_3 = r \text{ (common to all register-reference instruct ions } RR(i) = B_i (i = 0, 1, 2,, 11)$ $r: SC \leftarrow 0$ CLA $rB_{1i}: AC \leftarrow 0$ CLE $rB_{2i}: E \leftarrow 0$ CMA $rB_{3i}: E \leftarrow 0$ CMA $rB_{3i}: E \leftarrow \overline{E}$ CIR $rB_{5i}: AC \leftarrow AC$ CME $rB_{5i}: AC \leftarrow AC$ CIL $rB_{6i}: AC \leftarrow Shr AC, AC (15) \leftarrow E, E \leftarrow AC (0)$ CIL $rB_{6i}: AC \leftarrow Shr AC, AC (0) \leftarrow E, E \leftarrow AC (15)$ INC $rB_{5i}: AC \leftarrow AC + 1$ SPA $rB_{5i}: If (AC (15) = 0) \text{ then } (PC \leftarrow PC + 1)$ SNA $rB_{5i}: If (AC (15) = 1) \text{ then } (PC \leftarrow PC + 1)$ SNA $rB_{5i}: If (AC (15) = 1) \text{ then } (PC \leftarrow PC + 1)$ INP $D_2TT_3 = p \text{ (common to all input-output instructions)}$ $R(i) = B_{5i}: If (E = 0) \text{ then } (PC \leftarrow PC \leftarrow PC + 1)$ INP $D_2TT_3 = p \text{ (common to all input-output instructions)}$ $R(i) = B_{5i}: If (E = 0) \text{ then } (PC \leftarrow PC \leftarrow PC + 1)$ SSZE $rB_{1i}: If (E = 0) \text{ then } (PC \leftarrow PC $	ADD		
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	ADD		
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	LDA		true.
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	LDA		
BUN $D_{i}T_{i}^{+}$: $PC \leftarrow AR$, $SC \leftarrow 0$ BSA $D_{5}T_{i}$: $M[AR] \leftarrow PC$, $AR \leftarrow AR + 1$ $D_{i}T_{5}^{+}$: $PC \leftarrow AR$, $SC \leftarrow 0$ ISZ $D_{6}T_{i}^{+}$: $DR \leftarrow M[AR]$ $D_{6}T_{5}^{+}$: $DR \leftarrow DR + 1$ $D_{6}T_{5}^{+}$: $DR \leftarrow DR + 1$ $D_{6}T_{6}^{+}$: $M[AR] \leftarrow DR$, if $(DR = 0)$ then $(PC \leftarrow PC + 1)$, $SC \leftarrow 0$ Register-reference: $\begin{array}{ccccccccccccccccccccccccccccccccccc$	STA		-
$\begin{array}{cccccccccccccccccccccccccccccccccccc$			
ISZ $D_5T_5: PC \leftarrow AR, SC \leftarrow 0$ $D_5T_5: DR \leftarrow M[AR]$ $D_6T_6: DR \leftarrow DR + 1$ $D_5T_6: M[AR] \leftarrow DR, \text{ if } (DR = 0) \text{ then } (PC \leftarrow PC + 1), SC \leftarrow 0$ Register-reference: $D_7I'T_3 = r \text{ (common to all register-reference instruct ions } IR(i) = B_i (i = 0, 1, 2, \dots, 11)$ $r: SC \leftarrow 0$ $CLA \qquad rB_{11}: AC \leftarrow 0$ $CLE \qquad tB_{20}: E \leftarrow 0$ $CMA \qquad tB_{2}: AC \leftarrow AC$ $CME \qquad tB_{3}: E \leftarrow \overline{E}$ $CIR \qquad tB_{5}: AC \leftarrow Shr AC, AC (15) \leftarrow E, E \leftarrow AC (0)$ $CIL \qquad tB_{5}: AC \leftarrow Shr AC, AC (0) \leftarrow E, E \leftarrow AC (15)$ $INC \qquad tB_{5}: AC \leftarrow AC + 1$ $SPA \qquad tB_{6}: AC \leftarrow Shr AC, AC (15) \leftarrow D, E \leftarrow C (15)$ $INC \qquad tB_{5}: AC \leftarrow AC + 1$ $SNA \qquad tB_{2}: If (AC (15) = 0) \text{ then } (PC \leftarrow PC + 1)$ $SNA \qquad tB_{3}: If (AC (15) = 1) \text{ then } (PC \leftarrow PC + 1)$ $SZA \qquad tB_{2}: If (AC = 0) \text{ then } PC \leftarrow PC + 1$ $INT \qquad tB_{0}: S \leftarrow 0$ $INP \qquad D_7IT_3 = p \text{ (common to all input-output instructions)}$ $IR(i) = B_i (i = 6, 7, 8, 9, 10, 11)$ $p: SC \leftarrow 0$ $OUT \qquad pB_{20}: OUTR \leftarrow AC (0 - 7), FGO \leftarrow 0$ $SKI \qquad pB_{2}: If (FGI - 1) \text{ then } (PC \leftarrow PC + 1)$ $SKO \qquad pB_{2}: If (FGO - 1) \text{ then } (PC \leftarrow PC + 1)$ $IEN \leftarrow 1$			
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	DOA		
$D_{6}T_{5}: \qquad DR \leftarrow DR + 1 \\ D_{6}T_{6}: \qquad M[AR] \leftarrow DR, \text{if } (DR = 0) \text{ then } \\ (PC \leftarrow PC + 1), SC \leftarrow 0$ Register-reference: $D_{7}FT_{3} = r \text{ (common to all register-reference instruct ions } \\ IR(i) = B_{i} (i = 0, 1, 2, \dots, 11)$ $r: \qquad SC \leftarrow 0$ $CLA \qquad rB_{11}: \qquad AC \leftarrow 0$ $CLE \qquad rB_{20}: \qquad E \leftarrow 0$ $CMA \qquad rB_{2}: \qquad AC \leftarrow AC$ $CME \qquad rB_{8}: \qquad E \leftarrow \overline{E}$ $CIR \qquad rB_{7}: \qquad AC \leftarrow \text{shr } AC, AC(15) \leftarrow E, E \leftarrow AC(0)$ $CIL \qquad rB_{6}: \qquad AC \leftarrow \text{shr } AC, AC(0) \leftarrow E, E \leftarrow AC(15)$ $INC \qquad rB_{5}: \qquad AC \leftarrow \text{shr } AC, AC(0) \leftarrow E, E \leftarrow AC(15)$ $INC \qquad rB_{5}: \qquad AC \leftarrow AC + 1$ $SPA \qquad rB_{4}: \qquad \text{if } (AC(15) = 0) \text{ then } (PC \leftarrow PC + 1)$ $SNA \qquad rB_{2}: \qquad \text{if } (AC(15) = 1) \text{ then } (PC \leftarrow PC + 1)$ $SZA \qquad rB_{2}: \qquad \text{if } (AC \leftarrow 0) \text{ then } PC \leftarrow PC + 1$ $SZE \qquad rB_{1}: \qquad \text{if } (E = 0) \text{ then } (PC \leftarrow PC + 1)$ $IND \qquad B_{1}: \qquad B_{1}: \qquad (E = 0) \text{ then } (PC \leftarrow PC + 1)$ $INP \qquad PB_{11}: \qquad AC(0-7) \leftarrow INPR, FGI \leftarrow 0$ $OUT \qquad PB_{20}: \qquad OUTR \leftarrow AC(0-7), FGO \leftarrow 0$ $SKI \qquad PB_{2}: \qquad \text{if } (FGI = 1) \text{ then } (PC \leftarrow PC + 1)$ $SKO \qquad PB_{8}: \qquad \text{if } (FGO = 1) \text{ then } (PC \leftarrow PC + 1)$ $IEN \leftarrow 1$	157		
Register–reference: $ \begin{aligned} D_{0} \overline{I_{6}} &: \qquad M \left[AR\right] \leftarrow DR, & \text{if } (DR=0) \text{ then} \\ (PC \leftarrow PC+1), SC \leftarrow 0 \end{aligned} $ Register–reference: $ \begin{aligned} D_{7} I^{*} T_{3} &= r \left(\text{common to all register-reference instruct ions} \right. \\ IR(i) &= B_{i} \left(i = 0, 1, 2, \ldots, 11 \right) \end{aligned} $ $ r: \qquad SC \leftarrow 0 $ CLA $ rB_{11} : \qquad AC \leftarrow 0 $ CLE $ rB_{10} : \qquad E \leftarrow 0 \\ \text{CMA} \qquad rB_{9} : \qquad AC \leftarrow AC \end{aligned} $ CME $ rB_{8} : \qquad E \leftarrow \overline{E} $ CIR $ rB_{5} : \qquad AC \leftarrow \text{shr } AC, AC \left(15 \right) \leftarrow E, E \leftarrow AC \left(0 \right) $ CIL $ rB_{5} : \qquad AC \leftarrow \text{shr } AC, AC \left(0 \right) \leftarrow E, E \leftarrow AC \left(0 \right) $ CIL $ rB_{5} : \qquad AC \leftarrow \text{shr } AC, AC \left(0 \right) \leftarrow E, E \leftarrow AC \left(15 \right) \end{aligned} $ INC $ rB_{5} : \qquad AC \leftarrow AC + 1 $ SPA $ rB_{4} : \qquad \text{If } \left(AC \left(15 \right) = 0 \right) \text{ then } \left(PC \leftarrow PC + 1 \right) $ SNA $ rB_{3} : \qquad \text{If } \left(AC \left(15 \right) = 1 \right) \text{ then } \left(PC \leftarrow PC + 1 \right) $ SZA $ rB_{2} : \qquad \text{If } \left(AC \left(15 \right) = 1 \right) \text{ then } \left(PC \leftarrow PC + 1 \right) $ SZE $ rB_{1} : \qquad \text{If } \left(E - 0 \right) \text{ then } \left(PC \leftarrow PC + 1 \right) $ SZE $ rB_{1} : \qquad \text{If } \left(E - 0 \right) \text{ then } \left(PC \leftarrow PC + 1 \right) $ HLT $ rB_{0} : \qquad S \leftarrow 0 $ Input—output: $ D_{7}TT_{3} = p \left(\text{common to all input—output instructions} \right) $ $ RR(i) = B_{i} \left(i = 6, 7, 8, 9, 10, 11 \right) $ $ p: \qquad SC \leftarrow 0 $ OUT $ pB_{11} : \qquad AC \left(0 - 7 \right) \leftarrow INPR, FGI \leftarrow 0 $ OUT $ pB_{20} : \qquad OUTR \leftarrow AC \left(0 - 7 \right), FGO \leftarrow 0 $ SKI $ pB_{2} : \qquad \text{If } \left(FGI - 1 \right) \text{ then } \left(PC \leftarrow PC + 1 \right) $ SKO $ pB_{8} : \qquad \text{If } \left(FGO - 1 \right) \text{ then } \left(PC \leftarrow PC + 1 \right) $ ION $ pB_{7} : \qquad IEN \leftarrow 1 $	1023		
Register–reference: $\begin{array}{cccccccccccccccccccccccccccccccccccc$			
Register–reference: $D_7F T_3 = r \text{ (common to all register-reference instruct ions} \\ IR(i) = B_i (i = 0, 1, 2, \dots, 11) \\ r: SC \leftarrow 0 \\ CLA \\ rB_{11}: AC \leftarrow 0 \\ CLE \\ rB_{20}: E \leftarrow 0 \\ CMA \\ rB_{2}: AC \leftarrow AC \\ CME \\ rB_{2}: AC \leftarrow Shr AC, AC (15) \leftarrow E, E \leftarrow AC (0) \\ CIR \\ rB_{2}: AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \\ rB_{2}: AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \\ rB_{2}: AC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \\ rB_{2}: AC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \\ rB_{2}: AC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \\ rB_{2}: AC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \\ rB_{2}: AC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \\ rB_{2}: AC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \\ rB_{2}: AC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \\ rB_{2}: AC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (15) \\ INC \leftarrow AC \leftarrow Shl AC, AC (0) \leftarrow E, E \leftarrow AC (0, 15) \\ INC \leftarrow AC \leftarrow Shl AC, AC (0, 15) \leftarrow E, E \leftarrow AC (0, 15) \\ INC \leftarrow AC \leftarrow Shl AC, AC (0, 15) \leftarrow E, E \leftarrow AC (0, 15) \\ INC \leftarrow AC \leftarrow Shl AC, AC (0, 15) \leftarrow E, E \leftarrow AC (0, 15) \\ INC \leftarrow AC \leftarrow Shl AC, AC (0, 15) \leftarrow E, E \leftarrow AC (0, 15) \leftarrow E, E \leftarrow AC (0, 15) \\ INC \leftarrow AC \leftarrow Shl AC, AC (0, 15) \leftarrow E, E \leftarrow AC (0, 15) \leftarrow E, E \leftarrow AC (0, 15) \\ INC \leftarrow AC \leftarrow Shl AC, AC (0, 15) \leftarrow E, E \leftarrow AC (0, 15) \leftarrow E$		2526.	
$D_7FT_3 = r \text{ (common to all register-reference instruct ions}$ $IR(i) = B_i (i = 0, 1, 2, \dots, 11)$ $r : SC \leftarrow 0$ $CLA \qquad rB_{11}: \qquad AC \leftarrow 0$ $CLE \qquad rB_{10}: \qquad E \leftarrow 0$ $CMA \qquad rB_{2}: \qquad AC \leftarrow \overline{AC}$ $CME \qquad rB_{3}: \qquad E \leftarrow \overline{E}$ $CIR \qquad rB_{7}: \qquad AC \leftarrow \text{shr } AC, AC(15) \leftarrow E, E \leftarrow AC(0)$ $CIL \qquad rB_{6}: \qquad AC \leftarrow \text{shl } AC, AC(0) \leftarrow E, E \leftarrow AC(15)$ $INC \qquad rB_{2}: \qquad AC \leftarrow \text{shl } AC, AC(0) \leftarrow E, E \leftarrow AC(15)$ $INC \qquad rB_{3}: \qquad If (AC(15) = 0) \text{ then } (PC \leftarrow PC + 1)$ $SNA \qquad rB_{3}: \qquad If (AC(15) = 1) \text{ then } (PC \leftarrow PC + 1)$ $SZA \qquad rB_{2}: \qquad If (AC = 0) \text{ then } PC \leftarrow PC + 1$ $SZE \qquad rB_{1}: \qquad If (E = 0) \text{ then } (PC \leftarrow PC + 1)$ $HLT \qquad rB_{0}: \qquad S \leftarrow 0$ $Input-output: \qquad D_7IT_3 = p \text{ (common to all input-output instructions)}$ $IR(i) = B_i (i = 6, 7, 8, 9, 10, 11)$ $p: \qquad SC \leftarrow 0$ $INP \qquad pB_{11}: \qquad AC(0 - 7) \leftarrow INPR, FGI \leftarrow 0$ $OUT \qquad pB_{20}: \qquad OUTR \leftarrow AC(0 - 7), FGO \leftarrow 0$ $SKI \qquad pB_{2}: \qquad If (FGI - 1) \text{ then } (PC \leftarrow PC + 1)$ $SKO \qquad pB_{3}: \qquad If (FGO - 1) \text{ then } (PC \leftarrow PC + 1)$ $IEN \leftarrow 1$	Register-reference:		(**************************************
$IR(i) = B_i \ (i = 0, 1, 2, \dots, 11)$ $r : SC \leftarrow 0$ $CLA \qquad rB_{11}: \qquad AC \leftarrow 0$ $CLE \qquad rB_{20}: \qquad E \leftarrow 0$ $CMA \qquad rB_{2}: \qquad AC \leftarrow AC$ $CME \qquad rB_{3}: \qquad E \leftarrow \overline{E}$ $CIR \qquad rB_{5}: \qquad AC \leftarrow \text{shr } AC, AC \ (15) \leftarrow E, E \leftarrow AC \ (0)$ $CIL \qquad rB_{5}: \qquad AC \leftarrow \text{shl } AC, AC \ (0) \leftarrow E, E \leftarrow AC \ (15)$ $INC \qquad rB_{5}: \qquad AC \leftarrow \text{shl } AC, AC \ (0) \leftarrow E, E \leftarrow AC \ (15)$ $INC \qquad rB_{5}: \qquad AC \leftarrow AC + 1$ $SPA \qquad rB_{4}: \qquad If \ (AC \ (15) = 0) \ \text{then } \ (PC \leftarrow PC + 1)$ $SNA \qquad rB_{3}: \qquad If \ (AC \ (15) = 1) \ \text{then } \ (PC \leftarrow PC + 1)$ $SZA \qquad rB_{2}: \qquad If \ (AC \ (0) \ \text{then } \ PC \leftarrow PC + 1)$ $SZE \qquad rB_{1}: \qquad If \ (E - 0) \ \text{then } \ (PC \leftarrow PC + 1)$ $INT \qquad rB_{0}: \qquad S \leftarrow 0$ $Input-output:$ $D_{7}II_{3} = p \ (\text{common to all input-output instructions})$ $IR(i) = B_{i} \ (i = 6, 7, 8, 9, 10, 11)$ $p: \qquad SC \leftarrow 0$ $INP \qquad pB_{11}: \qquad AC(0 - 7) \leftarrow INPR, FGI \leftarrow 0$ $OUT \qquad pB_{10}: \qquad OUTR \leftarrow AC \ (0 - 7), FGO \leftarrow 0$ $SKI \qquad pB_{9}: \qquad If \ (FGI - 1) \ \text{then } \ (PC \leftarrow PC + 1)$ $SKO \qquad pB_{8}: \qquad If \ (FGO - 1) \ \text{then } \ (PC \leftarrow PC + 1)$ $IEN \leftarrow 1$	Tree Person	$D_n I' T_n = \tau (\text{comm} \sigma)$	on to all register-reference instruct ions
$\begin{array}{cccccccccccccccccccccccccccccccccccc$			
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		1.7	
CLE rB_{0} : $E \leftarrow 0$	CLA		
CMA rB_9 : $AC \leftarrow \overline{AC}$ CME rB_8 : $E \leftarrow \overline{E}$ CIR rB_7 : $AC \leftarrow \operatorname{shr} AC$, $AC(15) \leftarrow E$, $E \leftarrow AC(0)$ CIL rB_6 : $AC \leftarrow \operatorname{shl} AC$, $AC(0) \leftarrow E$, $E \leftarrow AC(15)$ INC rB_5 : $AC \leftarrow AC + 1$ SPA rB_4 : If $(AC(15) = 0)$ then $(PC \leftarrow PC + 1)$ SNA rB_3 : If $(AC(15) = 1)$ then $(PC \leftarrow PC + 1)$ SZA rB_9 : If $(AC = 0)$ then $PC \leftarrow PC + 1$ SZE rB_1 : If $(E = 0)$ then $(PC \leftarrow PC + 1)$ HIT rB_0 : $S \leftarrow 0$ Input—output: $D_7II_3 = p \text{ (common to all input—output instructions)}$ $IR(i) = B_i \text{ (}i = 6, 7, 8, 9, 10, 11)$ p : $SC \leftarrow 0$ INP pB_{11} : $AC(0-7) \leftarrow INPR$, $FGI \leftarrow 0$ OUT pB_{12} : $OUTR \leftarrow AC(0-7)$, $FGO \leftarrow 0$ SKI pB_9 : If $(FGI = 1)$ then $(PC \leftarrow PC + 1)$ SKO pB_8 : If $(FGO = 1)$ then $(PC \leftarrow PC + 1)$ ION pB_7 : $IEN \leftarrow 1$			
CME CIR rB_8 : $E \leftarrow \overline{E}$ CIR rB_7 : $AC \leftarrow \operatorname{shr} AC$, $AC(15) \leftarrow E$, $E \leftarrow AC(0)$ CIL rB_6 : $AC \leftarrow \operatorname{shl} AC$, $AC(0) \leftarrow E$, $E \leftarrow AC(15)$ INC rB_5 : $AC \leftarrow AC + 1$ SPA rB_4 : If $(AC(15) = 0)$ then $(PC \leftarrow PC + 1)$ SNA rB_3 : If $(AC(15) = 1)$ then $(PC \leftarrow PC + 1)$ SZA rB_2 : If $(AC = 0)$ then $PC \leftarrow PC + 1$ SZE rB_1 : If $(E = 0)$ then $(PC \leftarrow PC + 1)$ HIT rB_0 : $S \leftarrow 0$ Input—output: $D_7II_3 = p \text{ (common to all input—output instructions)}$ $IR(i) = B_i \text{ (}i = 6, 7, 8, 9, 10, 11)$ p : $SC \leftarrow 0$ INP pB_{11} : $AC(0-7) \leftarrow INPR$, $FGI \leftarrow 0$ OUT pB_{20} : OUTR $\leftarrow AC(0-7)$, $FGO \leftarrow 0$ SKI pB_9 : If $(FGI = 1)$ then $(PC \leftarrow PC + 1)$ SKO pB_8 : If $(FGO = 1)$ then $(PC \leftarrow PC + 1)$ IEN $\leftarrow 1$	CMA		
CIR rB_7^{-} : $AC \leftarrow \sin AC$, $AC(15) \leftarrow E$, $E \leftarrow AC(0)$ CIL rB_6 : $AC \leftarrow \sin AC$, $AC(0) \leftarrow E$, $E \leftarrow AC(15)$ INC rB_5 : $AC \leftarrow AC + 1$ SPA rB_4 : If $(AC(15) = 0)$ then $(PC \leftarrow PC + 1)$ SNA rB_3 : If $(AC(15) = 1)$ then $(PC \leftarrow PC + 1)$ SZA rB_2 : If $(AC = 0)$ then $PC \leftarrow PC + 1$ SZE rB_1 : If $(E = 0)$ then $(PC \leftarrow PC + 1)$ HLT rB_0 : $S \leftarrow 0$ Input—output: $D_7IT_3 = p \text{ (common to all input—output instructions)}$ $IR(i) = B_i \text{ (}i = 6, 7, 8, 9, 10, 11)$ $p: SC \leftarrow 0$ INP pB_{11} : $AC(0-7) \leftarrow INPR$, $FGI \leftarrow 0$ OUT pB_{20} : $OUTR \leftarrow AC(0-7)$, $FGO \leftarrow 0$ SKI pB_9 : If $(FGI = 1)$ then $(PC \leftarrow PC + 1)$ SKO pB_8 : If $(FGO = 1)$ then $(PC \leftarrow PC + 1)$ ION pB_7 : $IEN \leftarrow 1$	CME		
CIL rB_6 : $AC \leftarrow \sinh AC$, $AC(0) \leftarrow E$, $E \leftarrow AC(15)$ INC rB_5 : $AC \leftarrow AC + 1$ SPA rB_4 : If $(AC(15) = 0)$ then $(PC \leftarrow PC + 1)$ SNA rB_3 : If $(AC(15) = 1)$ then $(PC \leftarrow PC + 1)$ SZA rB_2 : If $(AC = 0)$ then $PC \leftarrow PC + 1$ SZE rB_1 : If $E = 0$ then $E \leftarrow PC \leftarrow PC + 1$ HLT rB_0 : $E \leftarrow 0$ then $E \leftarrow PC \leftarrow P$	CIR	rB₁:	$AC \leftarrow \text{shr } AC$, $AC(15) \leftarrow E$, $E \leftarrow AC(0)$
INC rB_5 : $AC \leftarrow AC + 1$ SPA rB_4 : If $(AC(15) = 0)$ then $(PC \leftarrow PC + 1)$ SNA rB_3 : If $(AC(15) = 1)$ then $(PC \leftarrow PC + 1)$ SZA rB_2 : If $(AC - 0)$ then $PC \leftarrow PC + 1$ SZE rB_1 : If $(E - 0)$ then $(PC \leftarrow PC + 1)$ HLT rB_0 : $S \leftarrow 0$ Input—output: $D_7II_3 = p \text{ (common to all input—output instructions)}$ $IR(i) = B_i \text{ (}i = 6, 7, 8, 9, 10, 11)$ $p: SC \leftarrow 0$ INP pB_{11} : $AC(0-7) \leftarrow INPR$, $FGI \leftarrow 0$ OUT pB_{20} : $OUTR \leftarrow AC(0-7)$, $FGO \leftarrow 0$ SKI pB_2 : If $(FGI - 1)$ then $(PC \leftarrow PC + 1)$ SKO pB_8 : If $(FGO - 1)$ then $(PC \leftarrow PC + 1)$ ION pB_7 : $IEN \leftarrow 1$	CIL	rB_6 :	
SNA rB_3 : If $(AC(15) - 1)$ then $(PC \leftarrow PC + 1)$ SZA rB_3 : If $(AC - 0)$ then $PC \leftarrow PC + 1)$ SZE rB_1 : If $(E - 0)$ then $(PC \leftarrow PC + 1)$ HLT rB_0 : $S \leftarrow 0$ Input–output: $D_7II_3' = p \text{ (common to all input–output instructions)}$ $IR(i) = B_i (i = 6, 7, 8, 9, 10, 11)$ $p: SC \leftarrow 0$ INP pB_{11} : $AC(0-7) \leftarrow INPR$, $FGI \leftarrow 0$ OUT pB_{20} : $OUTR \leftarrow AC (0-7)$, $FGO \leftarrow 0$ SKI pB_9 : If $(FGI - 1)$ then $(PC \leftarrow PC + 1)$ SKO pB_8 : If $(FGO - 1)$ then $(PC \leftarrow PC + 1)$ ION pB_7 : $IEN \leftarrow 1$	INC	rB₅:	
SNA rB_3 : If $(AC(15) - 1)$ then $(PC \leftarrow PC + 1)$ SZA rB_2 : If $(AC - 0)$ then $PC \leftarrow PC + 1$ SZE rB_1 : If $(E - 0)$ then $(PC \leftarrow PC + 1)$ HLT rB_0 : $S \leftarrow 0$ Input–output: $D_7IT_3 = p \text{ (common to all input–output instructions)}$ $IR(i) = B_i \text{ (}i = 6, 7, 8, 9, 10, 11)$ $p: SC \leftarrow 0$ INP pB_{11} : $AC(0-7) \leftarrow INPR$, $FGI \leftarrow 0$ OUT pB_{20} : $OUTR \leftarrow AC(0-7)$, $FGO \leftarrow 0$ SKI pB_2 : If $(FGI - 1)$ then $(PC \leftarrow PC + 1)$ SKO pB_8 : If $(FGO - 1)$ then $(PC \leftarrow PC + 1)$ ION pB_7 : $IEN \leftarrow 1$	SPA	rB_4 :	If $(AC(15) = 0)$ then $(PC \leftarrow PC + 1)$
SZE rB_1 : If $(E-0)$ then $(PC \leftarrow PC+1)$ HLT rB_0 : $S \leftarrow 0$ Input–output: $D_7IT_3 = p \text{ (common to all input–output instructions)}$ $IR(i) = B_i (i = 6, 7, 8, 9, 10, 11)$ $p: SC \leftarrow 0$ INP pB_{11} : $AC(0-7) \leftarrow INPR$, $FGI \leftarrow 0$ OUT pB_{20} : $OUTR \leftarrow AC(0-7)$, $FGO \leftarrow 0$ SKI pB_2 : If $(FGI-1)$ then $(PC \leftarrow PC+1)$ SKO pB_8 : If $(FGO-1)$ then $(PC \leftarrow PC+1)$ ION pB_7 : $IEN \leftarrow 1$	SNA	rB₃:	
SZE rB_1 : If $(E-0)$ then $(PC \leftarrow PC+1)$ HLT rB_0 : $S \leftarrow 0$ Input–output: $D_7IT_3 = p \text{ (common to all input–output instructions)}$ $IR(i) = B_i (i = 6, 7, 8, 9, 10, 11)$ $p: SC \leftarrow 0$ INP pB_{11} : $AC(0-7) \leftarrow INPR$, $FGI \leftarrow 0$ OUT pB_{20} : $OUTR \leftarrow AC(0-7)$, $FGO \leftarrow 0$ SKI pB_2 : If $(FGI-1)$ then $(PC \leftarrow PC+1)$ SKO pB_8 : If $(FGO-1)$ then $(PC \leftarrow PC+1)$ ION pB_7 : $IEN \leftarrow 1$	SZA	rB_2 :	If $(AC - 0)$ then $PC \leftarrow PC + 1$
Input–output: $ D_7IT_3 = p \text{ (common to all input–output instructions)} $ $ IR(i) = B_i (i = 6, 7, 8, 9, 10, 11) $ $ p: SC \leftarrow 0 $ $ INP \qquad pB_{11}: \qquad AC(0-7) \leftarrow INPR, FGI \leftarrow 0 $ $ OUT \qquad pB_{10}: \qquad OUTR \leftarrow AC (0-7), FGO \leftarrow 0 $ $ SKI \qquad pB_9: \qquad If (FGI = 1) \text{ then } (PC \leftarrow PC + 1) $ $ SKO \qquad pB_8: \qquad If (FGO = 1) \text{ then } (PC \leftarrow PC + 1) $ $ ION \qquad pB_7: \qquad IEN \leftarrow 1 $	SZE	rB_1 :	
$D_7IT_3 = p \text{ (common to all input-output instructions)}$ $IR(i) = B_i (i = 6, 7, 8, 9, 10, 11)$ $p: SC \leftarrow 0$ $INP \qquad pB_{11}: \qquad AC(0-7) \leftarrow INPR, FGI \leftarrow 0$ $OUT \qquad pB_{20}: \qquad OUTR \leftarrow AC (0-7), FGO \leftarrow 0$ $SKI \qquad pB_9: \qquad \text{If } (FGI = 1) \text{ then } (PC \leftarrow PC + 1)$ $SKO \qquad pB_8: \qquad \text{If } (FGO - 1) \text{ then } (PC \leftarrow PC + 1)$ $ION \qquad pB_7: \qquad IEN \leftarrow 1$	HLT	rB_0 :	$S \leftarrow 0$
$D_7IT_3 = p \text{ (common to all input-output instructions)}$ $IR(i) = B_i (i = 6, 7, 8, 9, 10, 11)$ $p: SC \leftarrow 0$ $INP \qquad pB_{11}: \qquad AC(0-7) \leftarrow INPR, FGI \leftarrow 0$ $OUT \qquad pB_{20}: \qquad OUTR \leftarrow AC (0-7), FGO \leftarrow 0$ $SKI \qquad pB_9: \qquad \text{If } (FGI = 1) \text{ then } (PC \leftarrow PC + 1)$ $SKO \qquad pB_8: \qquad \text{If } (FGO - 1) \text{ then } (PC \leftarrow PC + 1)$ $ION \qquad pB_7: \qquad IEN \leftarrow 1$	Input-output:		
INP $\rho_{B_{11}}$: $AC(0-7) \leftarrow INPR$, $FGI \leftarrow 0$ OUT $\rho_{B_{10}}$: $OUTR \leftarrow AC(0-7)$, $FGO \leftarrow 0$ SKI $\rho_{B_{9}}$: If $(FGI = 1)$ then $(PC \leftarrow PC + 1)$ SKO $\rho_{B_{8}}$: If $(FGO = 1)$ then $(PC \leftarrow PC + 1)$ ION $\rho_{B_{7}}$: $IEN \leftarrow 1$		$D_7IT_3 = p (commo$	n to all input-output instructions)
INP $\rho B_{11}^{\prime\prime}$: $AC(0-7) \leftarrow INPR$, $FGI \leftarrow 0$ OUT ρB_{10} : $OUTR \leftarrow AC(0-7)$, $FGO \leftarrow 0$ SKI ρB_{9} : If $(FGI = 1)$ then $(PC \leftarrow PC + 1)$ SKO ρB_{8} : If $(FGO = 1)$ then $(PC \leftarrow PC + 1)$ ION ρB_{7} : $IEN \leftarrow 1$		$IR(i) = B_i (i = 6, 7)$	7, 8, 9, 10, 11)
OUT ρB_{00} : OUTR \leftarrow AC (0-7), FGO \leftarrow 0 SKI ρB_{0} : If $(FGI-1)$ then $(PC \leftarrow PC+1)$ SKO ρB_{8} : If $(FGO-1)$ then $(PC \leftarrow PC+1)$ ION ρB_{7} : IEN \leftarrow 1		p:	
SKI ρB_9 : If $(FGI = 1)$ then $(PC \leftarrow PC + 1)$ SKO ρB_8 : If $(FGO = 1)$ then $(PC \leftarrow PC + 1)$ ION ρB_7 : $IEN \leftarrow 1$		pB_{11} :	
SKO ρB_8 : If $(FGO-1)$ then $(PC \leftarrow PC+1)$ ION ρB_7 : $IEN \leftarrow 1$		<i>pB</i> ₁₀ :	
ION pB_7 : $IEN \leftarrow 1$		pB_9 :	
1 '	SKO	<i>pB</i> ₈ :	If $(FGO - 1)$ then $(PC \leftarrow PC + 1)$
IOF pB_6 : $IEN \leftarrow 0$		pB_7 :	
	IOF	pB_6 :	$IEN \leftarrow 0$

Control Functions and Microoperations

Control of Registers and Memory

- Control inputs of the registers
 - LD (load)
 - INR (increment)
 - CLR (clear)
- To derive the gate structure associated with the control inputs of AR
 - Find all the statements that change the content of AR

$$R' T_0: AR \leftarrow PC$$

 $R' T_2: AR \leftarrow IR(0-11)$
 $D_7' IT_3: AR \leftarrow M[AR]$
 $RT_0: AR \leftarrow 0$
 $D_5 T_4: AR \leftarrow AR + 1$

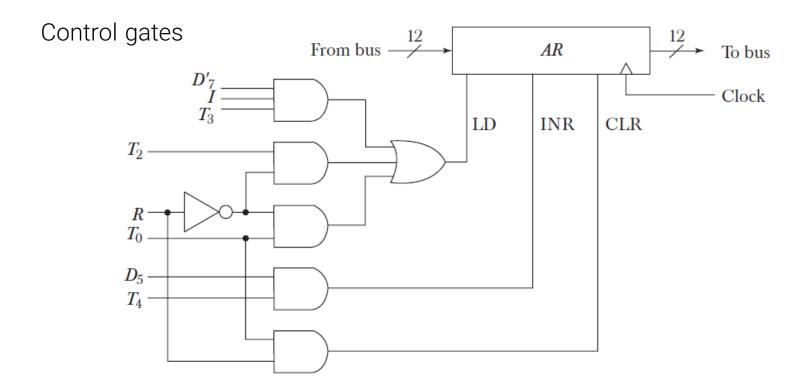
Control of Registers

Control functions

$$LD(AR) = R'T_0 + R'T_2 + D_7'IT_3$$

$$CLR(AR) = RT_0$$

$$INR(AR) = D_5T_4$$



Control of Memory

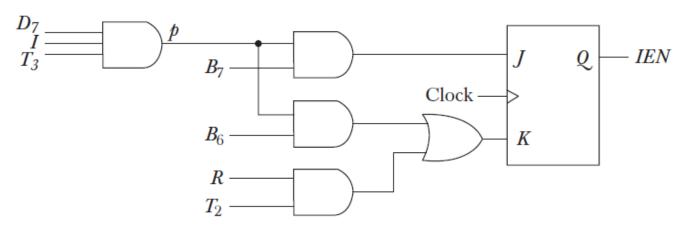
Read operation

Control function

Read =
$$R'T_1 + D_7'IT_3 + (D_0 + D_1 + D_2 + D_6)T_4$$

Control of Single Flip-flops

 pB_7 : $IEN \leftarrow 1$ pB_6 : $IEN \leftarrow 0$ RT_2 : $IEN \leftarrow 0$

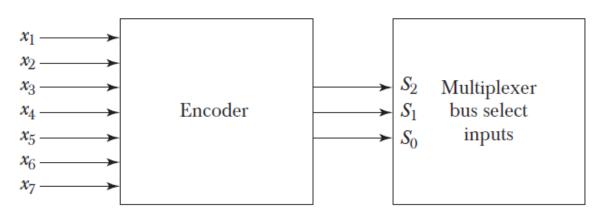


Control of Common Bus

Encoder for Bus Selection Circuit

S_0	=	x_1	+	x_3	+	x_5	+	x_7
S_1	=	x_2	+	x_3	+	x_6	+	x_7
S_2	=	x_4	+	x_5	+	x_6	+	x_7

			Inputs					Output	S	Register selected
x_1	x_2	x ₃	\mathcal{X}_4	x ₅	x_6	x_7	$\overline{S_2}$	S_1	S_0	for bus
0	0	0	0	0	0	0	0	0	0	None
1	0	0	0	0	0	0	0	0	1	AR
0	1	0	0	0	0	0	0	1	0	PC
0	0	1	0	0	0	0	0	1	1	DR
0	0	0	1	0	0	0	1	0	0	AC
0	0	0	0	1	0	0	1	0	1	IR
0	0	0	0	0	1	0	1	1	0	TR
0	0	0	0	0	0	1	1	1	1	Memory



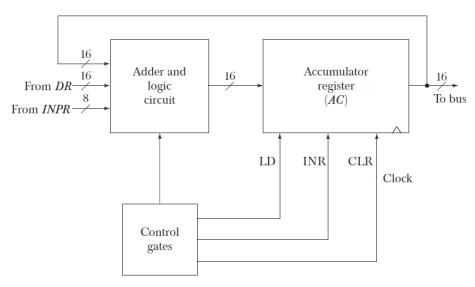
$$D_4T_4$$
: $PC \leftarrow AR$
 D_5T_5 : $PC \leftarrow AR$

$$x_1 = D_4 T_4 + D_5 T_5$$

Design of Accumulator Logic

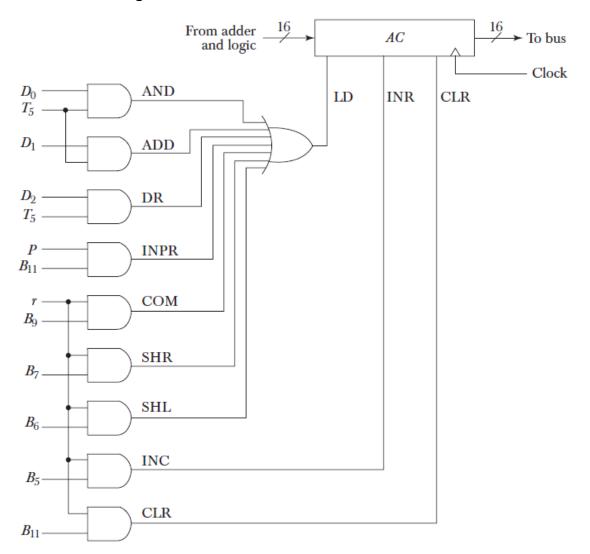
extract all the statements that change the content of AC

$D_0 T_5$:	$AC \leftarrow AC \land DR$	AND with DR
$D_1 T_5$:	$AC \leftarrow AC + DR$	Add with DR
D_2T_5 :	$AC \leftarrow DR$	Transfer from <i>DR</i>
pB_{11} :	$AC(0-7) \leftarrow INPR$	Transfer from INPR
rB_9 :	$AC \leftarrow \overline{AC}$	Complement
rB_7 :	$AC \leftarrow \text{shr } AC, AC(15) \leftarrow E$	Shift right
rB_6 :	$AC \leftarrow \text{shl } AC, AC(0) \leftarrow E$	Shift left
rB_{11} :	$AC \leftarrow 0$	Clear
rB_5 :	$AC \leftarrow AC + 1$	Increment

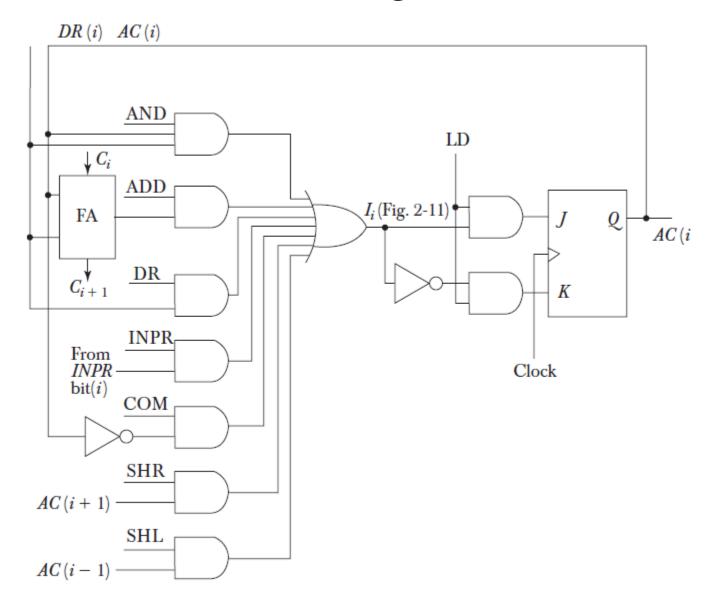


Control of AC Register

Gate structure for controlling the LD, INR, and CLR of AC



Adder and Logic Circuit



پایان

موفق و پیروز باشید