به نام خدا

طراحی سیستم‌های دیجیتال

مرور مولفه‌های مهم

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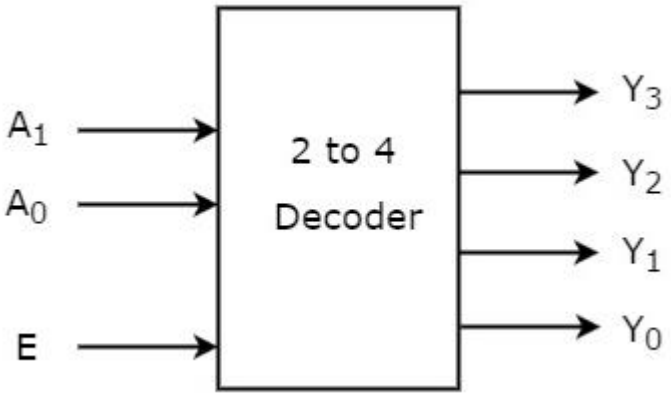
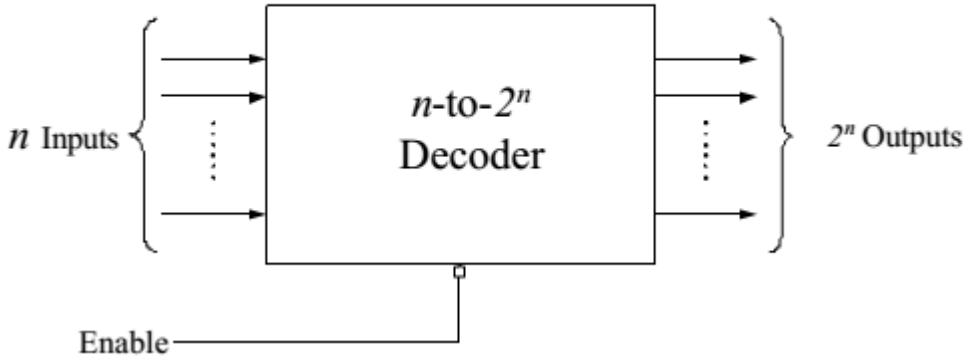
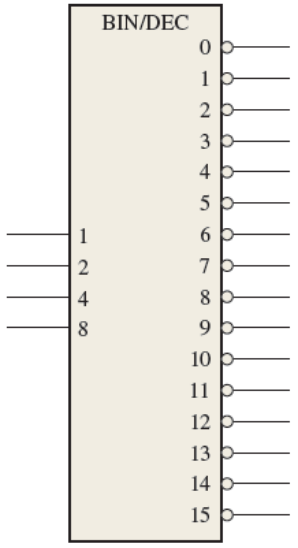
Decoders





Inputs			Outputs			
EN	A	B	Y_3	Y_2	Y_1	Y_0
0	×	×	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

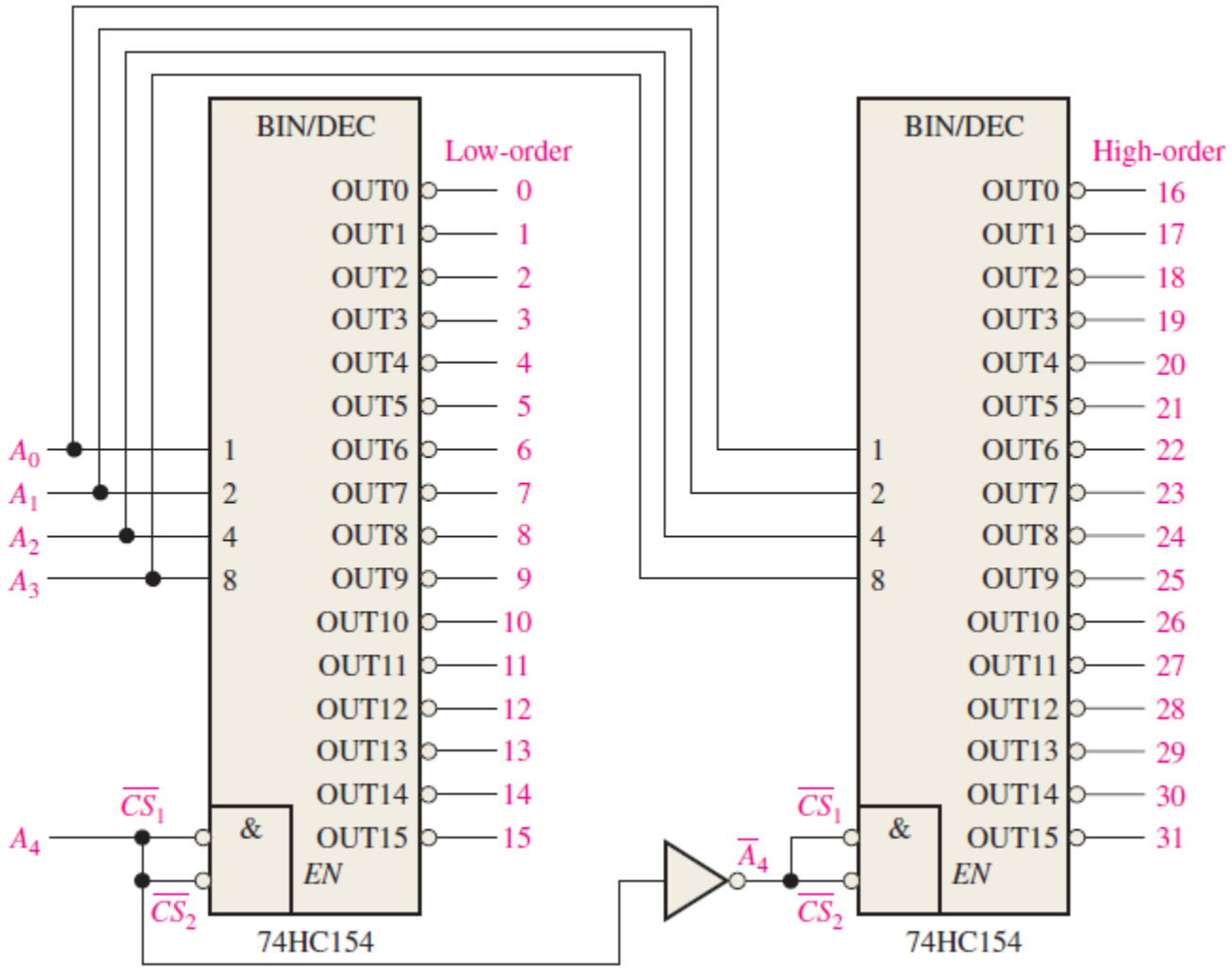
Decoders



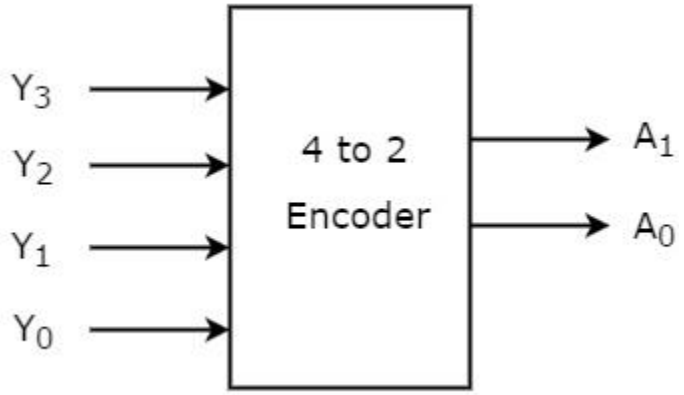
- 4-to-16 decoder with active-LOW outputs

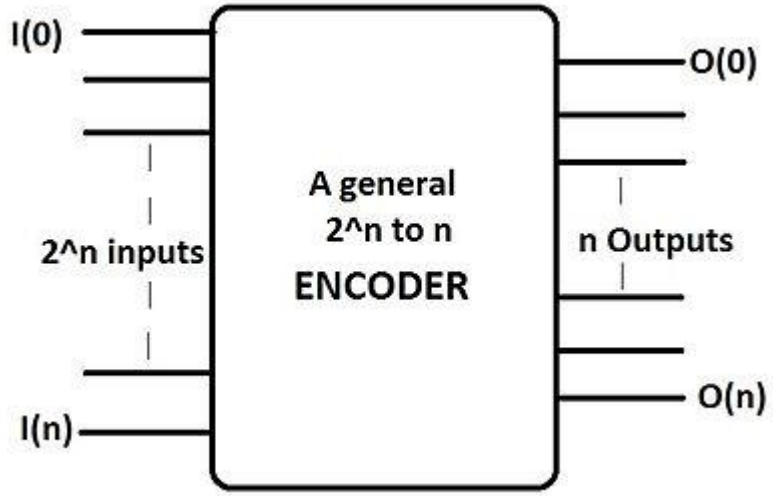
Decimal Digit	Binary Inputs A_3	A_2	A_1	A_0	Decoding Function	Outputs 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	$\overline{A}_3\overline{A}_2\overline{A}_1\overline{A}_0$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	$\overline{A}_3\overline{A}_2\overline{A}_1A_0$	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	0	1	0	$\overline{A}_3\overline{A}_2A_1\overline{A}_0$	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
3	0	0	1	1	$\overline{A}_3\overline{A}_2A_1A_0$	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
4	0	1	0	0	$\overline{A}_3A_2\overline{A}_1\overline{A}_0$	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
5	0	1	0	1	$\overline{A}_3A_2\overline{A}_1A_0$	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
6	0	1	1	0	$\overline{A}_3A_2A_1\overline{A}_0$	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
7	0	1	1	1	$\overline{A}_3A_2A_1A_0$	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
8	1	0	0	0	$A_3\overline{A}_2\overline{A}_1\overline{A}_0$	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
9	1	0	0	1	$A_3\overline{A}_2\overline{A}_1A_0$	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
10	1	0	1	0	$A_3\overline{A}_2A_1\overline{A}_0$	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
11	1	0	1	1	$A_3\overline{A}_2A_1A_0$	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
12	1	1	0	0	$A_3A_2\overline{A}_1\overline{A}_0$	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
13	1	1	0	1	$A_3A_2\overline{A}_1A_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
14	1	1	1	0	$A_3A_2A_1\overline{A}_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
15	1	1	1	1	$A_3A_2A_1A_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Decoders


BIN/DEC
Low-order
OUT0 0
OUT1 1
OUT2 2
OUT3 3
OUT4 4
OUT5 5
OUT6 6
OUT7 7
OUT8 8
OUT9 9
OUT10 10
OUT11 11
OUT12 12
OUT13 13
OUT14 14
OUT15 15
A_0
A_1
A_2
A_3
1
2
4
8
A_4
$\overline{CS}_1$
$\overline{CS}_2$
&
EN
74HC154
BIN/DEC
High-order
OUT0 16
OUT1 17
OUT2 18
OUT3 19
OUT4 20
OUT5 21
OUT6 22
OUT7 23
OUT8 24
OUT9 25
OUT10 26
OUT11 27
OUT12 28
OUT13 29
OUT14 30
OUT15 31
$\overline{A}_4$
74HC154

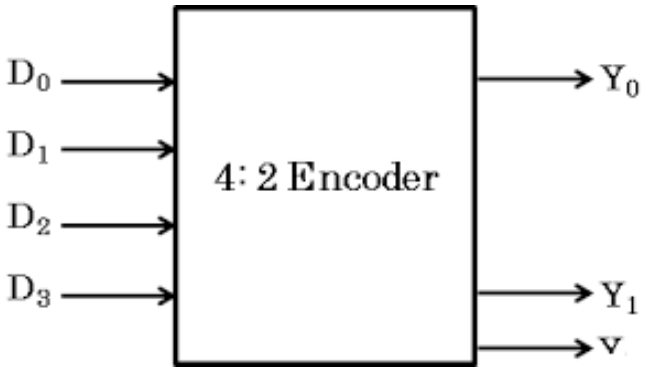
Encoders





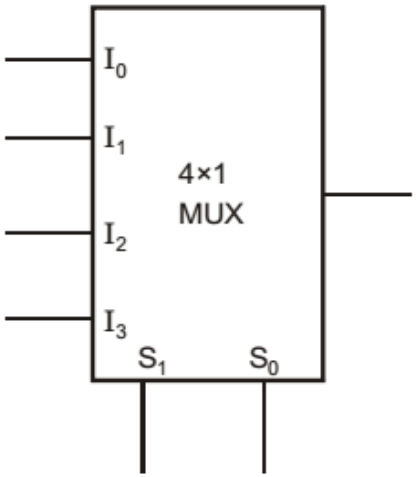
INPUTS				OUTPUTS	
Y_3	Y_2	Y_1	Y_0	A_1	A_0
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

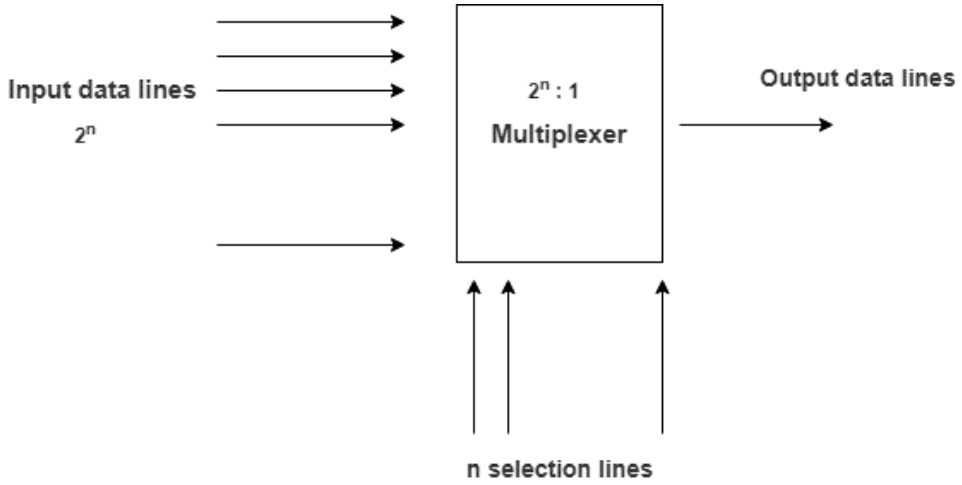
Encoders



Inputs				Outputs		
D_0	D_1	D_2	D_3	Y_1	Y_0	V
0	0	0	0	×	×	0
1	0	0	0	0	0	1
×	1	0	0	0	1	1
×	×	1	0	1	0	1
×	×	×	1	1	1	1

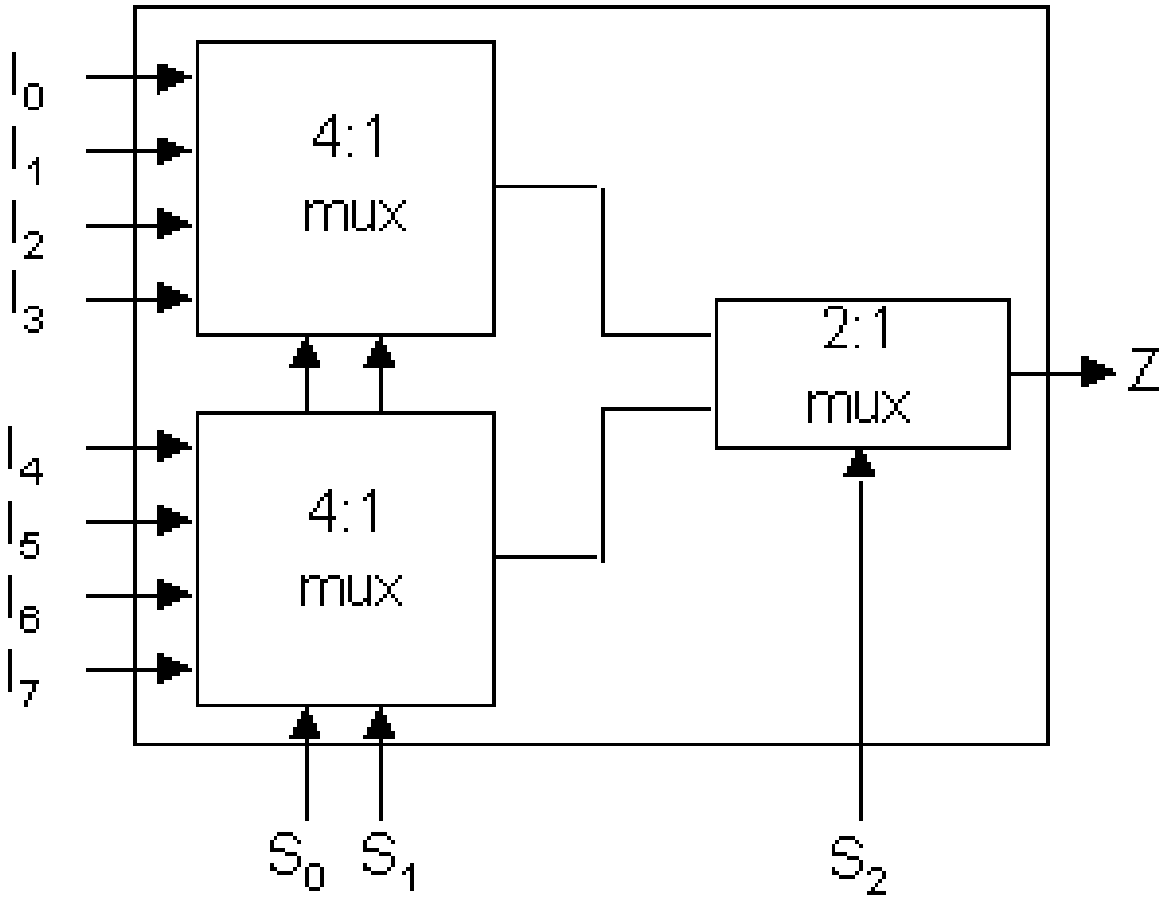
Multiplexers



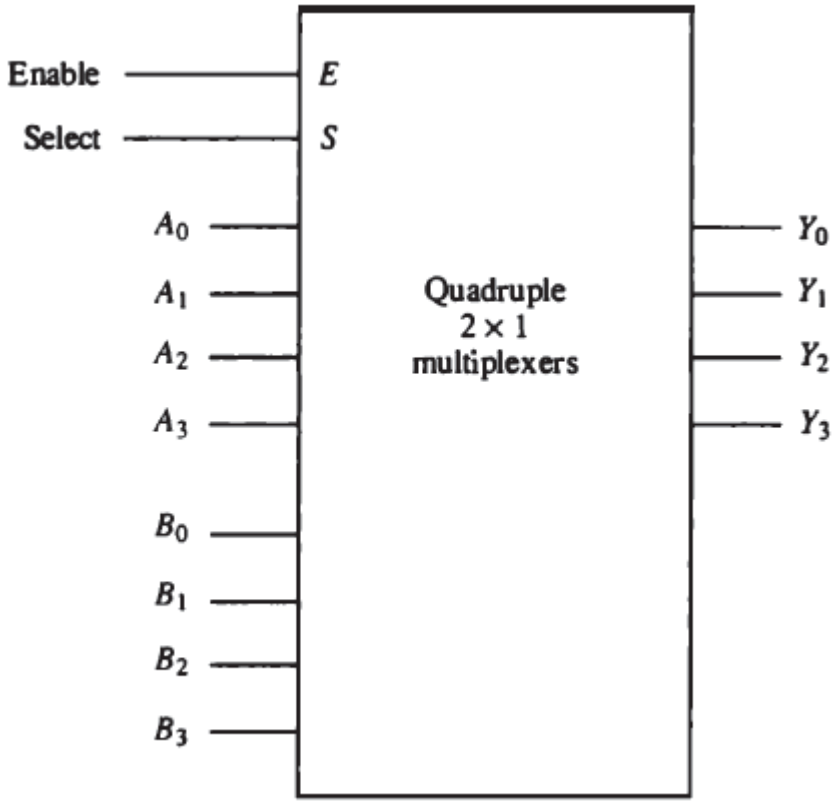


Selection Lines		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Multiplexers

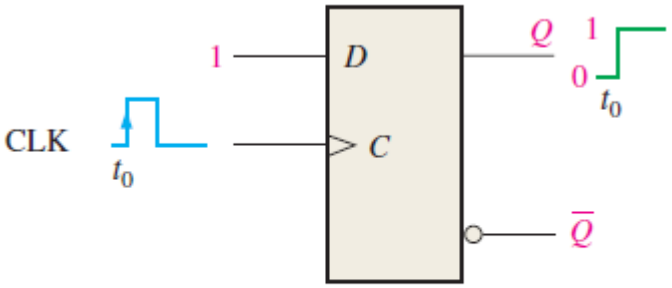


Multiplexers

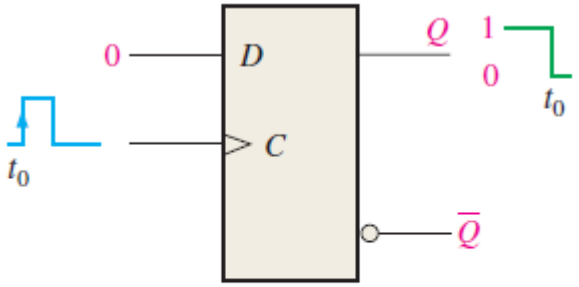


E	S	Y
0	×	All 0's
1	0	A
1	1	B

D Flip-flops



$D = 1$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



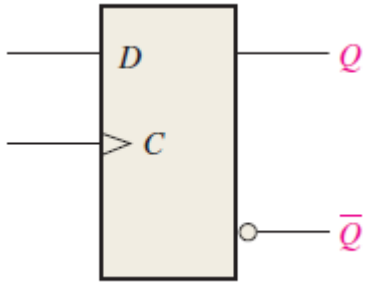
$D = 0$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

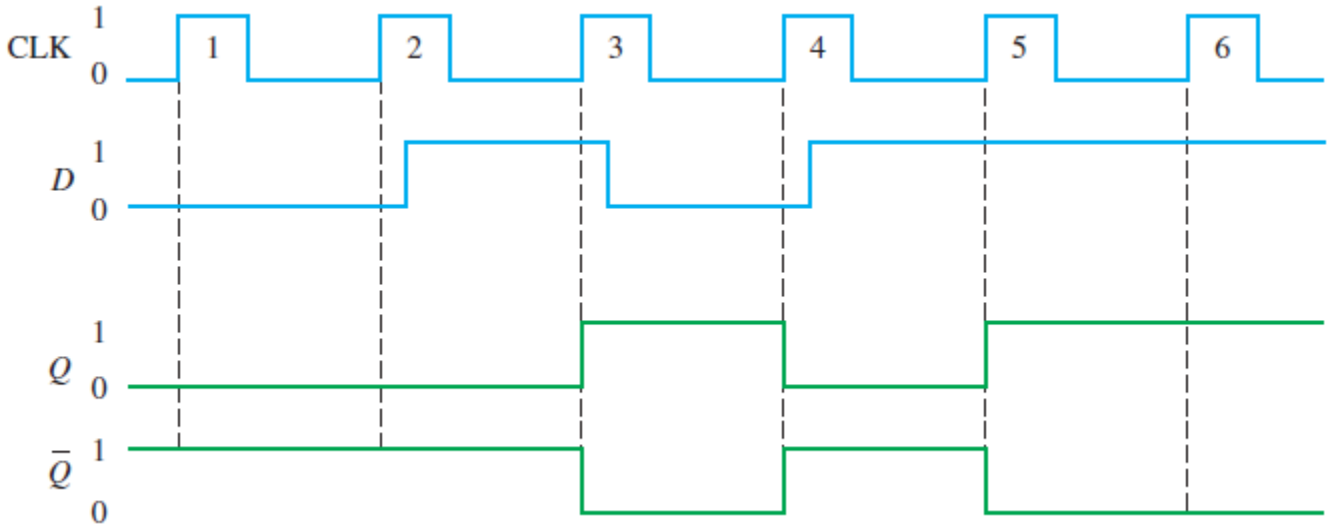
Truth table for a positive edge-triggered D flip-flop.

Inputs		Outputs		
D	CLK	Q	$\overline{Q}$	Comments
0	↑	0	1	RESET
1	↑	1	0	SET

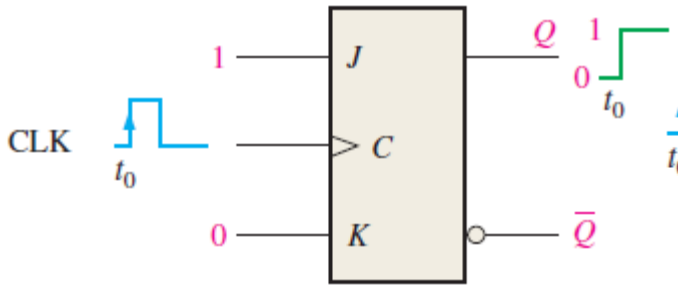
↑ = clock transition LOW to HIGH

D Flip-flops

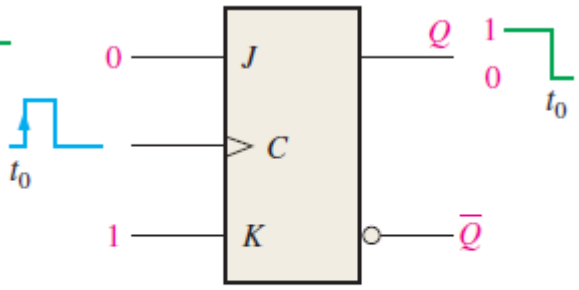




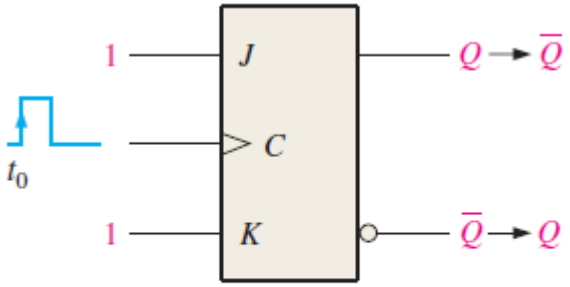
J-K Flip-Flop



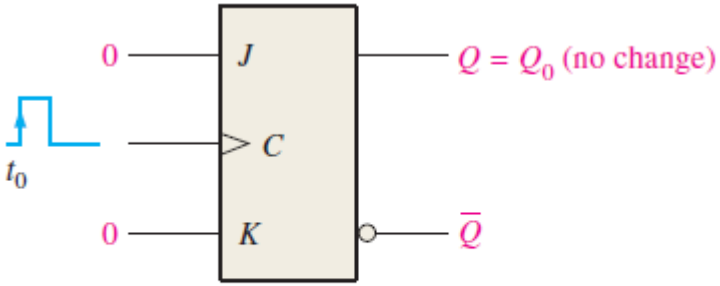
$J = 1, K = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



$J = 0, K = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



$J = 1, K = 1$ flip-flop changes state (toggle).



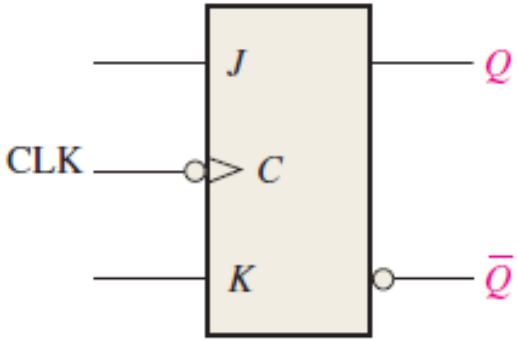
$J = 0, K = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

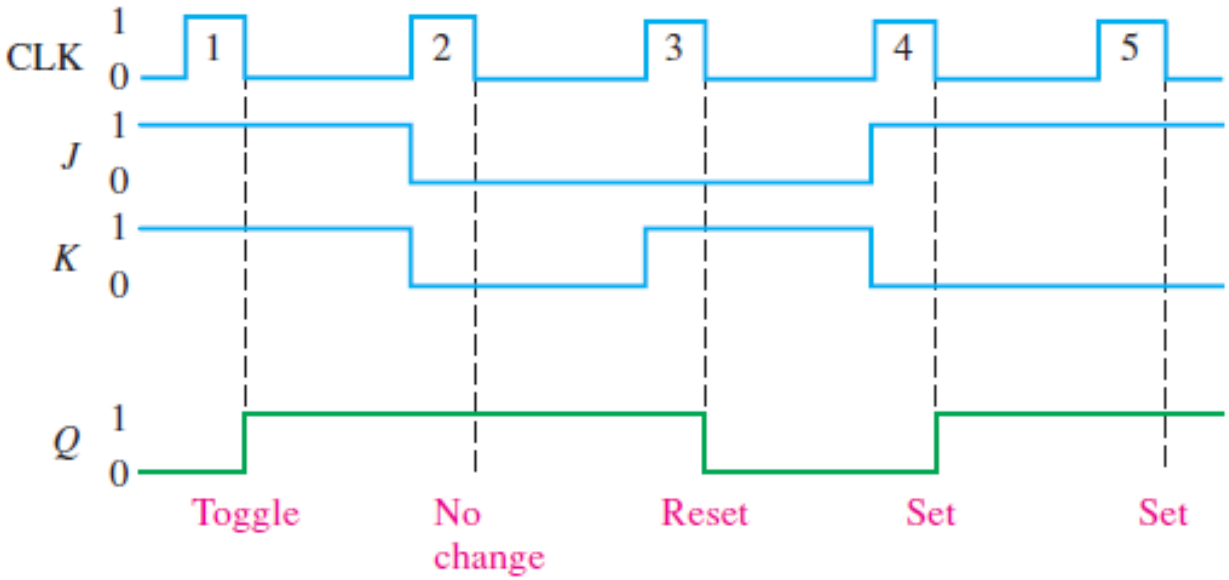
Truth table for a positive edge-triggered J-K flip-flop.

Inputs			Outputs		
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

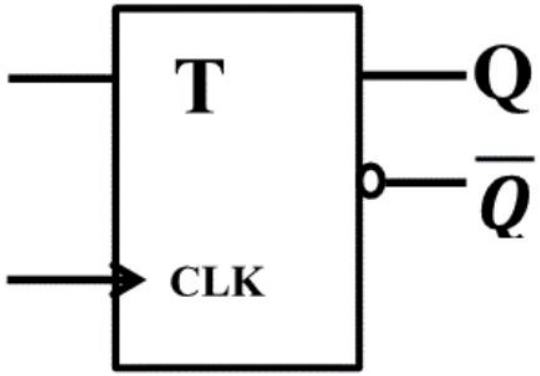
↑ = clock transition LOW to HIGH
Q_0 = output level prior to clock transition

J-K Flip-Flop


J
Q
CLK
C
K
$\overline{Q}$

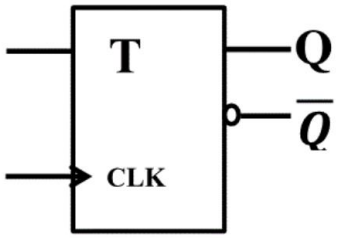

CLK
J
K
Q
1
0
1
2
3
4
5
Toggle
No change
Reset
Set
Set

T Flip-Flop

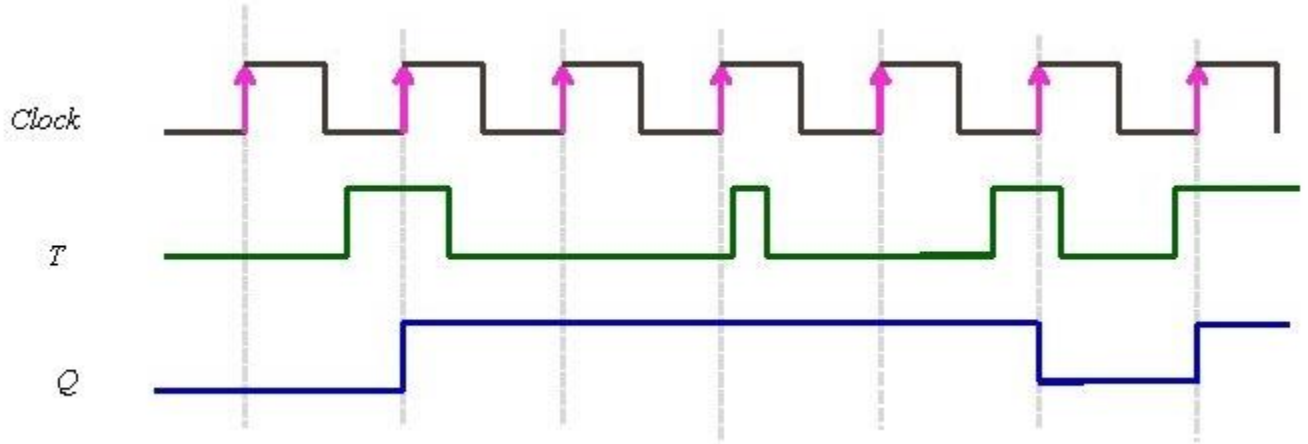


T	Q_{t+1}
0	Q_t
1	$\overline{Qt}$

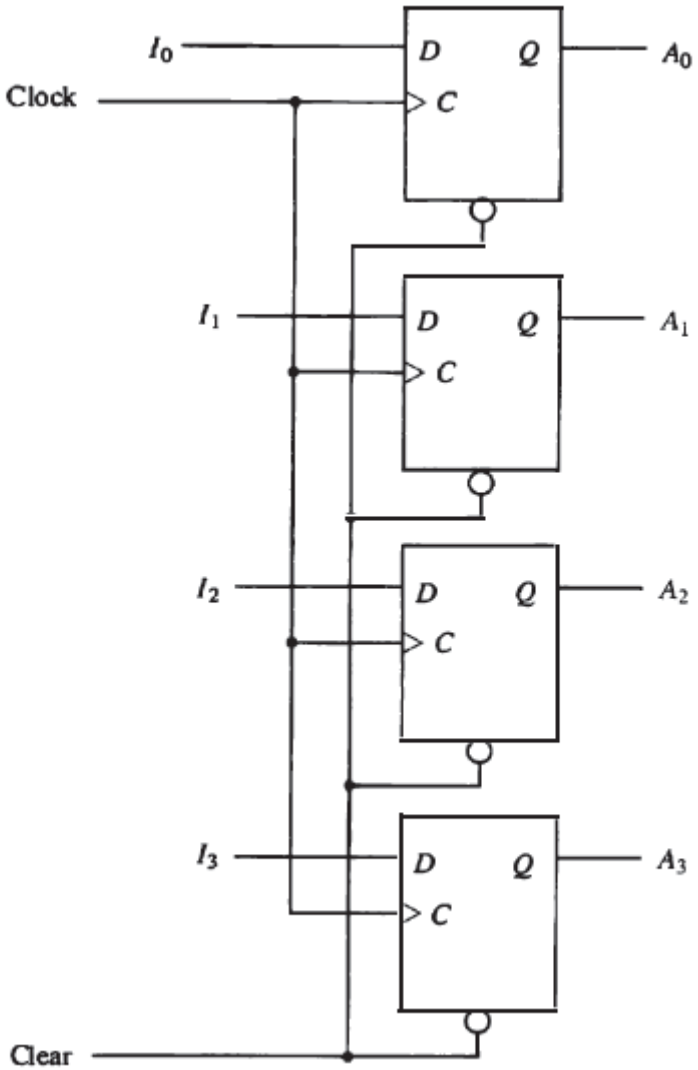
T Flip-Flop



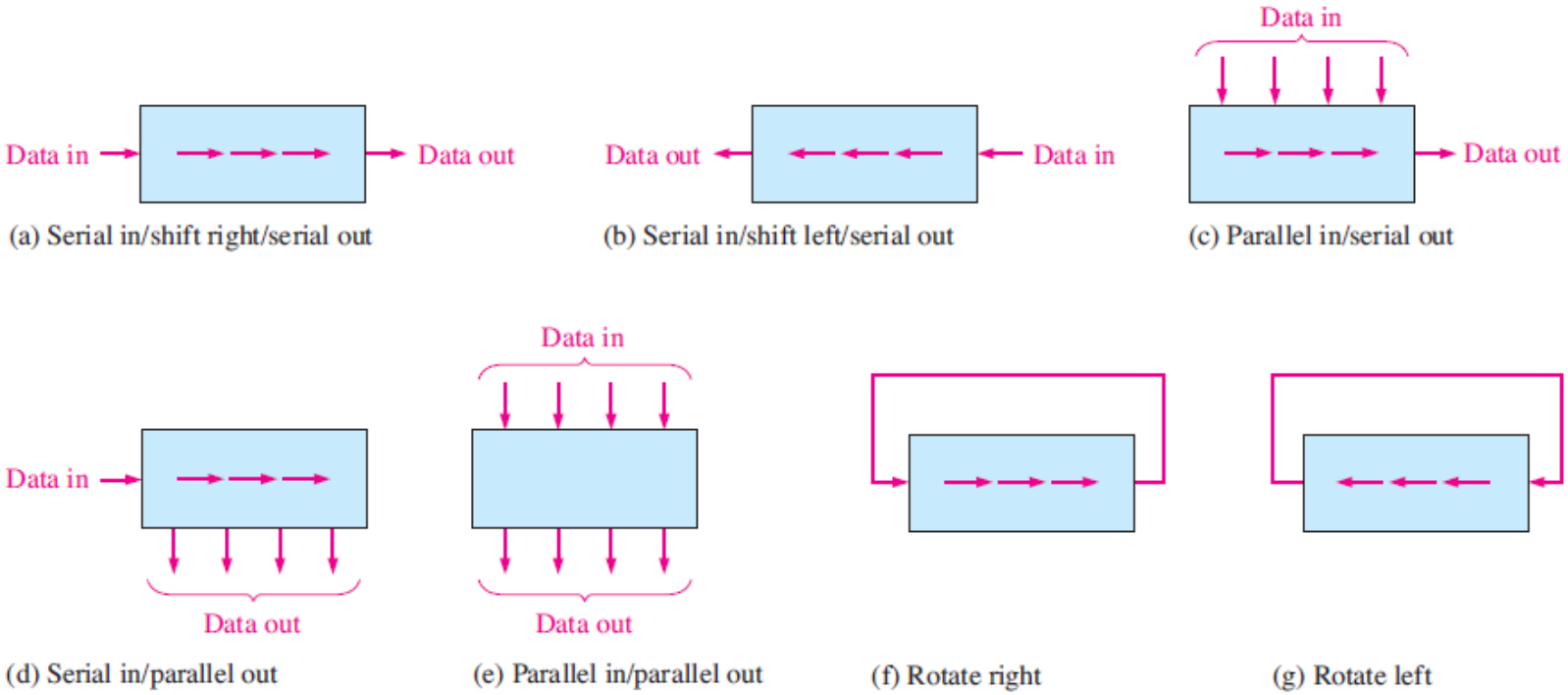
	Previous		Next	
T	Q_{Prev}	Q'_{Prev}	Q_{Next}	Q'_{Next}
0	0	1	0	1
0	1	0	1	0
1	0	1	1	0
1	1	0	0	1

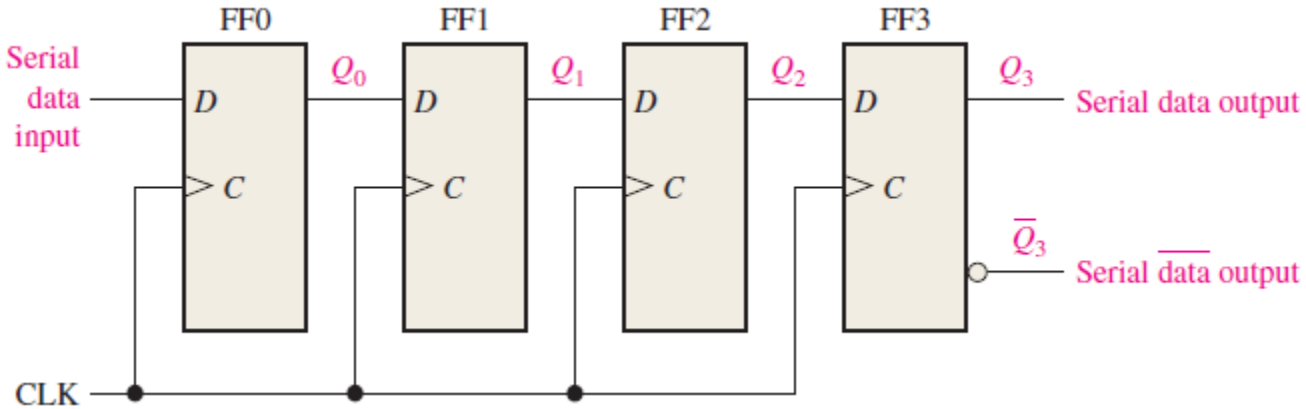


4-bit register

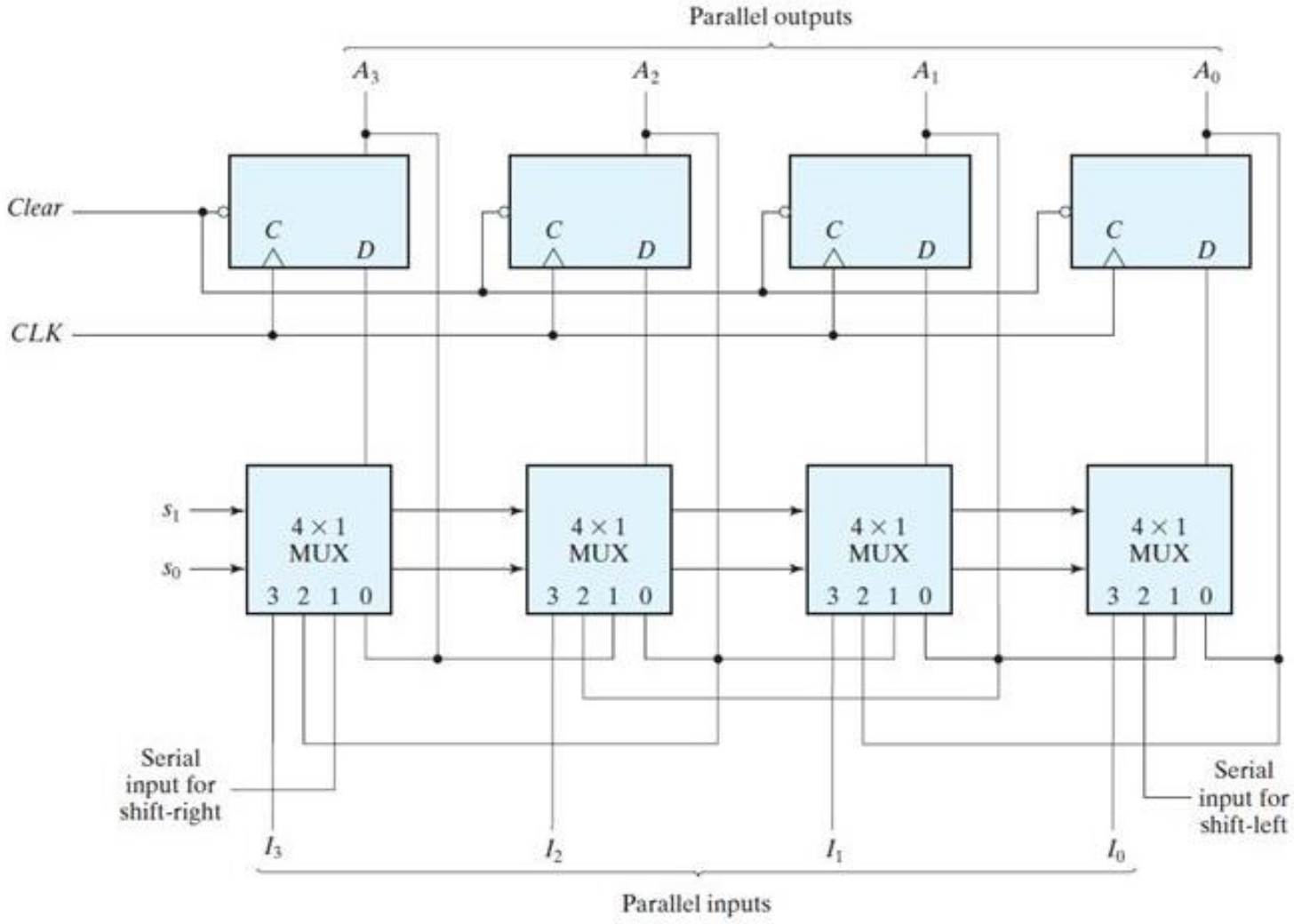


4-bit shift register

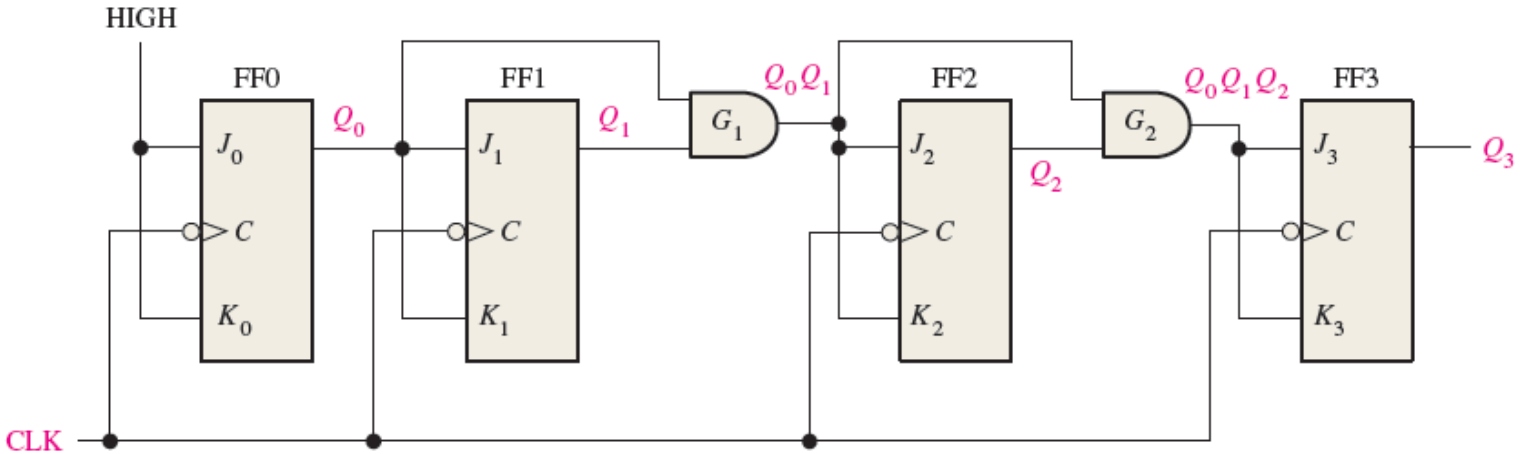


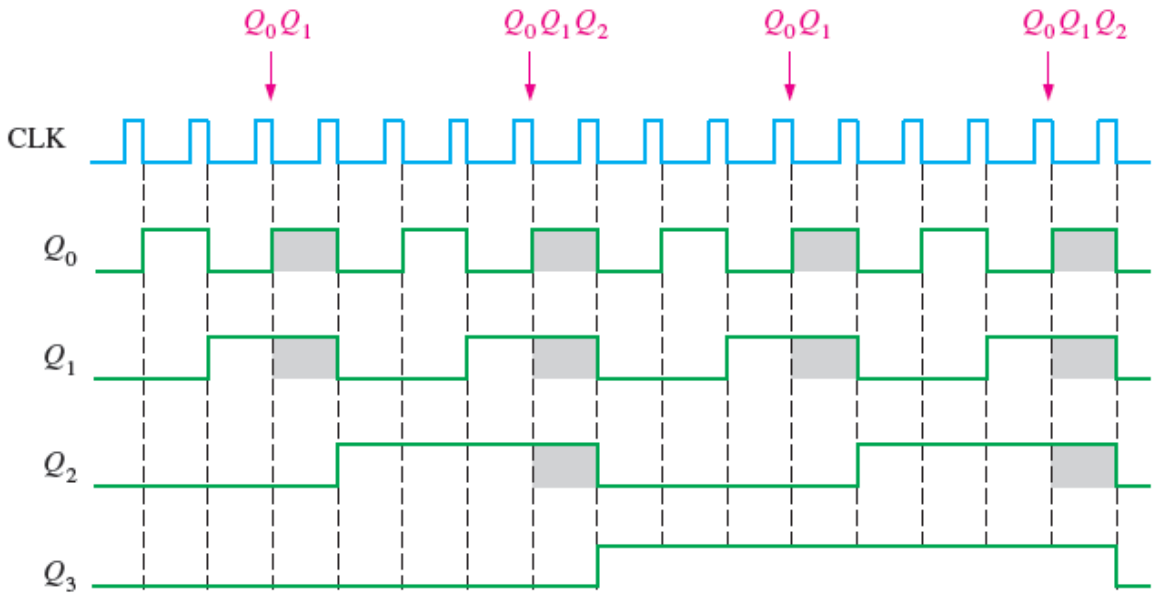


4-bit universal shift register



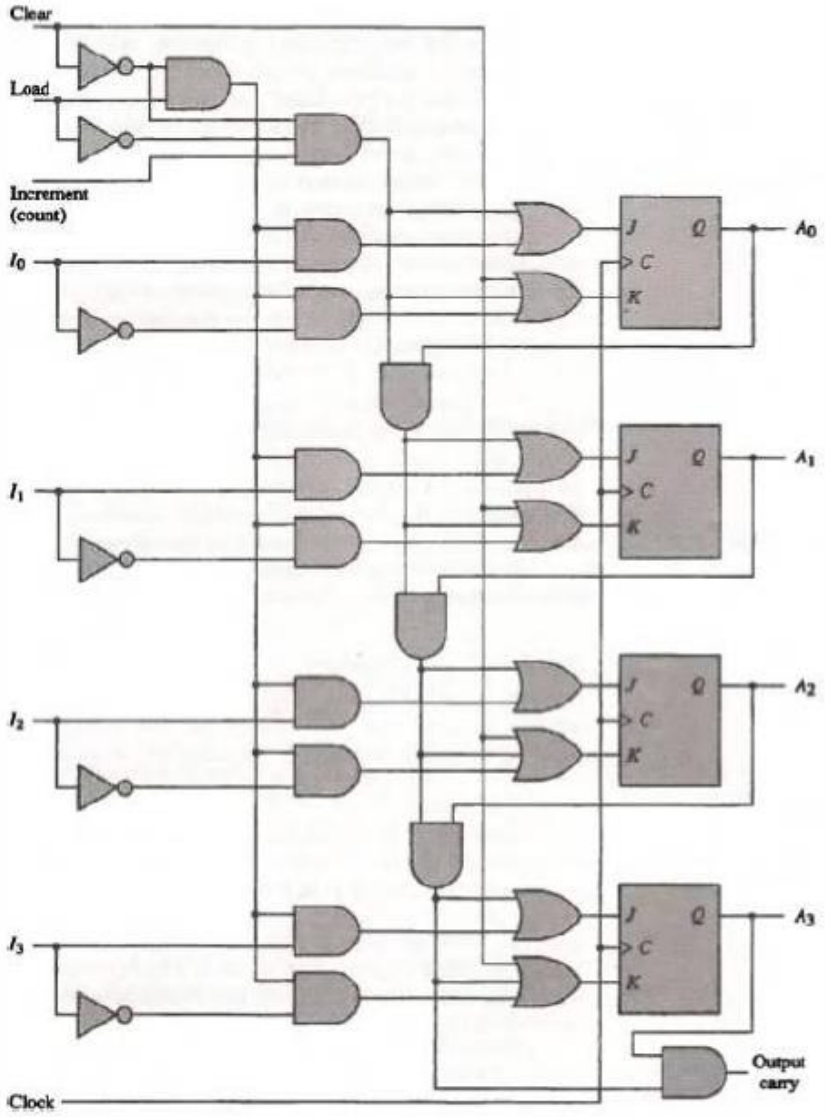
Counter





	toggle Frequency			
	f/16	f/8	f/4	f/2
Decimal	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Binary Counter with Parallel Load



پایان

موفق و پیروز باشید