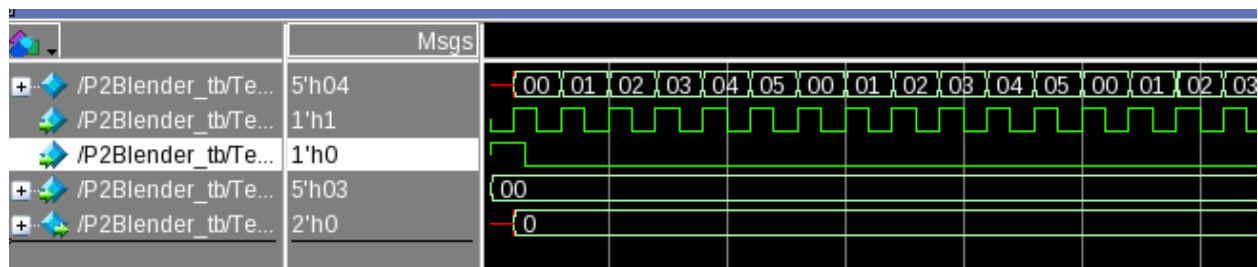
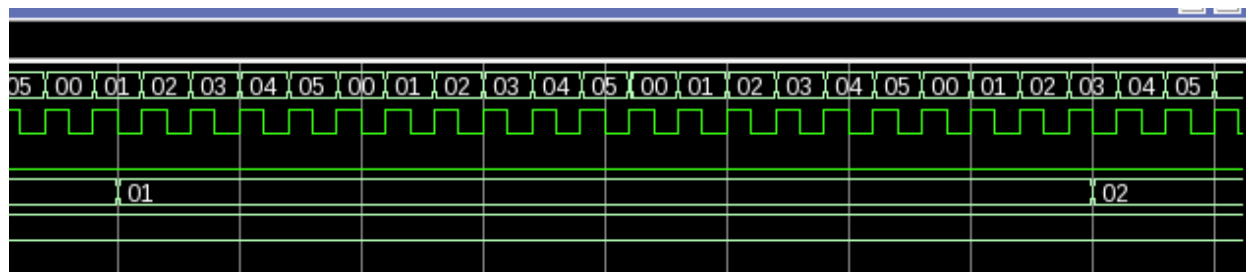


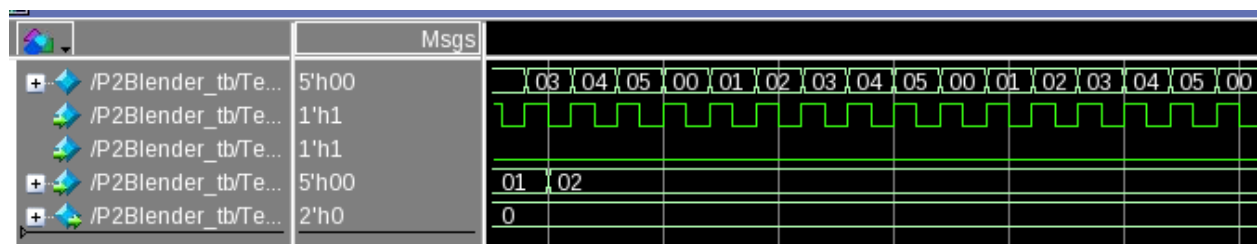
Daniel Li 50995133 Cadence



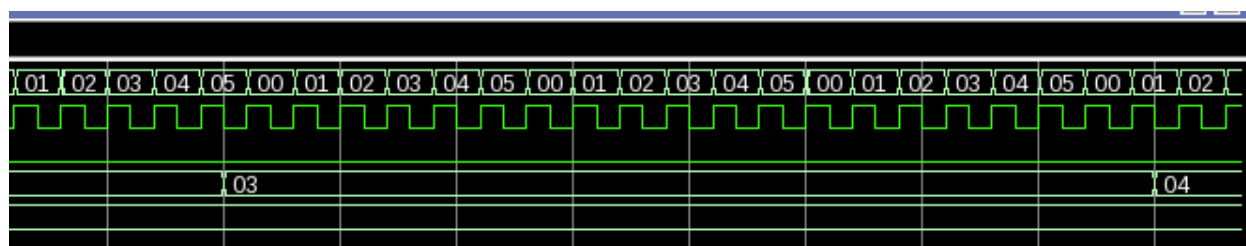
The changing of states for input mode 00, transitions from 00 to 05, which are the null states so output is 00



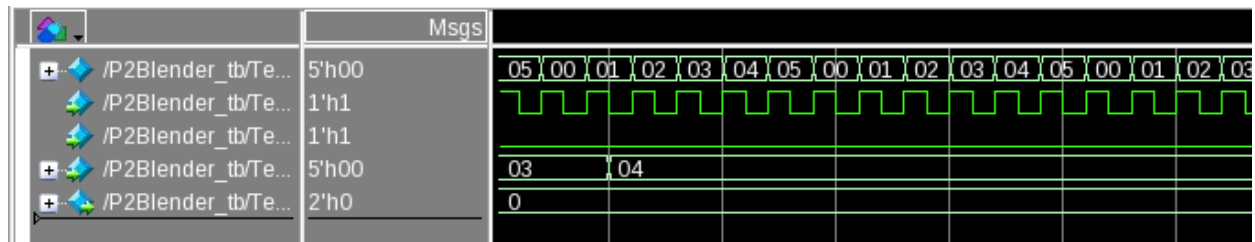
The changing of states for input mode 01, transitions from 00 to 05, which are the null states so output is 00



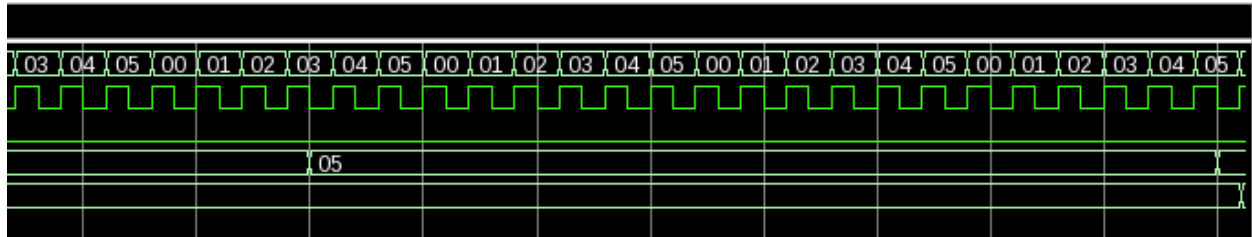
The changing of states for input mode 02, transitions from 00 to 05, which are the null states so output is 00



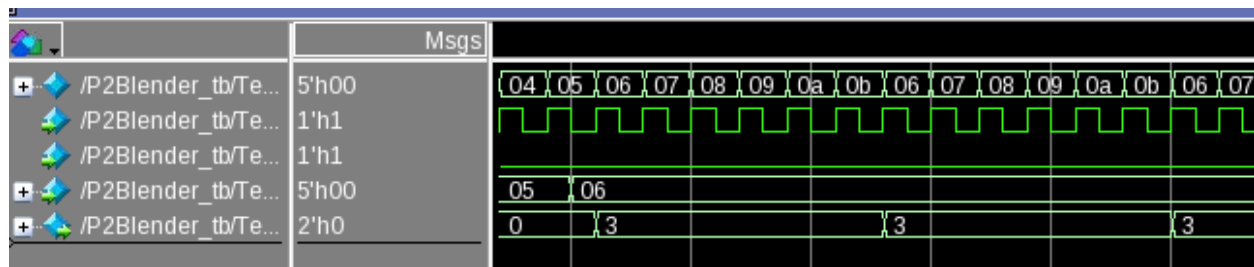
The changing of states for input mode 03, transitions from 00 to 05, which are the null states so output is 00



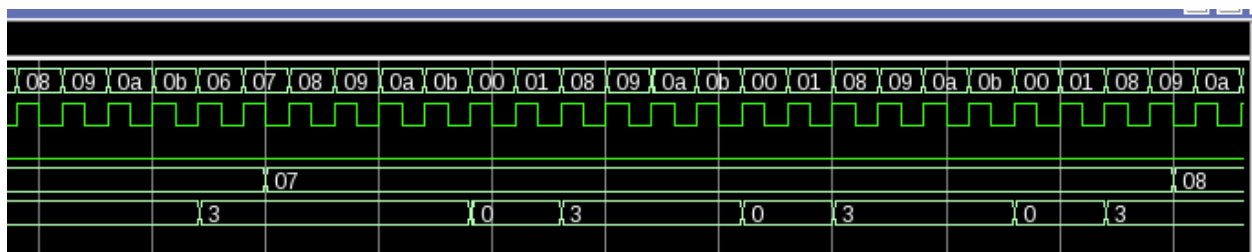
The changing of states for input mode 04, transitions from 00 to 05, which are the null states so output is 00



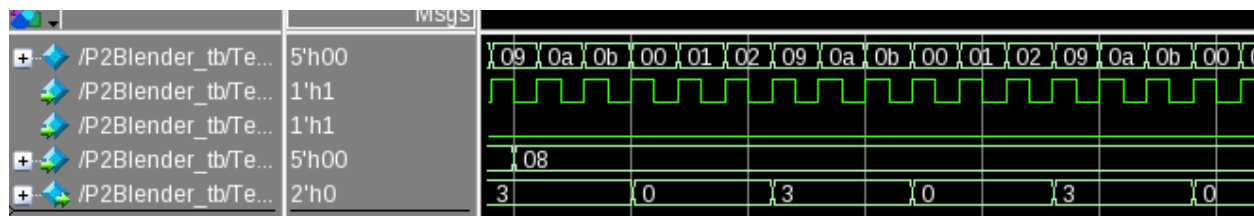
The changing of states for input mode 05, transitions from 00 to 05, which are the null states so output is 00



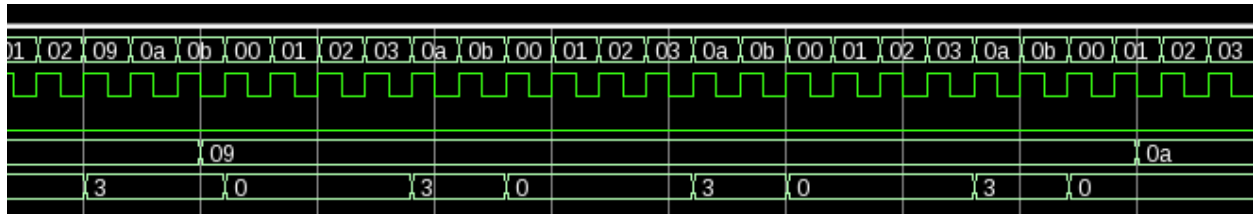
The changing of states for input mode 06, transitions from 06 to 11, which are the high-power states so output is 3



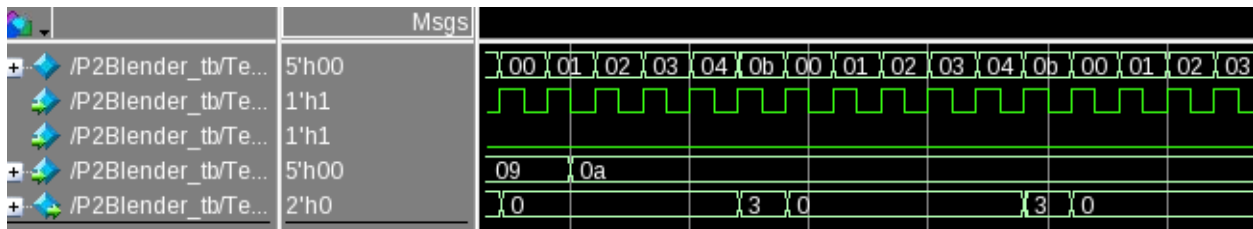
The changing of states for input mode 07, transitions from 06 to 11, which are the high-power states so output is 3



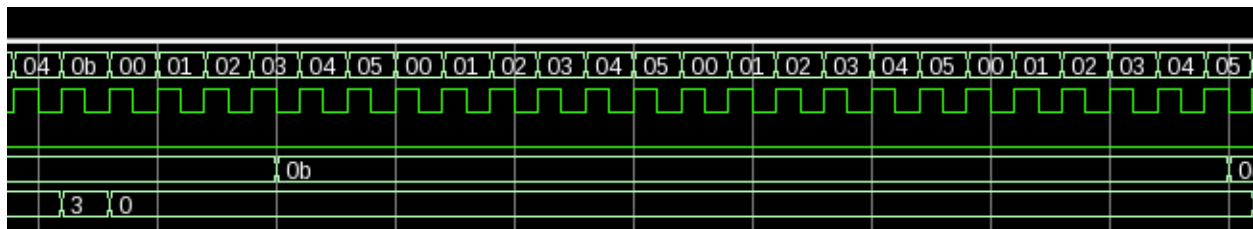
The changing of states for input mode 08, transitions from 06 to 11, which are the high-power states so output is 3



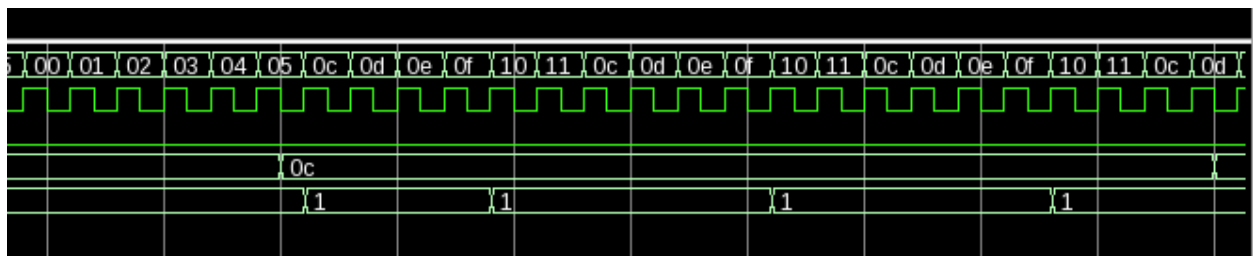
The changing of states for input mode 09, transitions from 06 to 11, which are the high-power states so output is 3



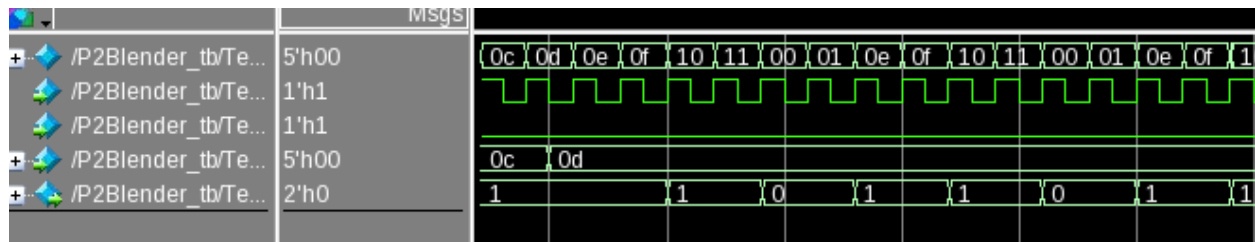
The changing of states for input mode 10, transitions from 06 to 11, which are the high-power states so output is 3



The changing of states for input mode 11, transitions from 06 to 11, which are the high-power states so output is 3, but the duty cycle is 0 in this final mode



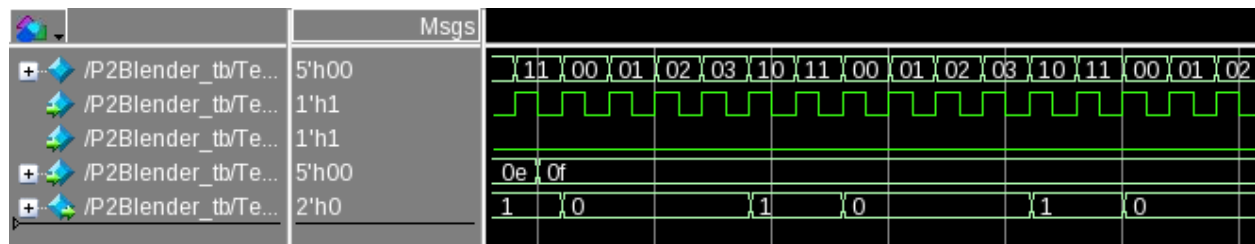
The changing of states for input mode 12, transitions from 12 to 17, which are the low-power states so output is 1



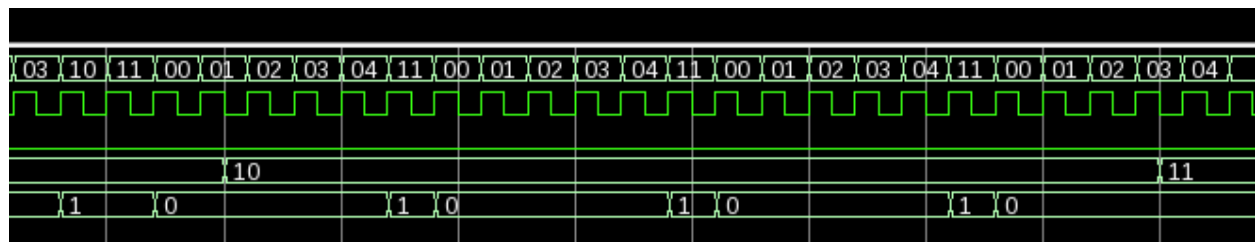
The changing of states for input mode 13, transitions from 12 to 17, which are the low-power states so output is 1



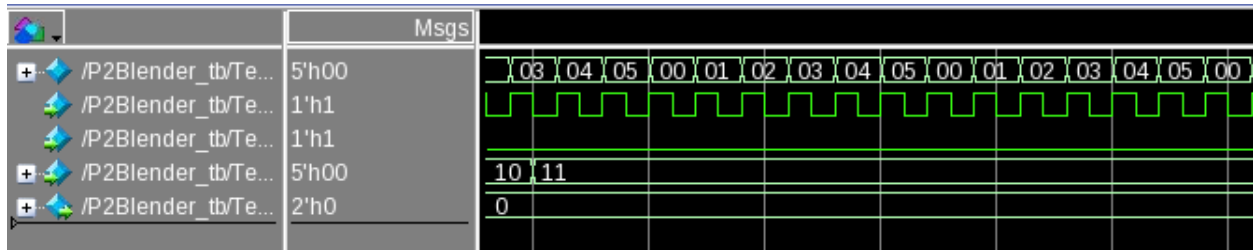
The changing of states for input mode 14, transitions from 12 to 17, which are the low-power states so output is 1



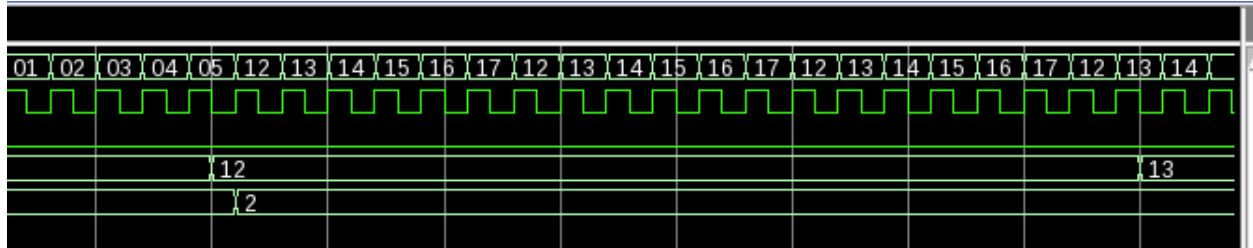
The changing of states for input mode 15, transitions from 12 to 17, which are the low-power states so output is 1



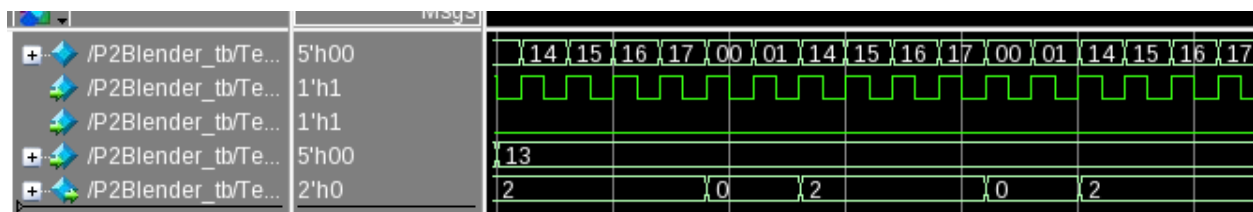
The changing of states for input mode 16, transitions from 12 to 17, which are the low-power states so output is 1



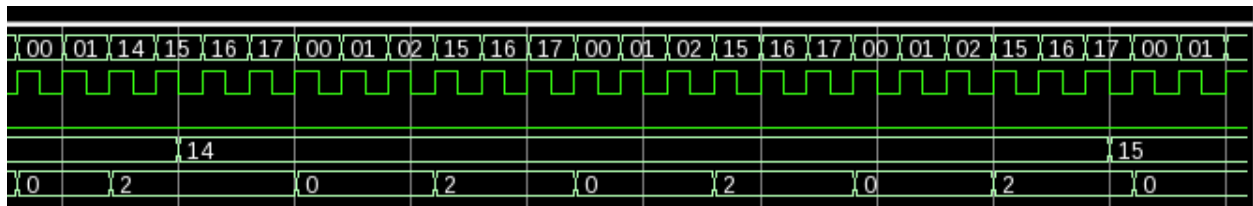
The changing of states for input mode 17, transitions from 12 to 17, which are the low-power states so output is 1. However, the duty cycle is 0, so there is no output.



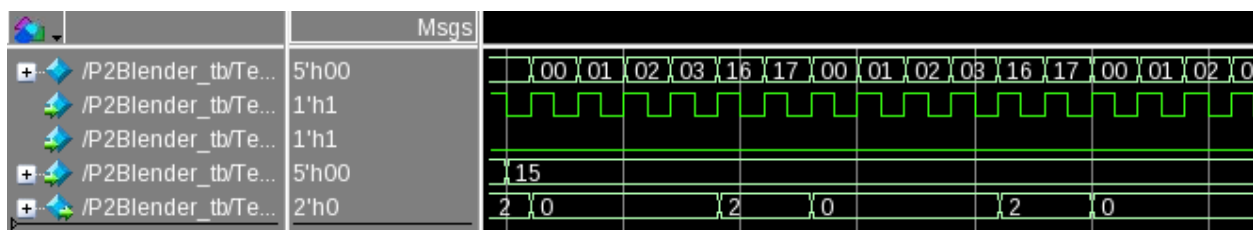
The changing of states for input mode 18, transitions from 18 to 23, which are the medium-power states so output is 2



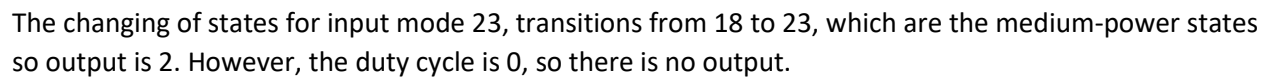
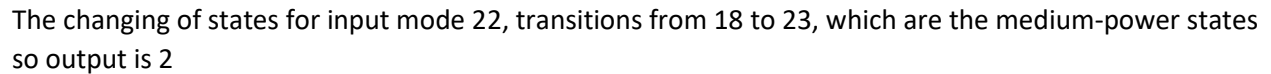
The changing of states for input mode 19, transitions from 18 to 23, which are the medium-power states so output is 2



The changing of states for input mode 20, transitions from 18 to 23, which are the medium-power states so output is 2

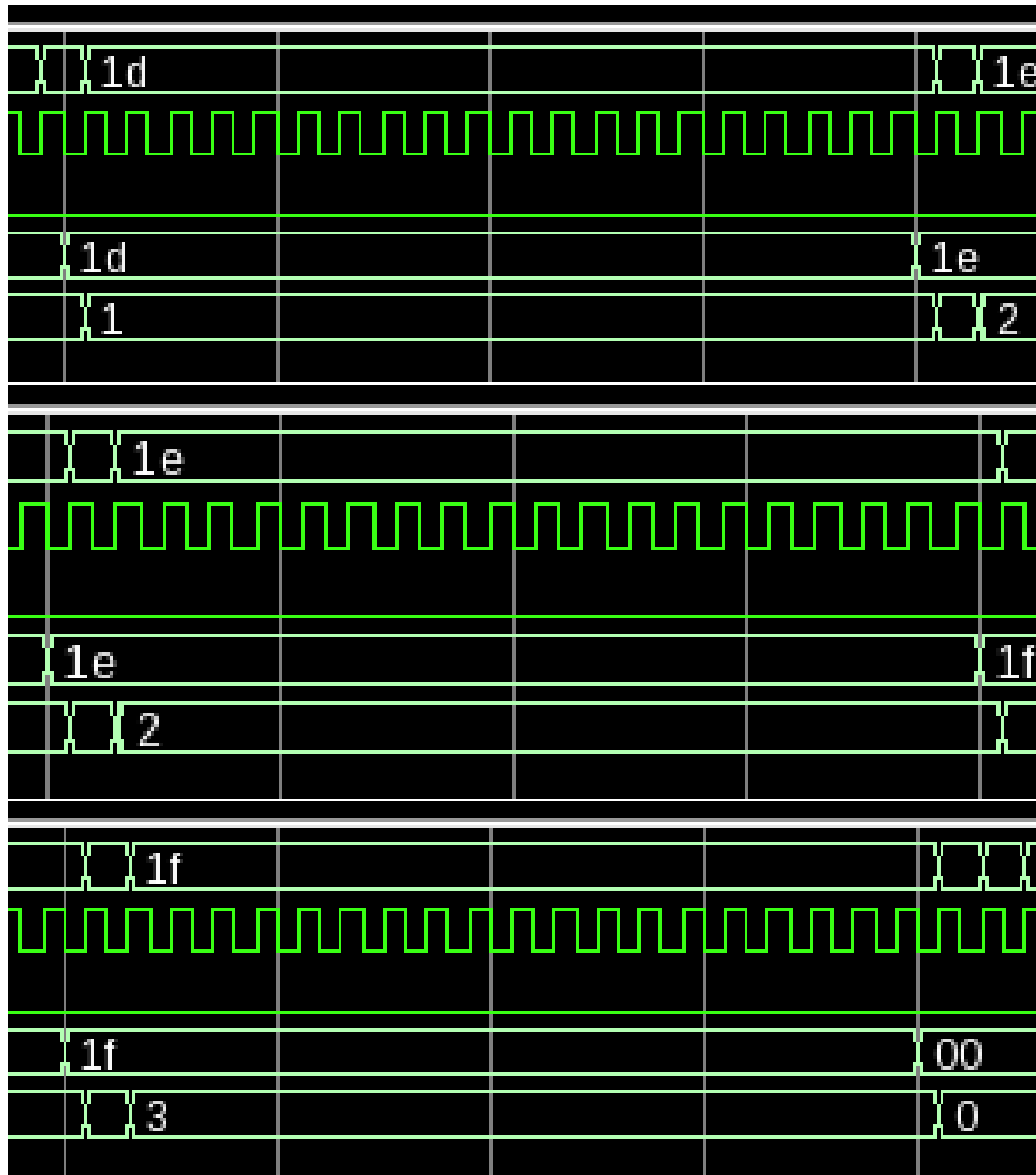


The changing of states for input mode 21, transitions from 18 to 23, which are the medium-power states so output is 2



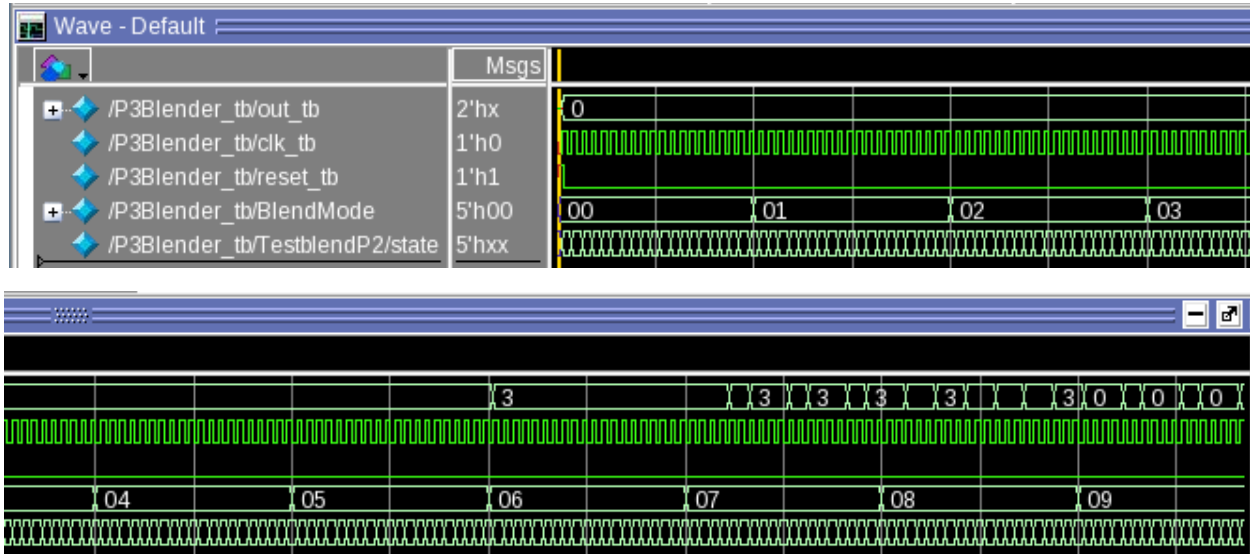
Timing diagram for the first two clock cycles of the 100 MHz clock. The diagram shows a green square wave for the clock signal. Below it, two horizontal lines are labeled '18' and '19', representing the clock cycle numbers. The clock signal is high for the first half of each cycle and low for the second half.

The last 3 states (29, 30 and 31) are all Pulse states, which means for as long as the button is pressed down (shown by the input mode) they will be at Low (29, Output 1), Medium (30, Output 2), or High (31, Output 3)

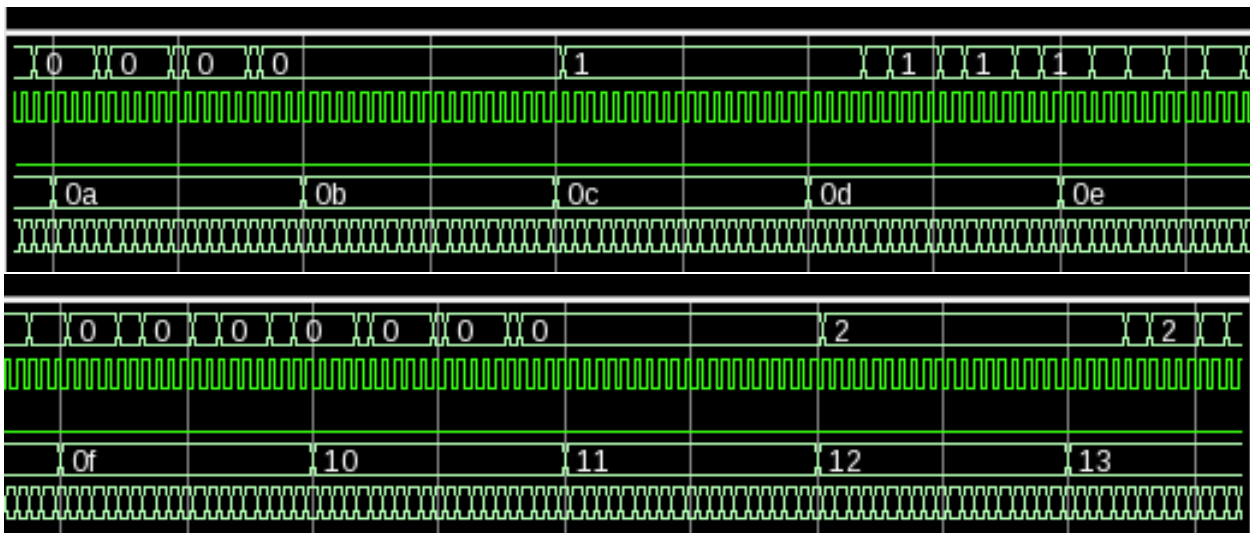


(The mode input display is in hexadecimal on Modelsim, even if I've mentioned the mode input in the report in decimal)

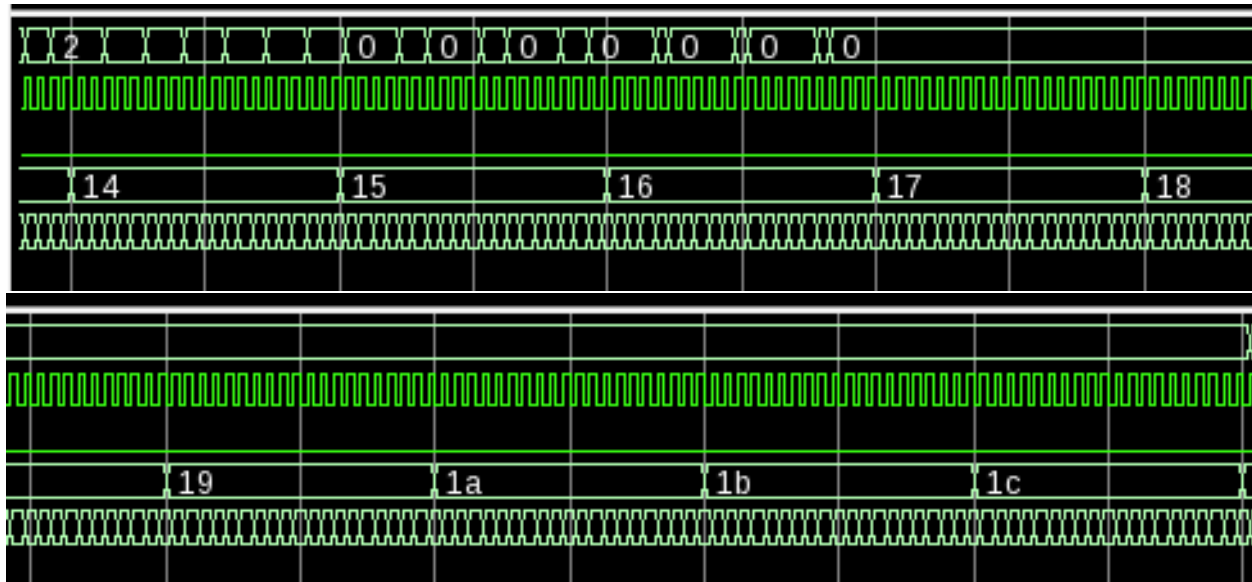
Project 2 differs from Project 1 by doubling the number of states. Although some new calculations have been introduced, fundamentally they are the same project. I have included the .sv files of both the Testbench of Project 2 and the Project 2 itself. The above files were all generated from the Cadence compiled .v file and as can be noted, there are no differences in simulation.



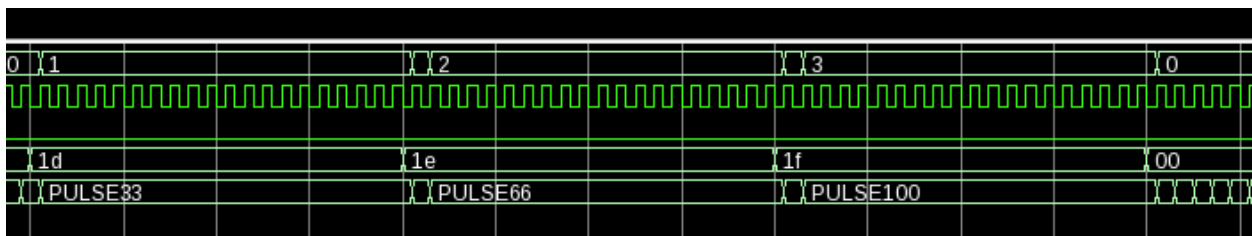
As seen, the conditions are still the same, with the first 6 modes (0 to 5) having 0 output, and the next few modes having a changing duty cycle for the highest level of output.



The next ones are the low-power states with reducing duty cycles, such that input mode 6 would have the highest duty cycle for that level of output, as would 12 and 18.



The blank states (23 – 28) are still the same on both the .sv and the .v files, as can be seen here.



The Pulse states are the same and have identical waveforms.

49	OAI22X1	2	4.104	slow_vddiv0
50	OAI2BB1X1	2	3.420	slow_vddiv0
51	OAI31X1	4	8.208	slow_vddiv0
52	OR2X1	4	5.472	slow_vddiv0
53	OR2XL	3	4.104	slow_vddiv0
54	OR4X1	3	6.156	slow_vddiv0
55	-----			
56	total	182	266.076	
57				
58				
59				
60	Type	Instances	Area	Area %
61	-----			
62	sequential	5	27.360	10.3
63	inverter	26	17.784	6.7
64	logic	151	220.932	83.0
65	-----			
66	total	182	266.076	100.0
67				
68				

Included is a screenshot of the report.