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UNIVERSITY OF TEHRAN

Report for Computer Assignment 2

Instructor : Dr. Navabi

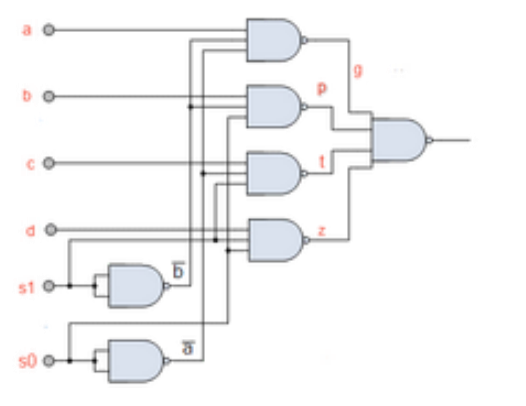
**Digital Logic Design, ECE 367 / Digital Systems I, ECE 894**

Danial Saeedi

Problem 1

From problem 1 in Computer Assignment 1, we know that the delays for 2, 3 and 4 input NAND gates are #(10,8), #(15,12) and #(20,16).

For simplicity, we assign the average of To0 and To1 delays. So the average delays for 2, 3 and 4 inputs are #9, #13 and #18.

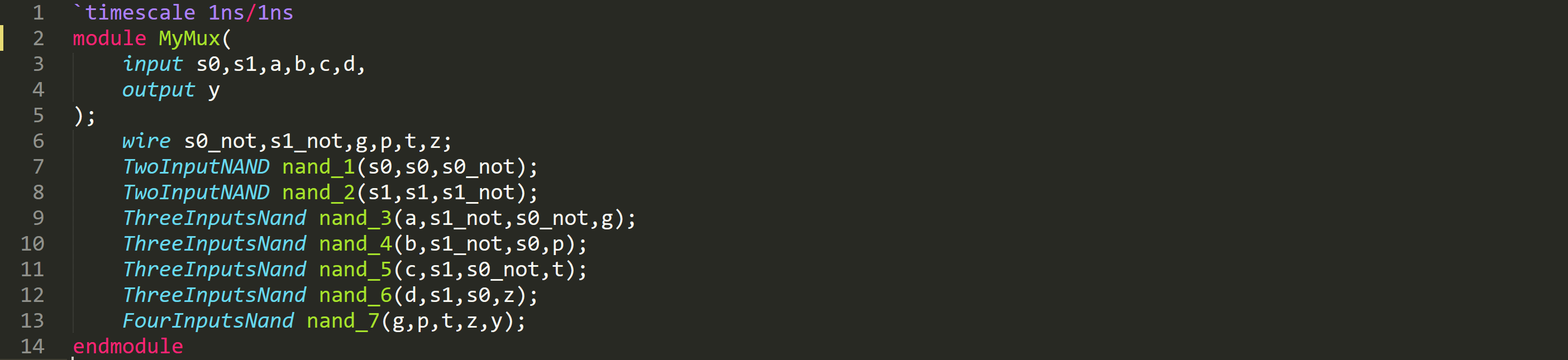


The worst-case delay of this circuit is :

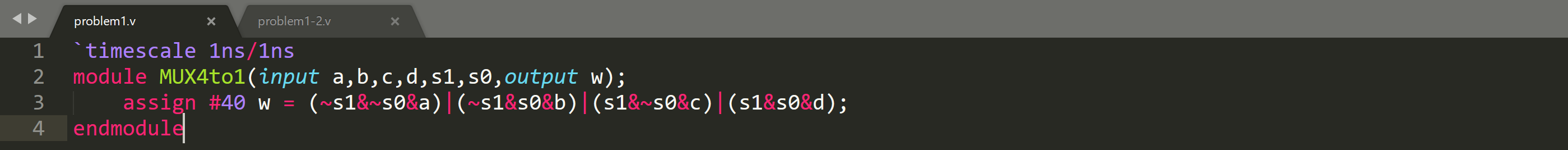
9+13+18 = 40ns

**Verilog Code**

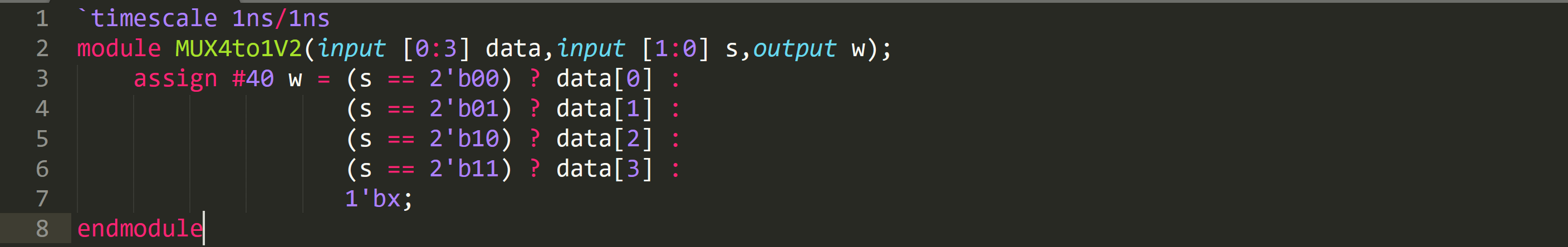
4 to 1 MUX implementation in Computer Assignment 1 :



MUX-CA1.v



Problem1.v



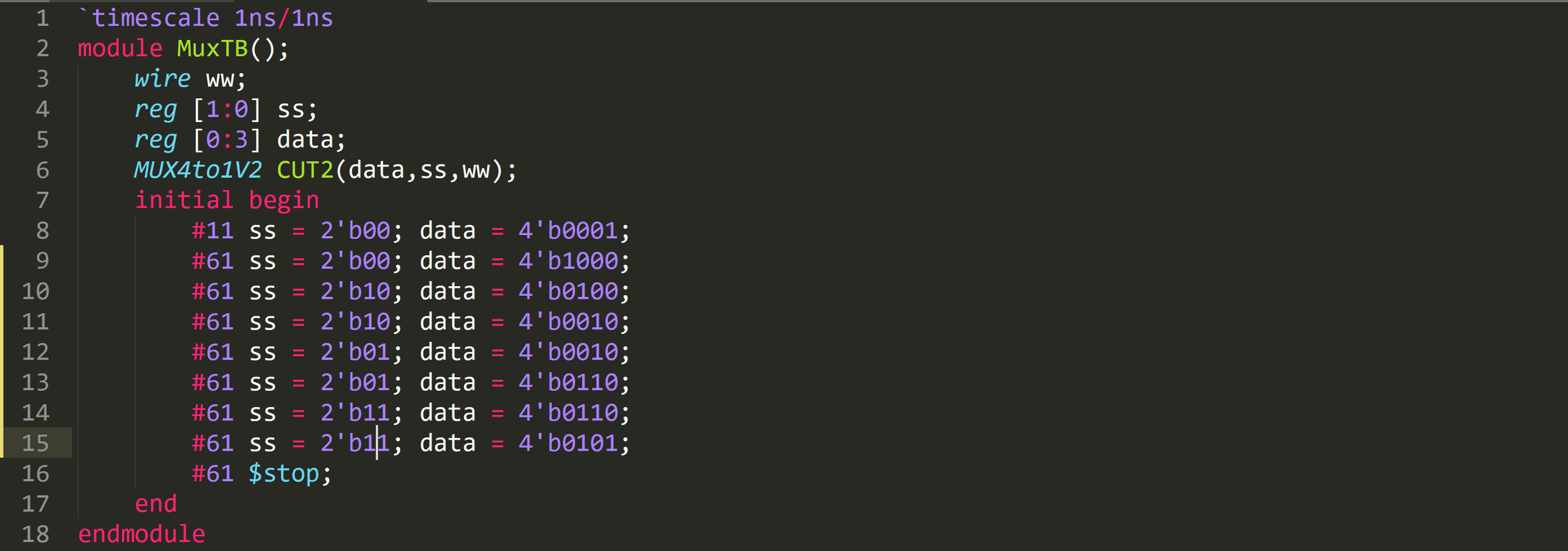
Problem1-2.v

**Worst-case Delay**

Every possible input has 40ns delay because we are using assign statement. So the worst-case delay is **40ns** in this problem.

**Testbench**

The ww1 and ww3 wires are the output of 3 different implementation of MUX.



TB-MUX.v

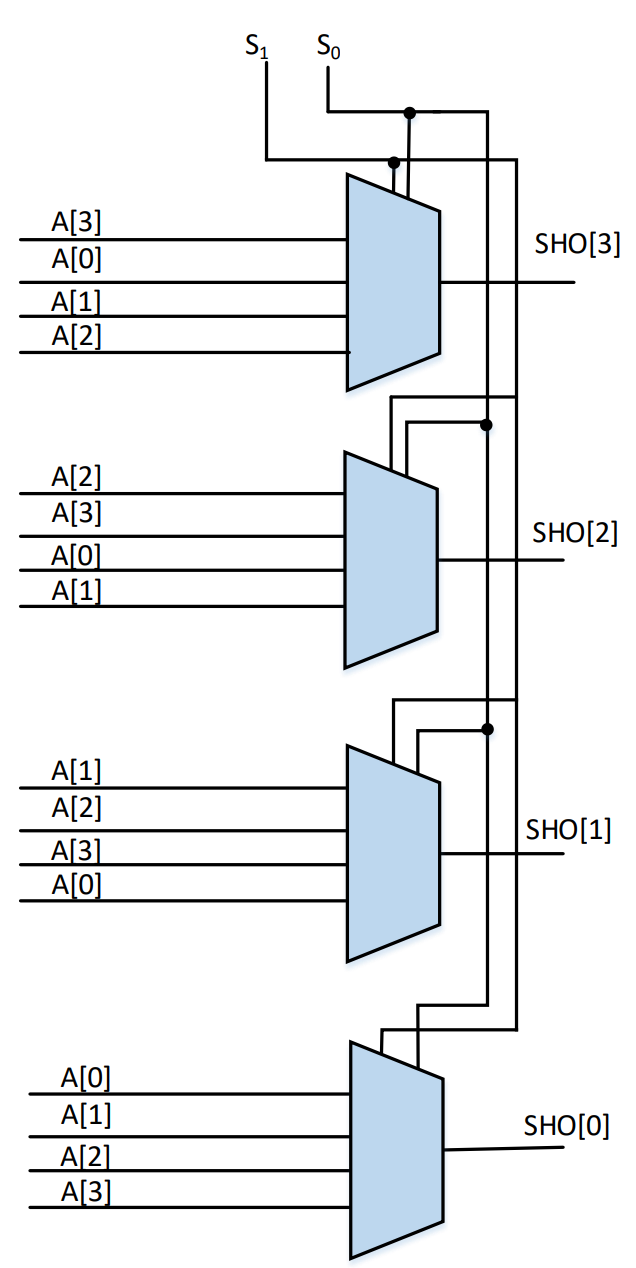
**Simulation Result**



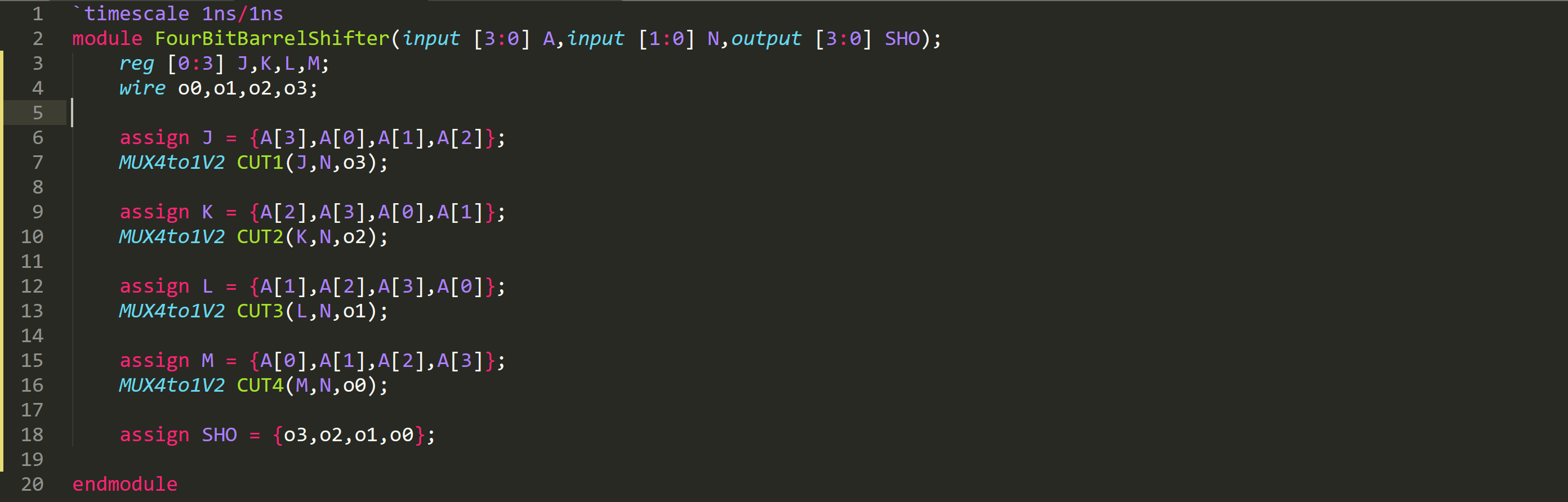
The worst-case delay is 40ns.

Problem 2

**Circuit Diagram**



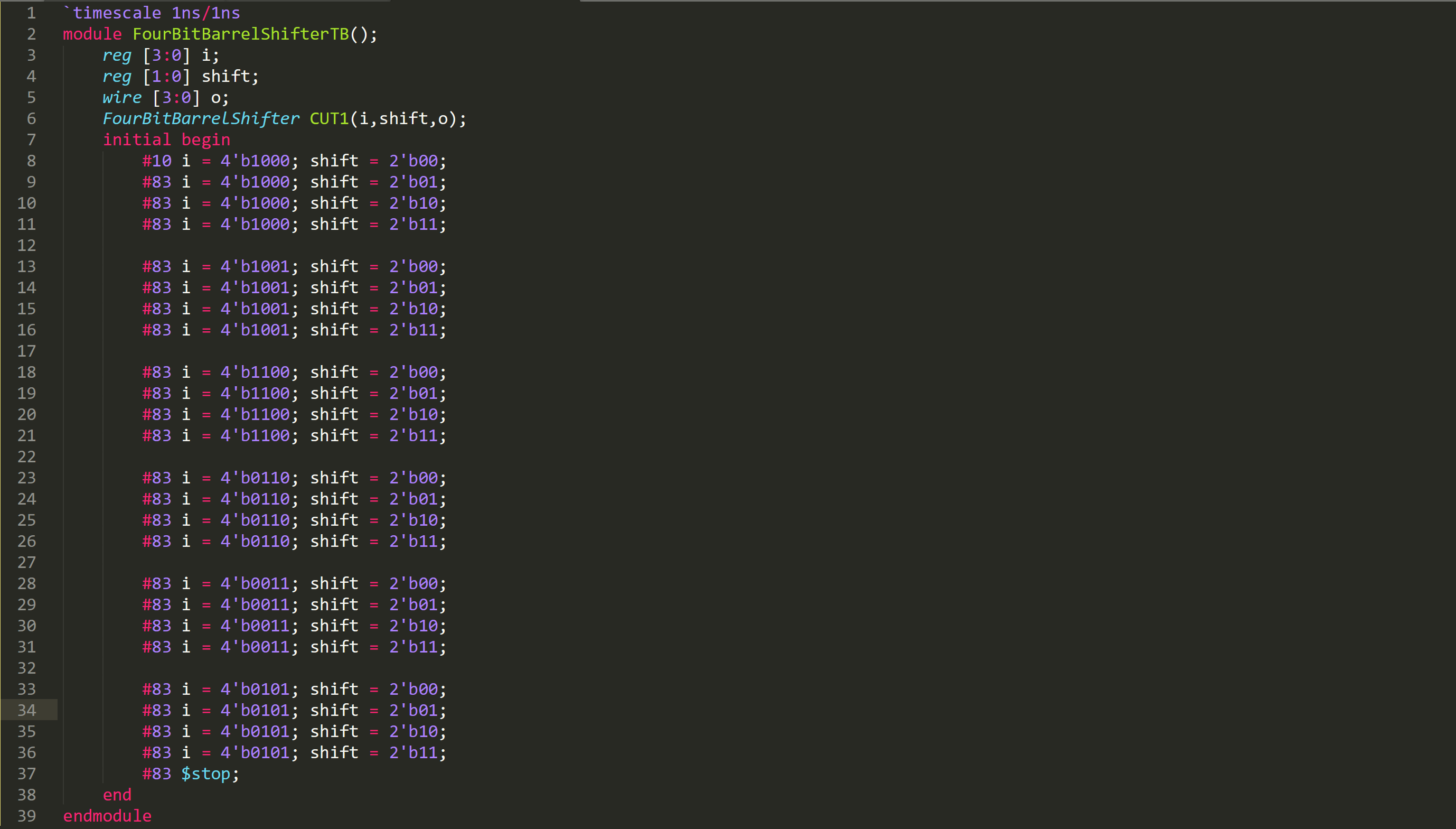
**Verilog Code**



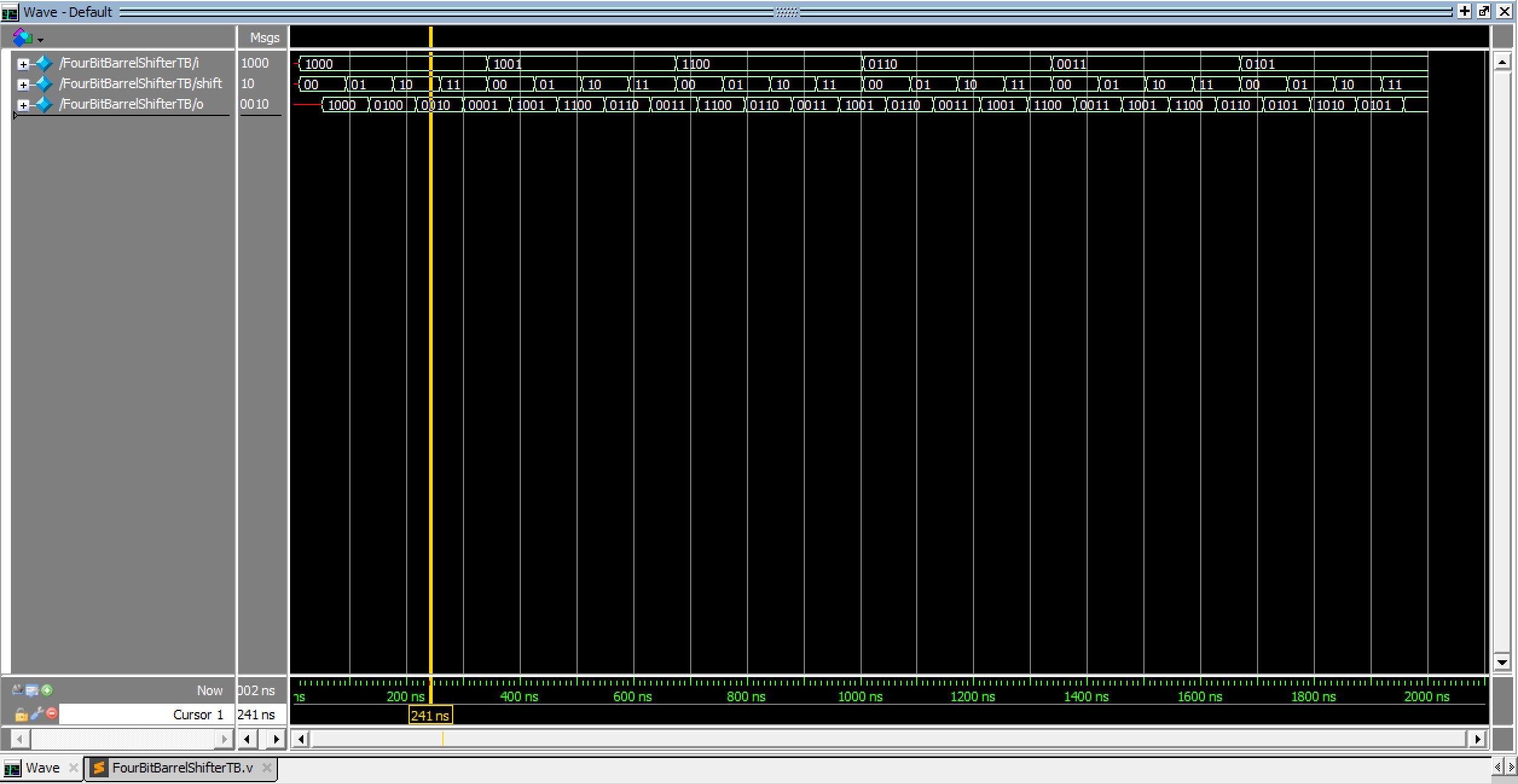
FourBitBarrelShifter.v

**Testbench**

i,shift and o represent input, shift value and output.



**Simulation Result**



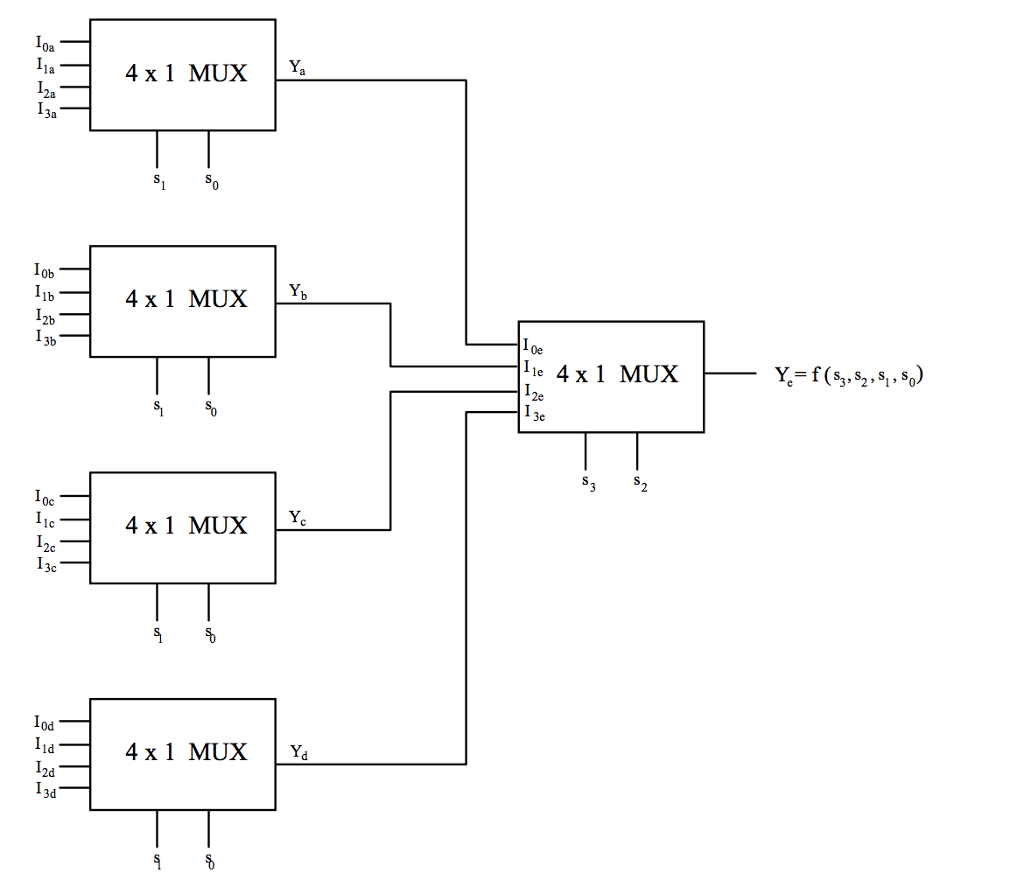
**Worst-case Delay**

Each 4 to 1 MUX has 40ns delay. So we expect worst-case delay would be **around 40ns**.

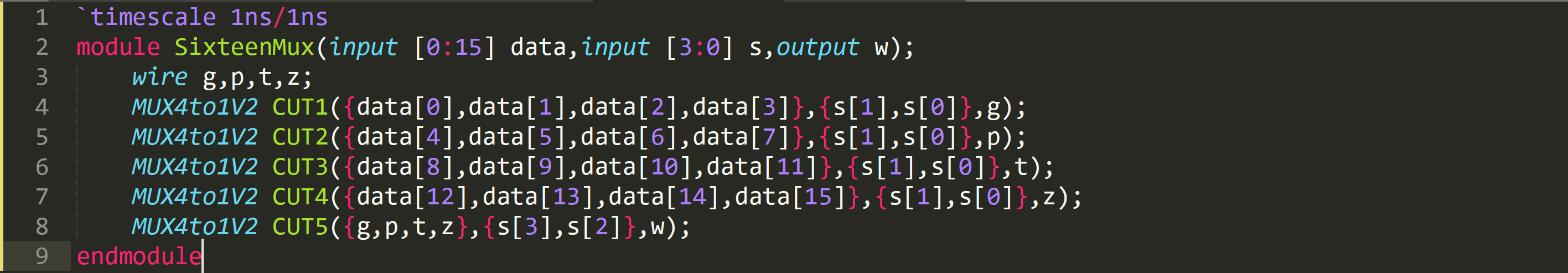
The waveform proves that the worst-case delay is **40ns**.

Problem 3

**Circuit Diagram**

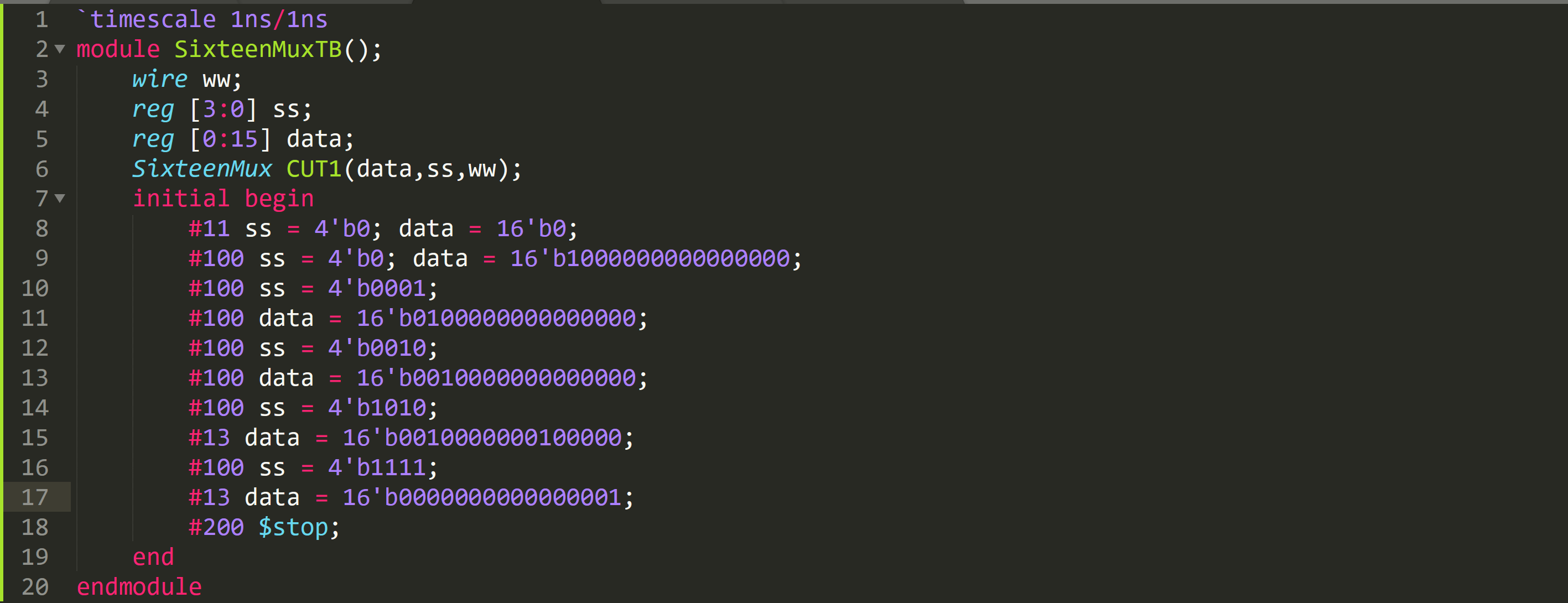


**Verilog Code**



SixteenMux.v

**Testbench**



**Simulation Result**



SixteenMuxTB.v

**Worst-case Delay**

Every path goes through 2 Muxes. So the worst-case delay is :

40 + 40 = 80ns

We can see from waveform, the worst-case delay is also 80ns.

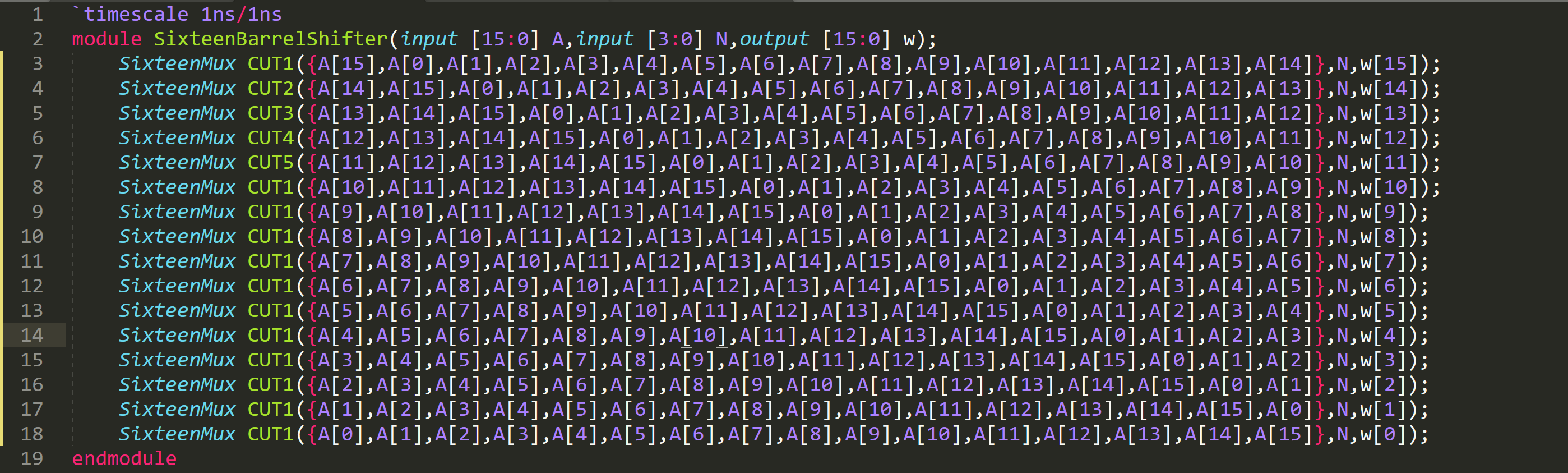
Problem 4

16-bit Barrel Shifter

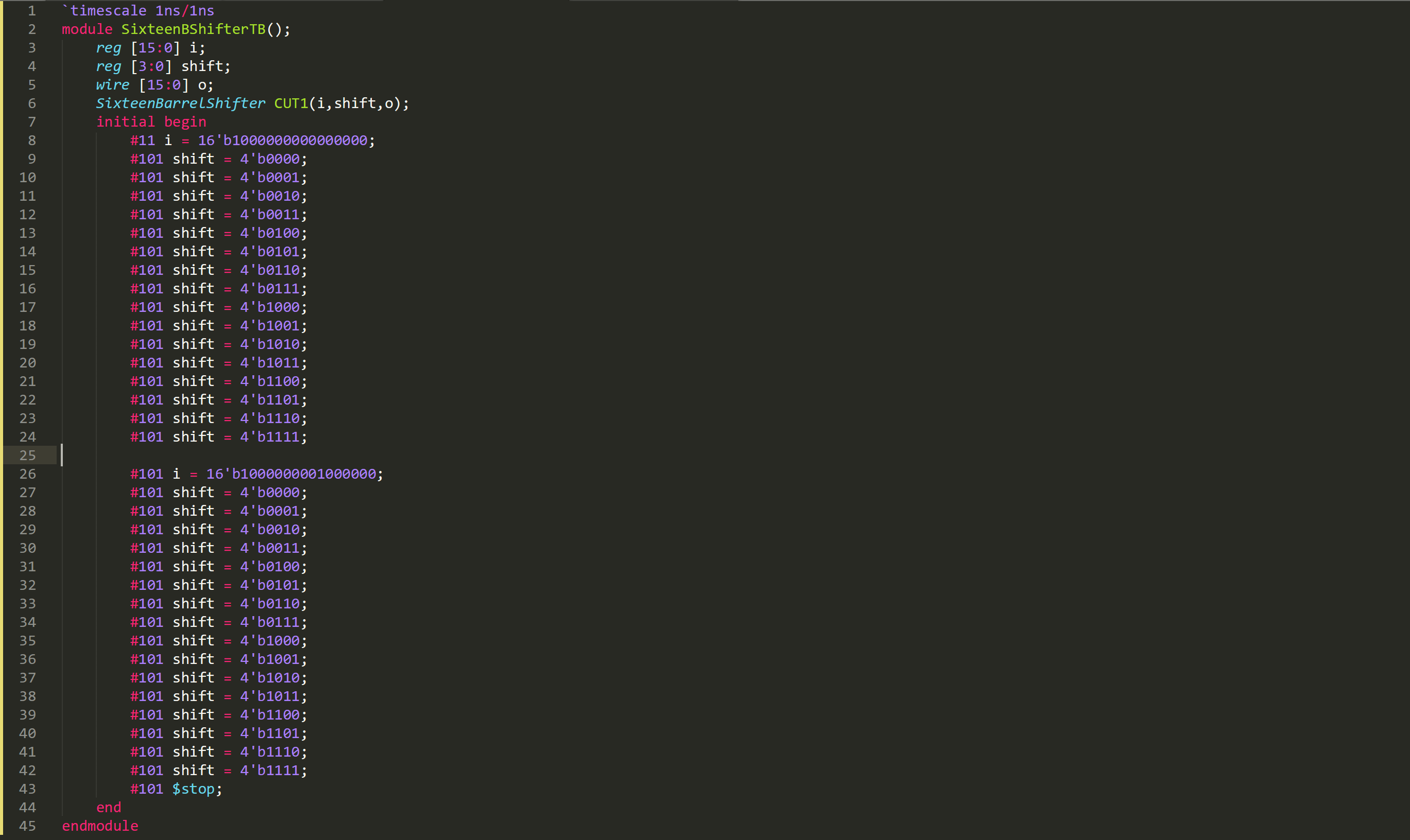
We need sixteen pieces of 16 to 1 MUX in parallel in order to generate 16-bit barrel shifter. We can design the circuit according to this table:

|  |  |
| --- | --- |
| s3,s2,s1,s0 | input |
| 0000 | A15,A14,A13,A12,A11,A10,A9,A8,A7, A6, A5,A4,A3,A2,A1,A0 |
| 0001 | A0,A15,A14,A13,A12,A11,A10,A9,A8,A7, A6, A5,A4,A3,A2,A1 |
| 0010 | A1,A0,A15,A14,A13, A12,A11, A10, A9, A8,A7,A6,A5,A4,A3,A2 |
| 0011 | A2,A1,A0,A15 ,A14,A13, A12,A11, A10, A9, A8,A7,A6,A5,A4,A3 |
| 0100 | A3,A2,A1,A0,A15,A14,A13, A12,A11, A10, A9, A8,A7,A6,A5,A4 |
| 0101 | A4,A3,A2,A1,A0,A15 ,A14,A13, A12,A11, A10, A9, A8,A7,A6,A5 |
| 0110 | A5,A4,A3,A2,A1,A0,A15,A14,A13, A12,A11, A10, A9, A8,A7,A6 |
| 0111 | A6,A5,A4,A3,A2,A1,A0,A15, A14,A13, A12,A11, A10, A9, A8,A7 |
| 1000 | A7,A6,A5,A4,A3,A2,A1,A0,A15 , A14,A13, A12,A11, A10, A9, A8 |
| 1001 | A8,A7,A6,A5,A4,A3,A2,A1,A0,A15 , A14,A13, A12,A11, A10, A9 |
| 1010 | A9,A8,A7,A6,A5,A4,A3,A2,A1,A0,A15 ,A14,A13, A12,A11, A10 |
| 1011 | A10,A9,A8,A7,A6,A5,A4,A3,A2,A1, A0,A15 ,A14,A13, A12,A11 |
| 1100 | A11,A10,A9,A8,A7,A6,A5,A4,A3,A2,A1,A0,A15 ,A14,A13, A12 |
| 1101 | A12,A11,A10,A9,A8,A7,A6,A5,A4,A3,A2,A1,A0,A15, A13 |
| 1110 | A13,A12,A11,A10,A9,A8,A7,A6,A5,A4,A3,A2,A1,A0, A15 , A14 |
| 1111 | A14,A13,A12,A11,A10,A9,A8,A7,A6,A5,A4,A3,A2,A1,A0, A15 |

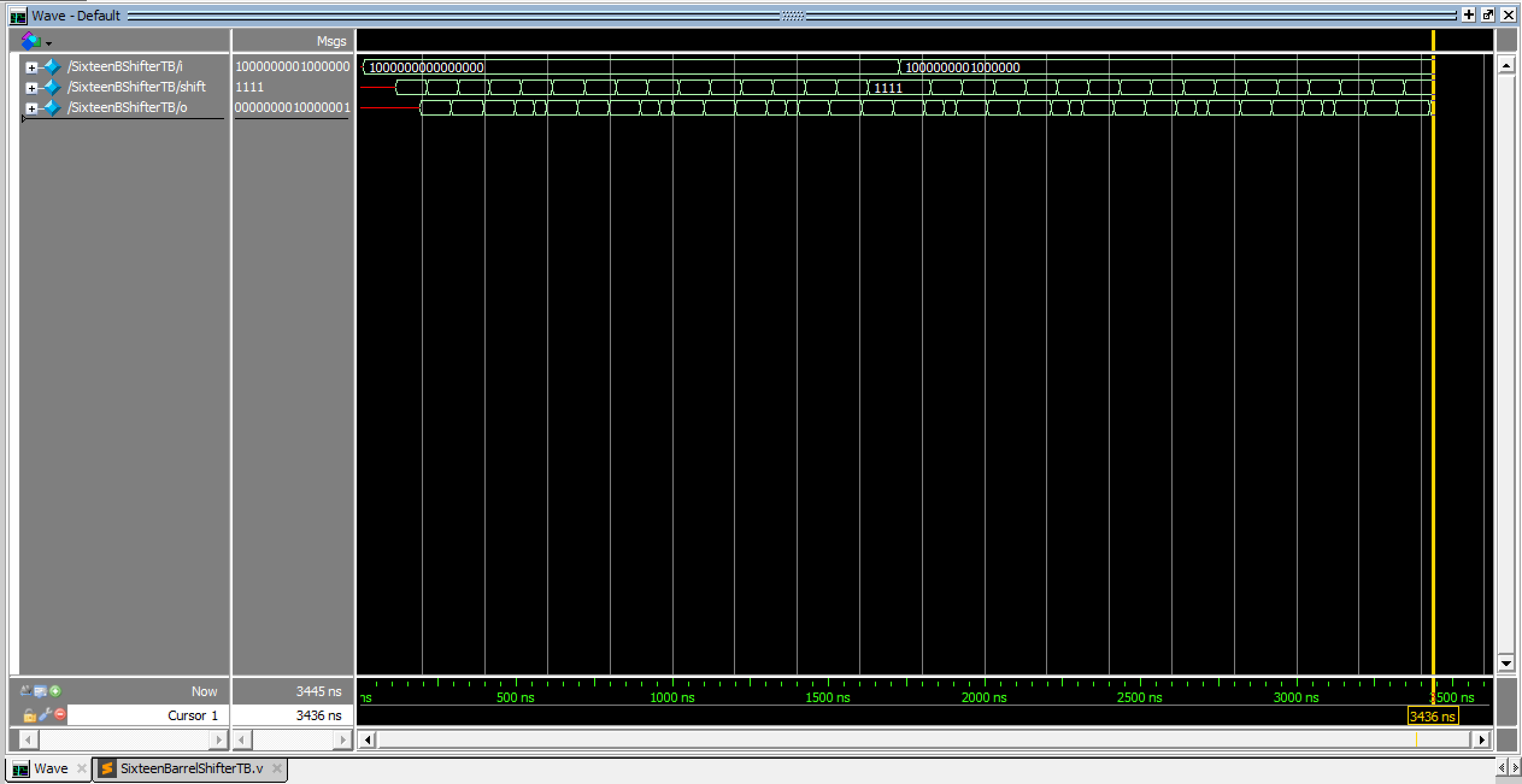
**Verilog Code**

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**Testbench**



**Simulation Result**

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**Worst-case Delay**

The design of 16-bit Barrel Shifter is very similar to 4-bit Barrel Shifter.

Every path from goes through one 16 to 1Mux. And from problem 3, we know that the delay of 16 to 1 Mux is **80ns**.

We can see from waveform, the worst-case delay is also **80ns**