

UNIVERSITY OF TEHRAN

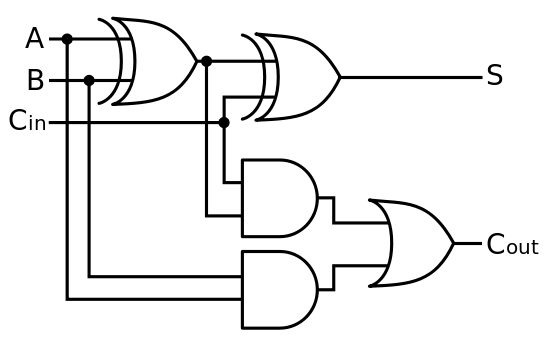
Report for Computer Assignment 3

**RT Level Components, Iterative Logic, Synthesis**

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Problem 1

**Circuit Diagram**

**Calculating Delay Values**

**AND Gate Delay**

In computer Assignment 1, we calculated the worst-case delay of NAND gate.( To 1 = 10ns ,To 0 = 8ns, Avg = 9ns)

Delay values for NOT gate are #(5,6). (Avg = 5ns)

If we invert a NAND gate, we get AND get. So the AND gate delay is 5 + 9 = 14ns.

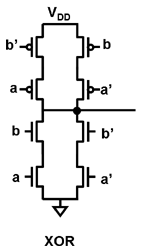
**OR Gate Delay**

Delay values for NOR gate is #(10,14). (Avg = 12ns)

If we invert a NOR gate, we get OR get. So the OR gate delay is 12+5 = 17ns

**XOR Gate Delay**

The XOR gate delay is 9 + 9 + 5 = 23ns



**Worst-case delay of FA**

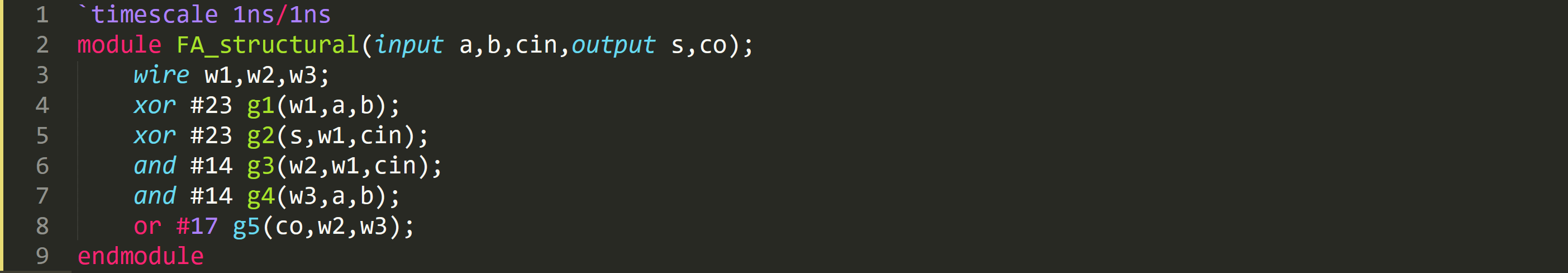
The sum output comes from two consecutive XOR gates. So worst-case delay for S is 23 + 23 = 46

The longest path from input to carry-out(co) includes AND, OR gate. So worst-case delay for CO is 14 + 17 = 31

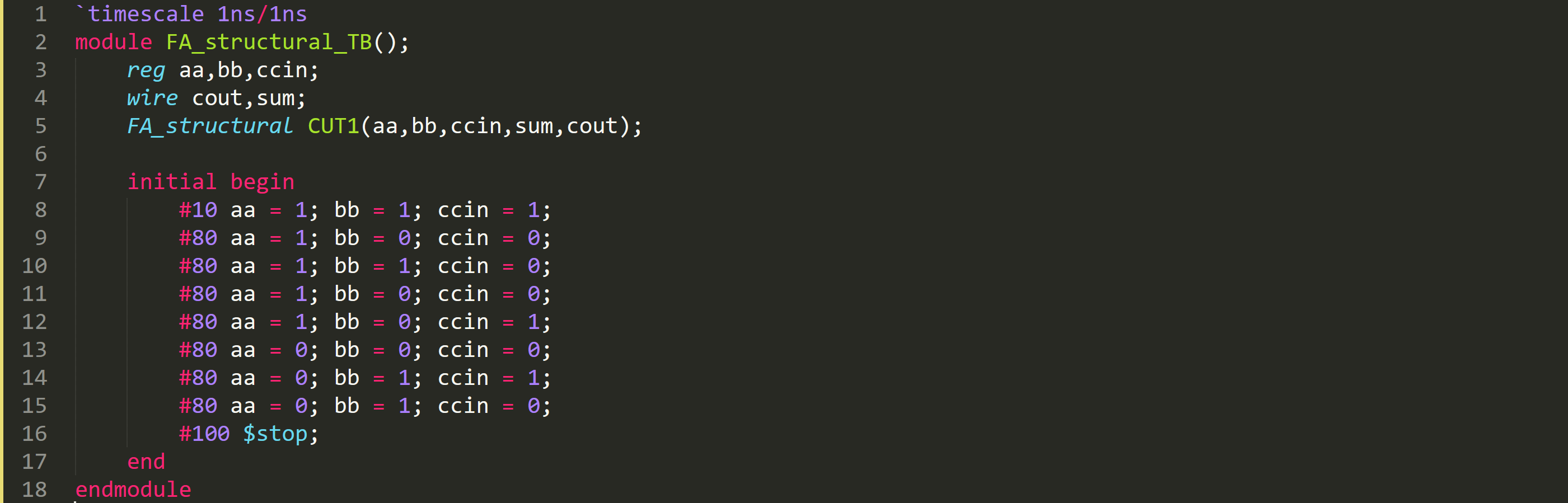
So the worst-case delay for FA is **46ns**.

**Verilog Code**

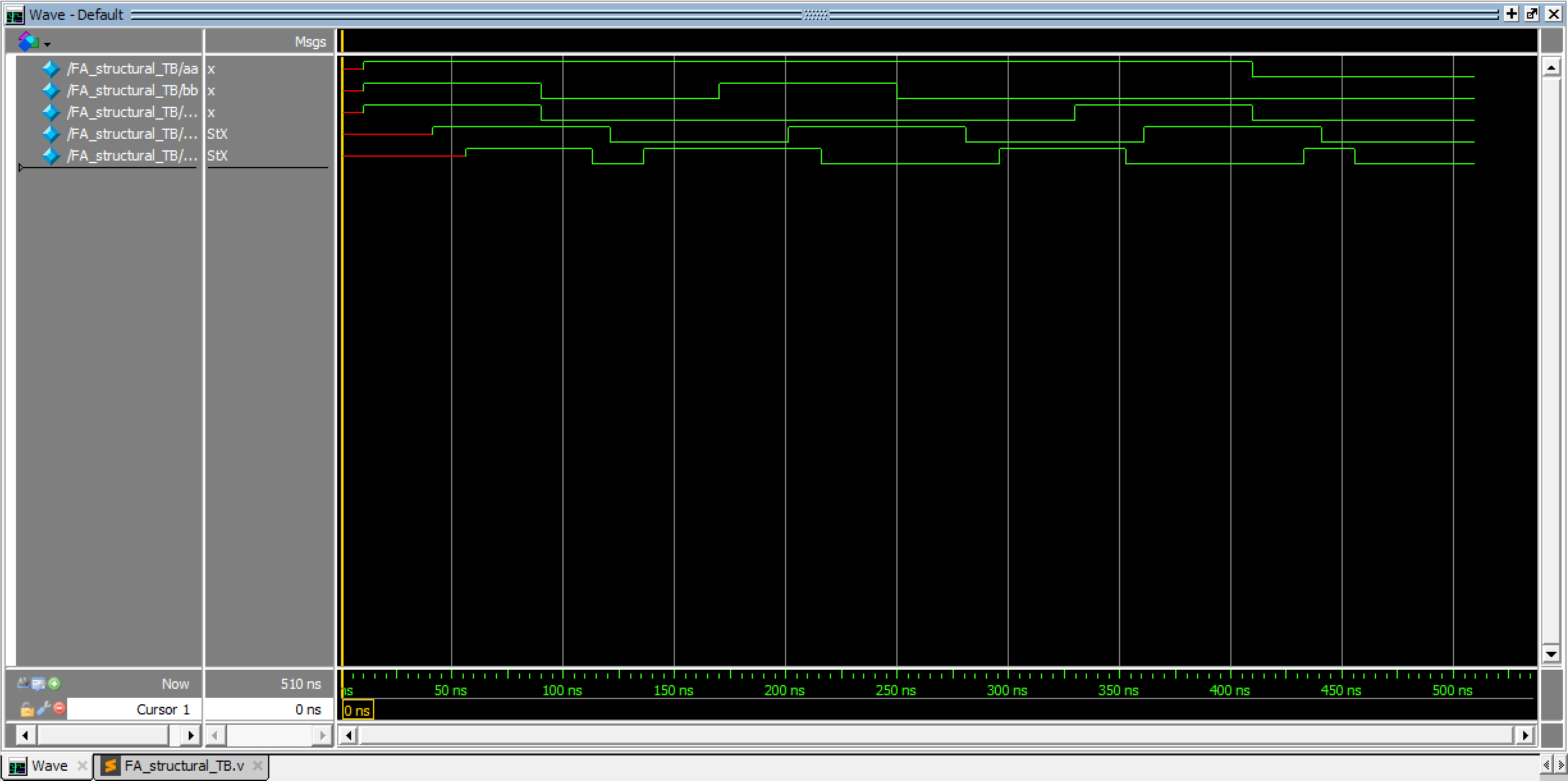
Structural implementation of FA :

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**Testbench**

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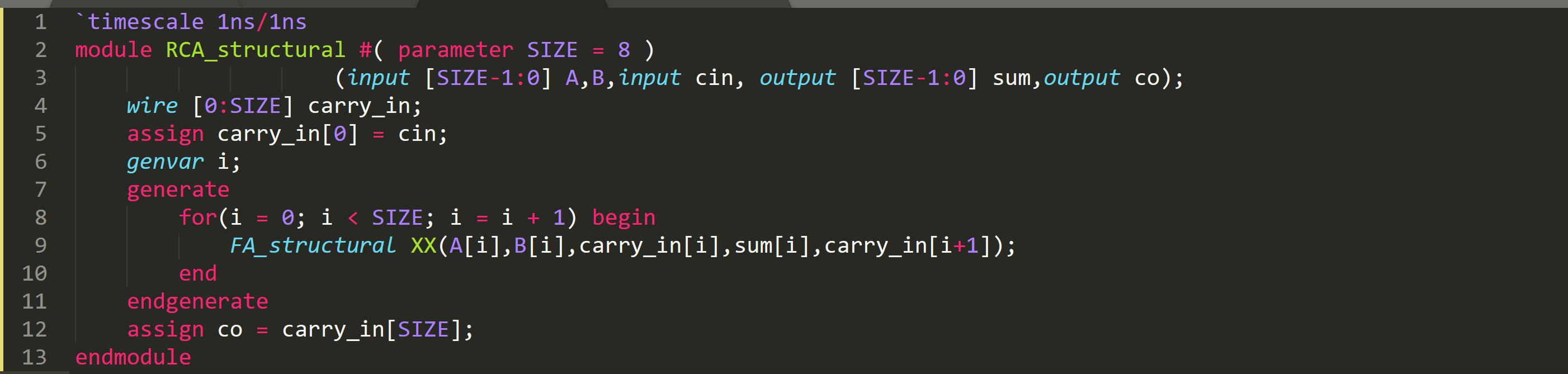
**Simulation Result**

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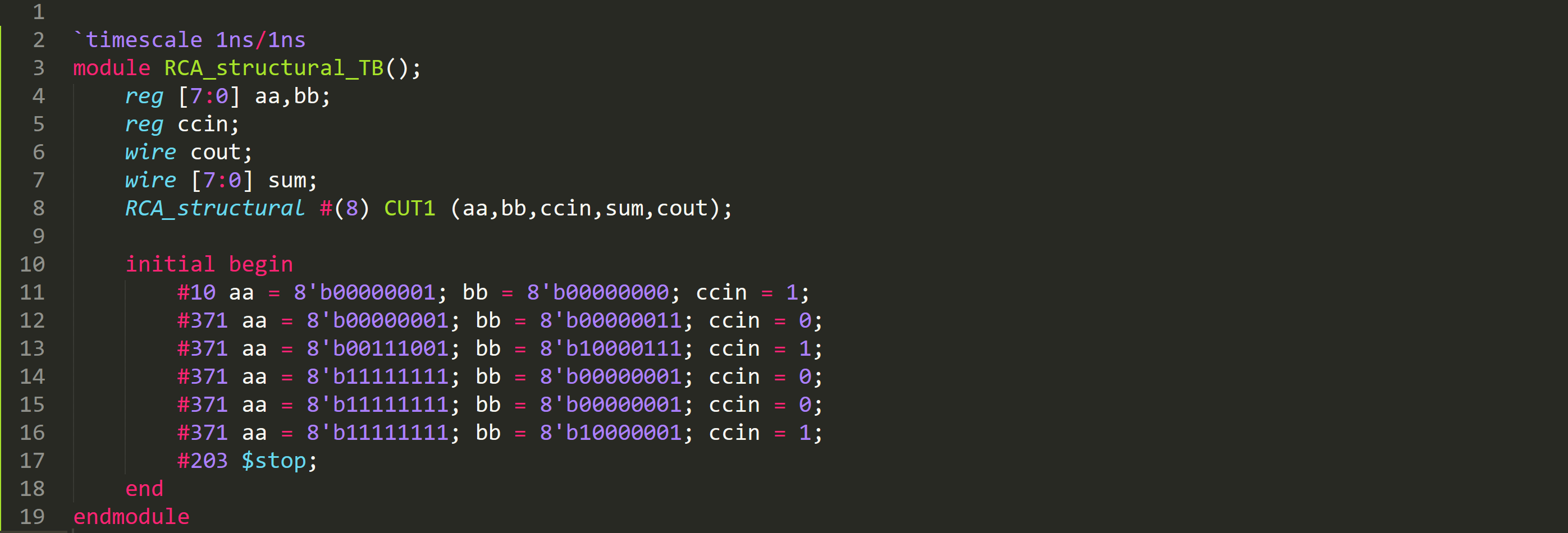
As you can see, the worst-case delay for s and co output are **46ns** and **31ns**.

**N-bit Ripple Carry Adder (Structural)**

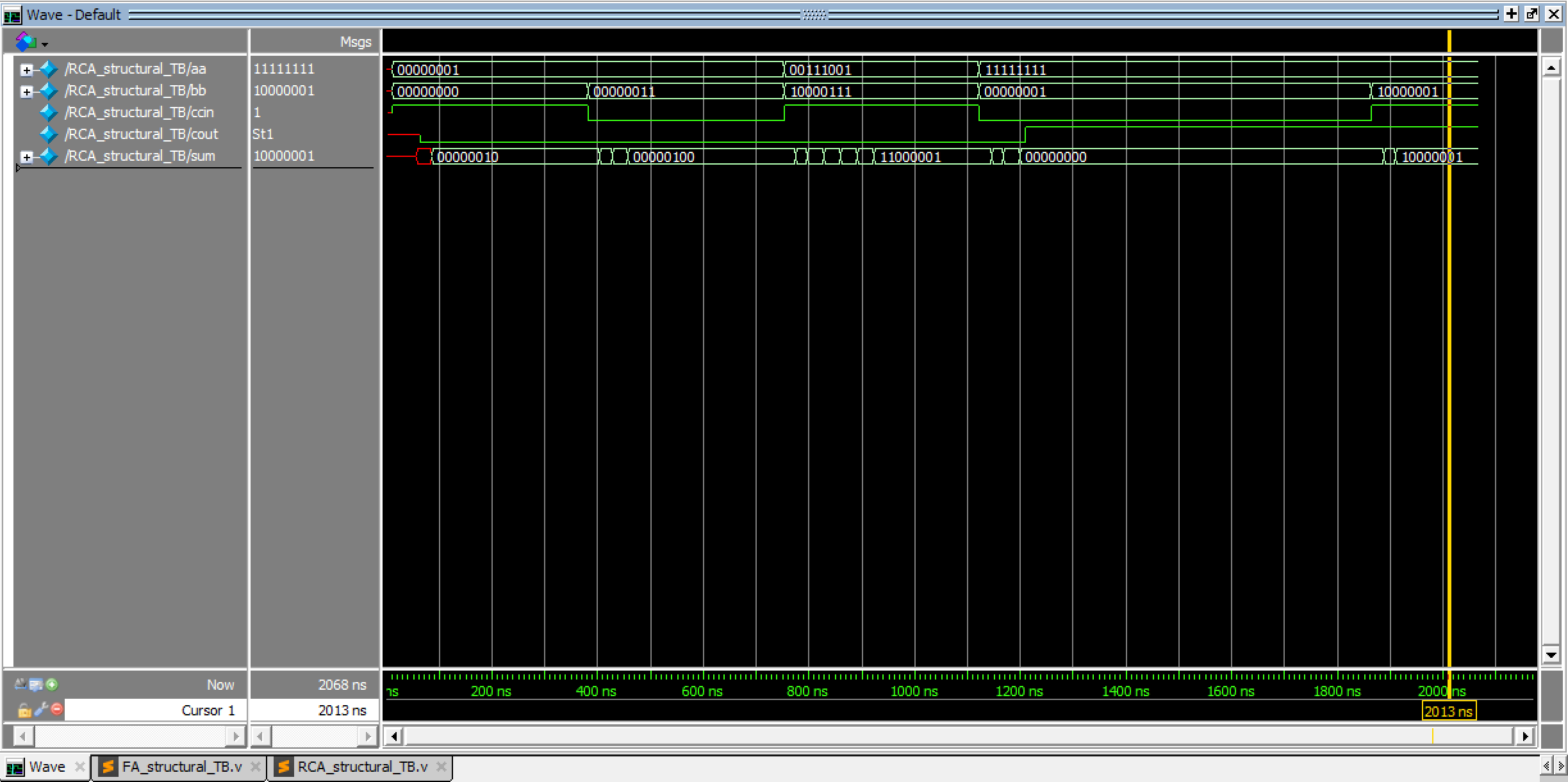
N-bit Ripple Carry Adder has been implemented using generate statement.

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**Testbench**

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**Simulation Result**

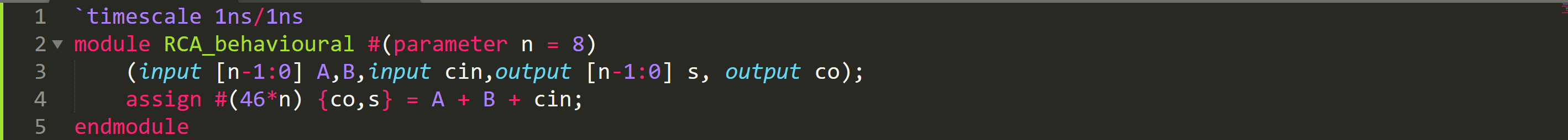
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In a 8-bit RCA, 8 Full-Adder are cascaded together. We know the worst-case delay of FA is 46ns.

So at most, it should take **46\*8 = 368ns** in the worst-case.

Problem 2

**Verilog Code**

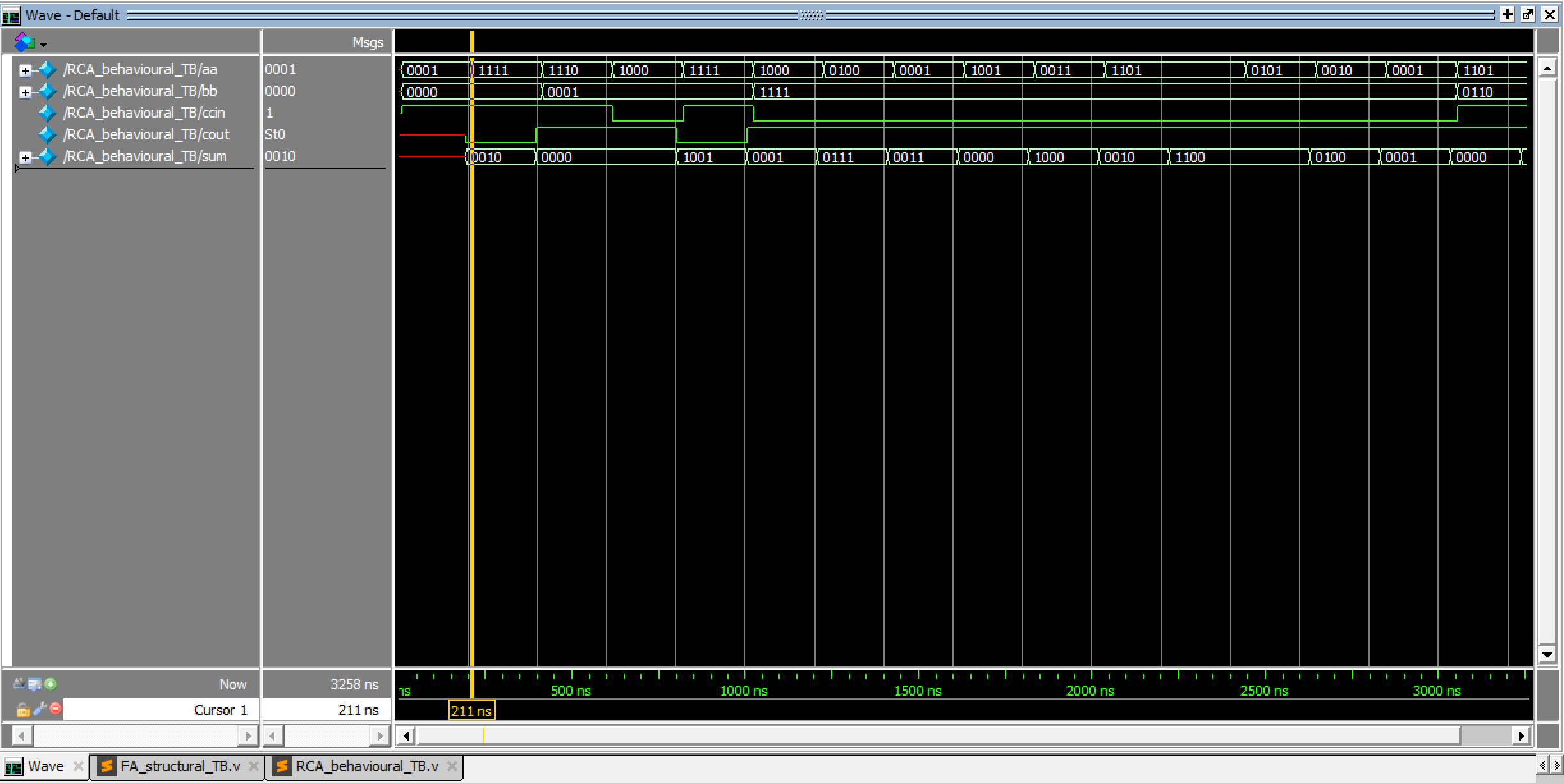
In problem 1, we calculated worst-case delay of FA which is 46ns. So n-bit Ripple Carry Adder has **46\*n** delay at most. 

Problem 3

**Testbench**

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**Simulation Result**

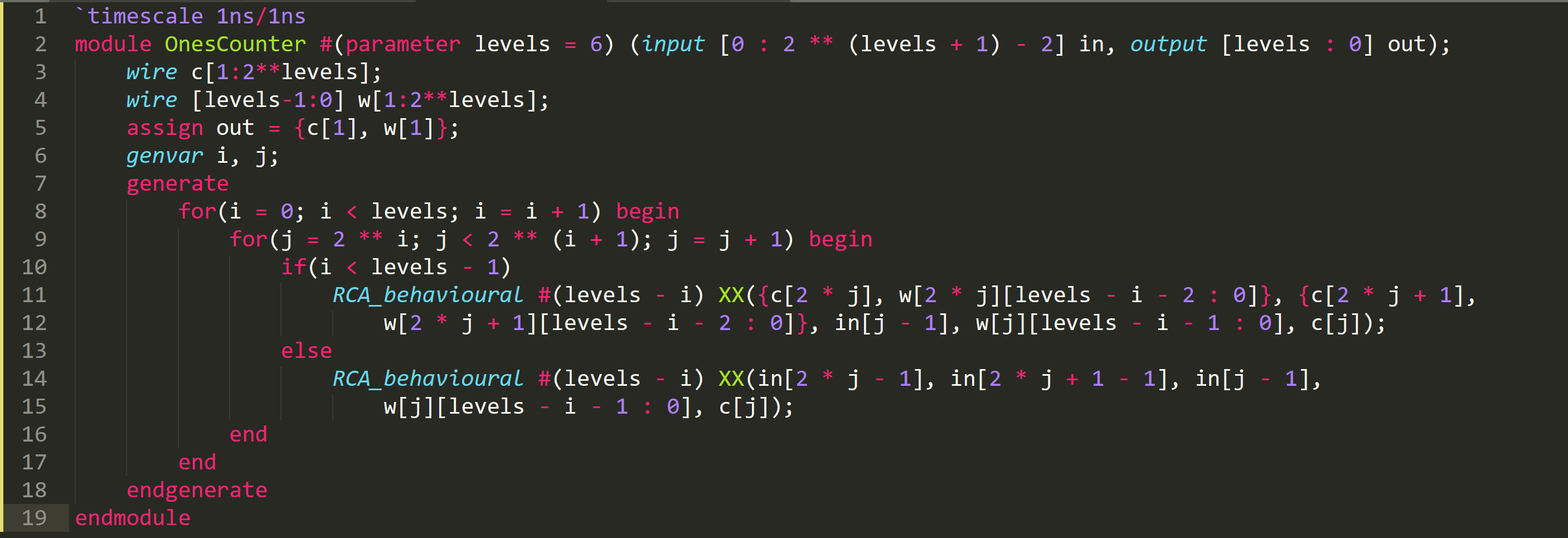
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Problem 4

**Circuit Diagram**

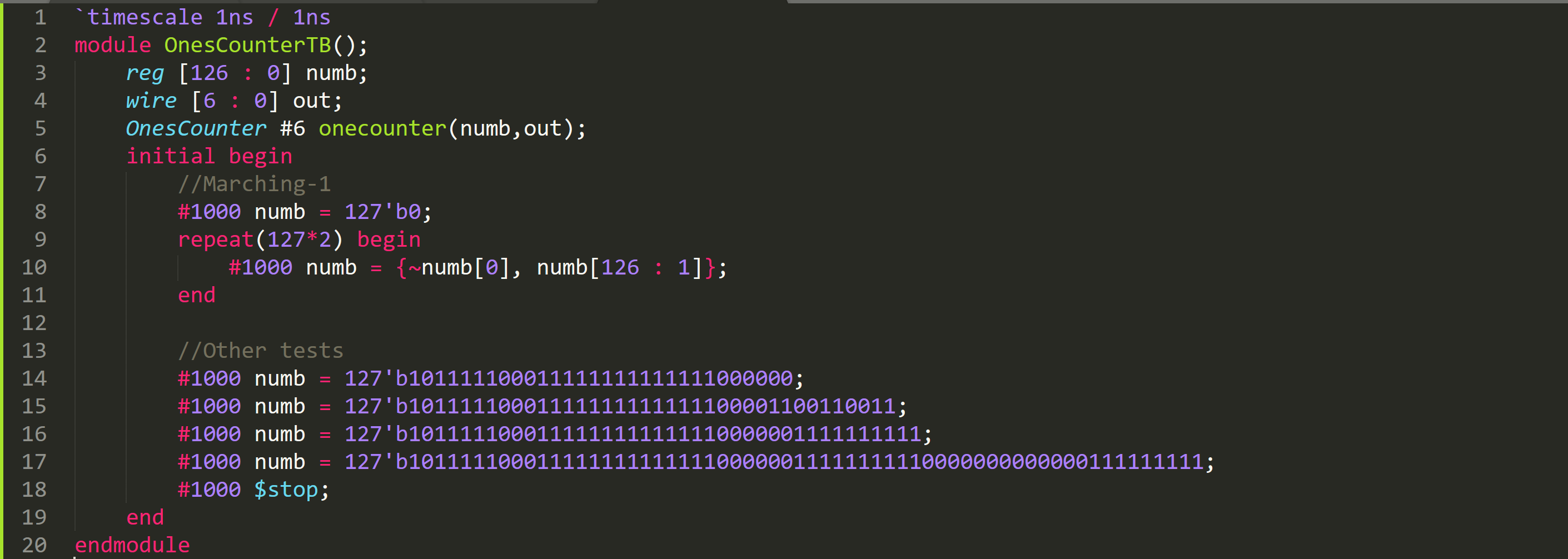
**????????**

**Verilog Code**

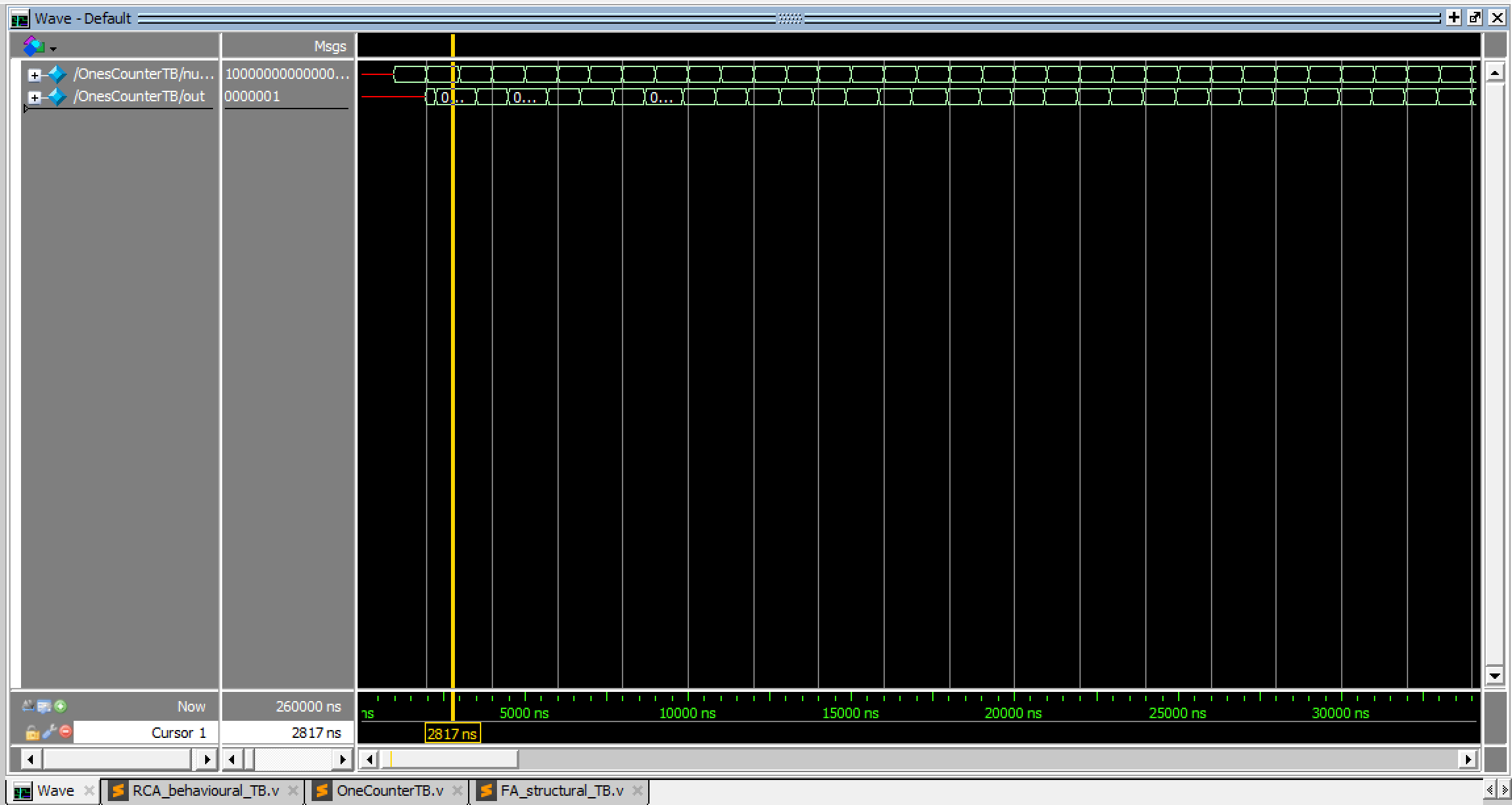
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Problem 5

**Testbench**

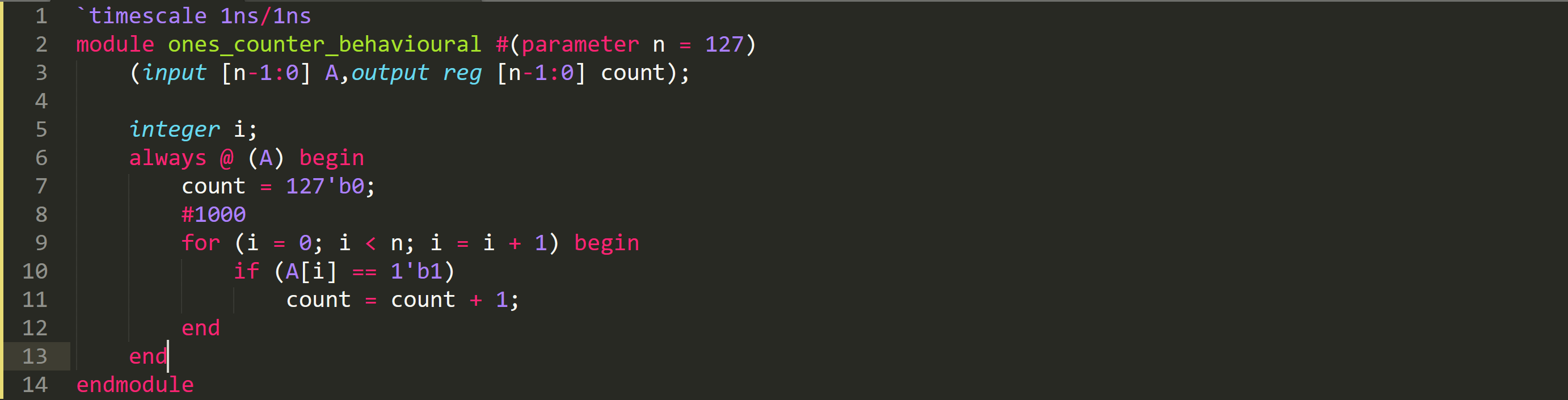


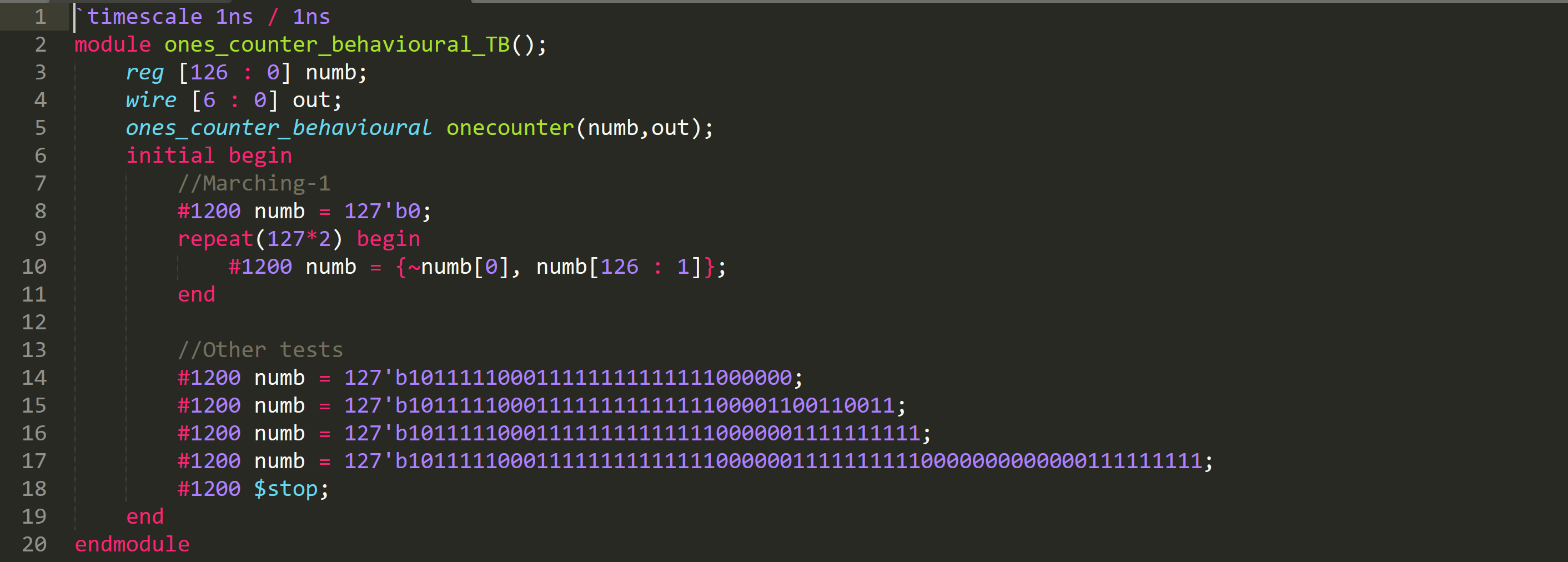
**Simulation Result**

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Problem 6

**Verilog Code**

**Testbench**

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**Simulation Result**

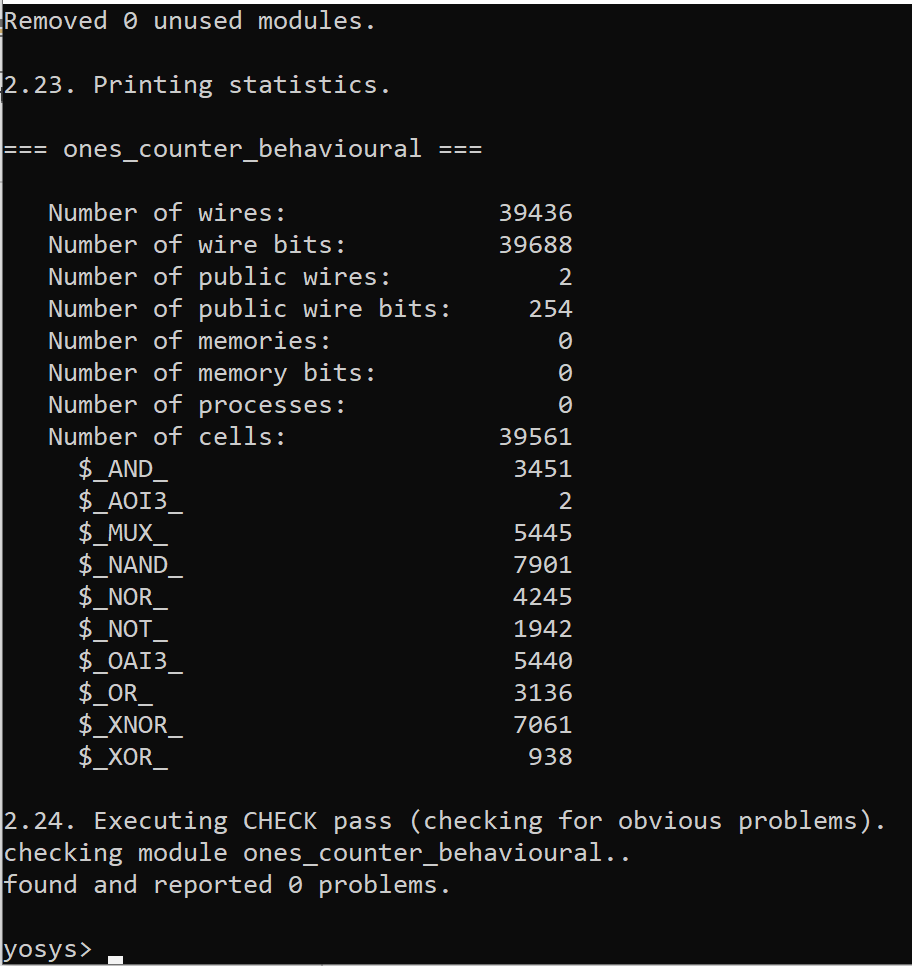
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The output of problem 5 and 6 are the same.

Problem 7

The synthesized file can be found in **OnesCounter2\_Synth.v**

Here you can see the number of wires and cells needed for this synthesis :



**Problem 4 and 7 comparision**

In problem 4, we have one 6-bit RCA, two 5-bit RCA, four 4-bit RCA, eight 3-bit RCA, sixteen 2-bit RCA and thirty-two 1-bit Adder.

Full-Adder circuit contains 5 gates and a n-bit RCA contains n FA pieces. So n-bit RCA contains **5n** logic gates.

**Number of gates** used in problem4 :

5\*6 + 2\*5\*5 + 4\*5\*4 + 8 \* 5 \* 3 + 16 \* 5 \* 2 + 32 \* 5 \* 1 = 600

**We only used 600 logic gates, whereas problem 7 used 40000 logic gates!**