

UNIVERSITY OF TEHRAN

Report for Computer Assignment 4

Latches, flip-flops, and a little beyond

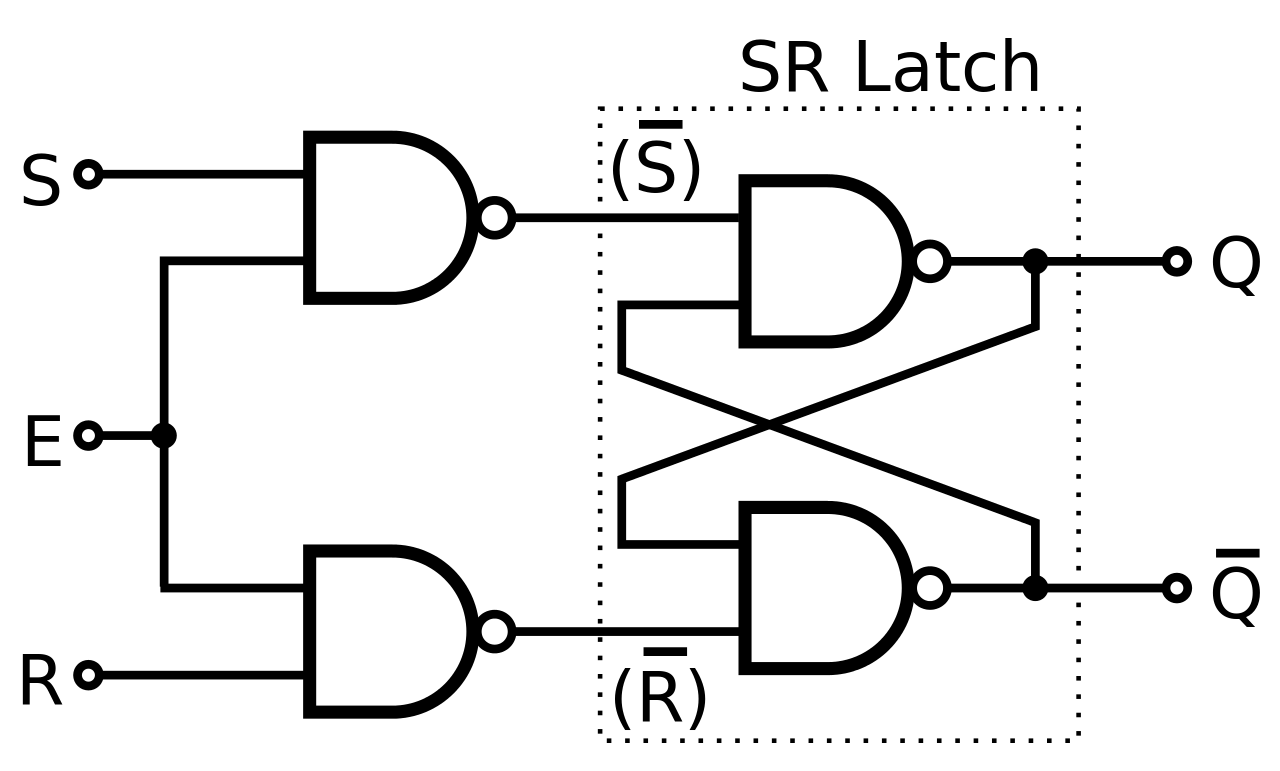
Instructor : Dr. Navabi

Danial Saeedi

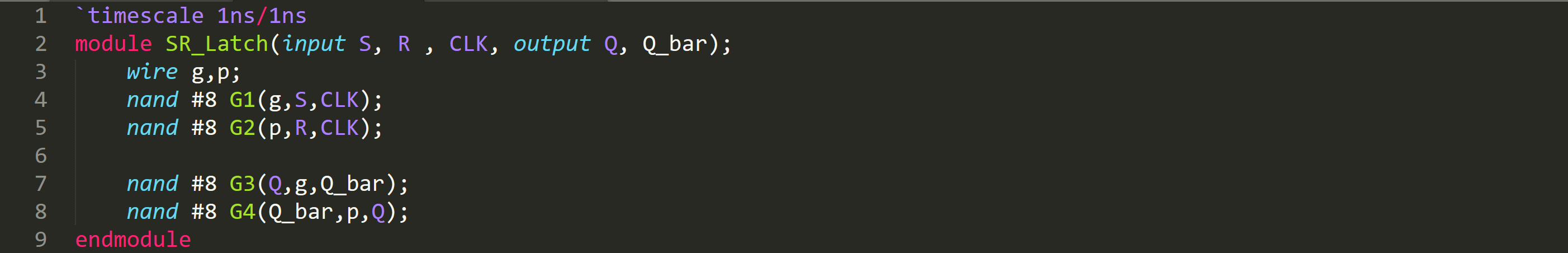
Problem 1

Circuit Diagram

The worst-case delay of NAND according to its delays is 4 + 4 = 8ns.

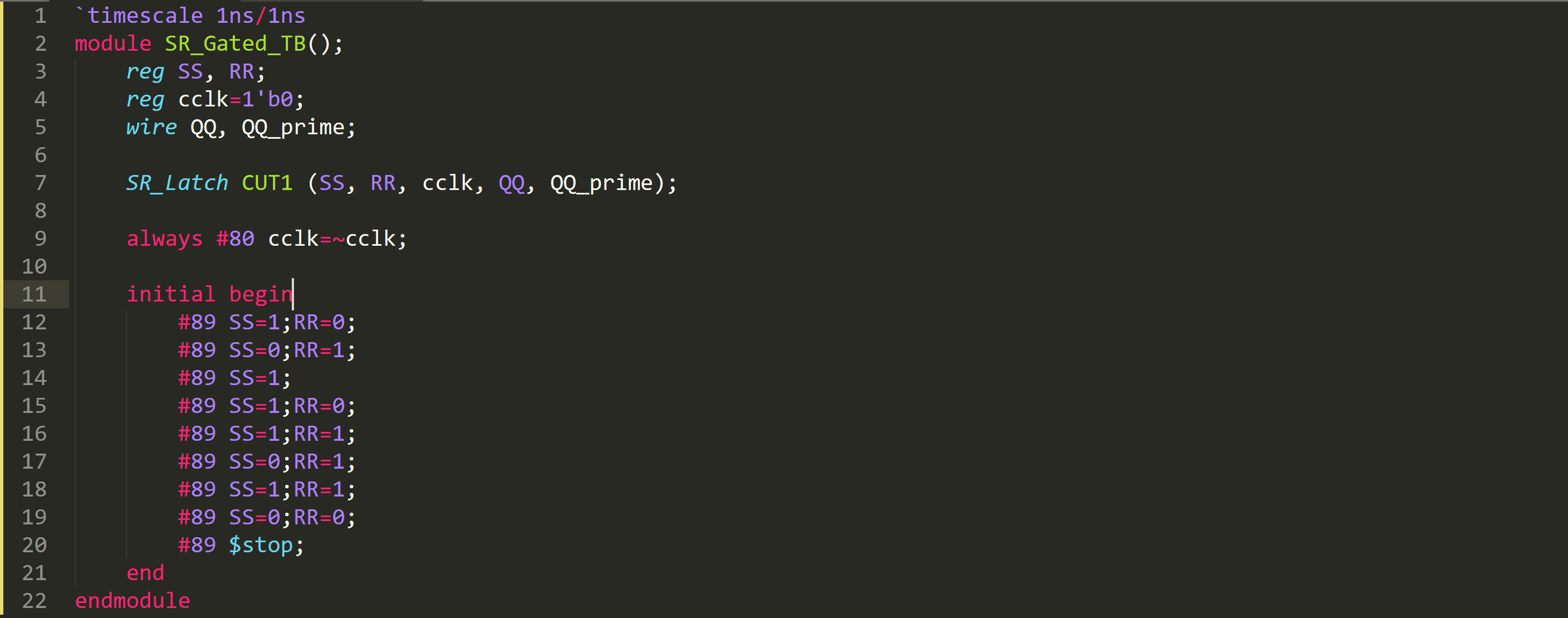


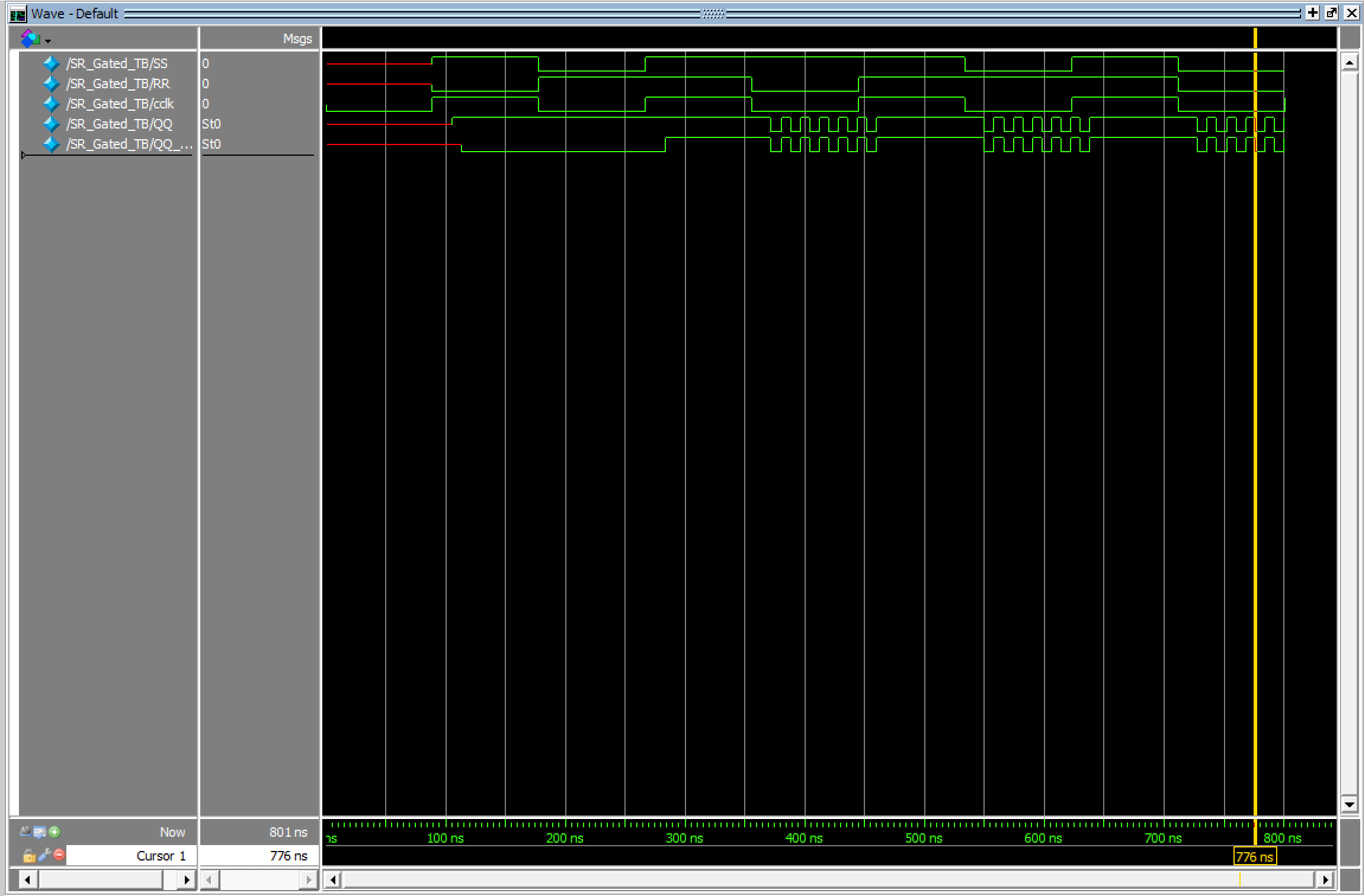
Verilog Code



Problem 2

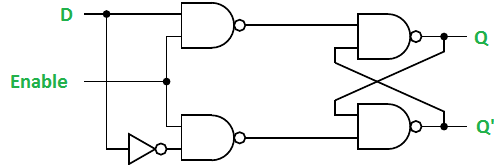
Testbench



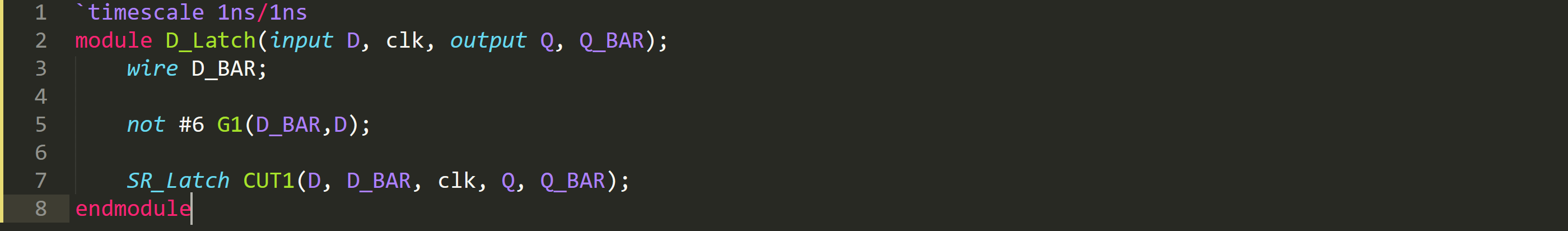


Problem 3

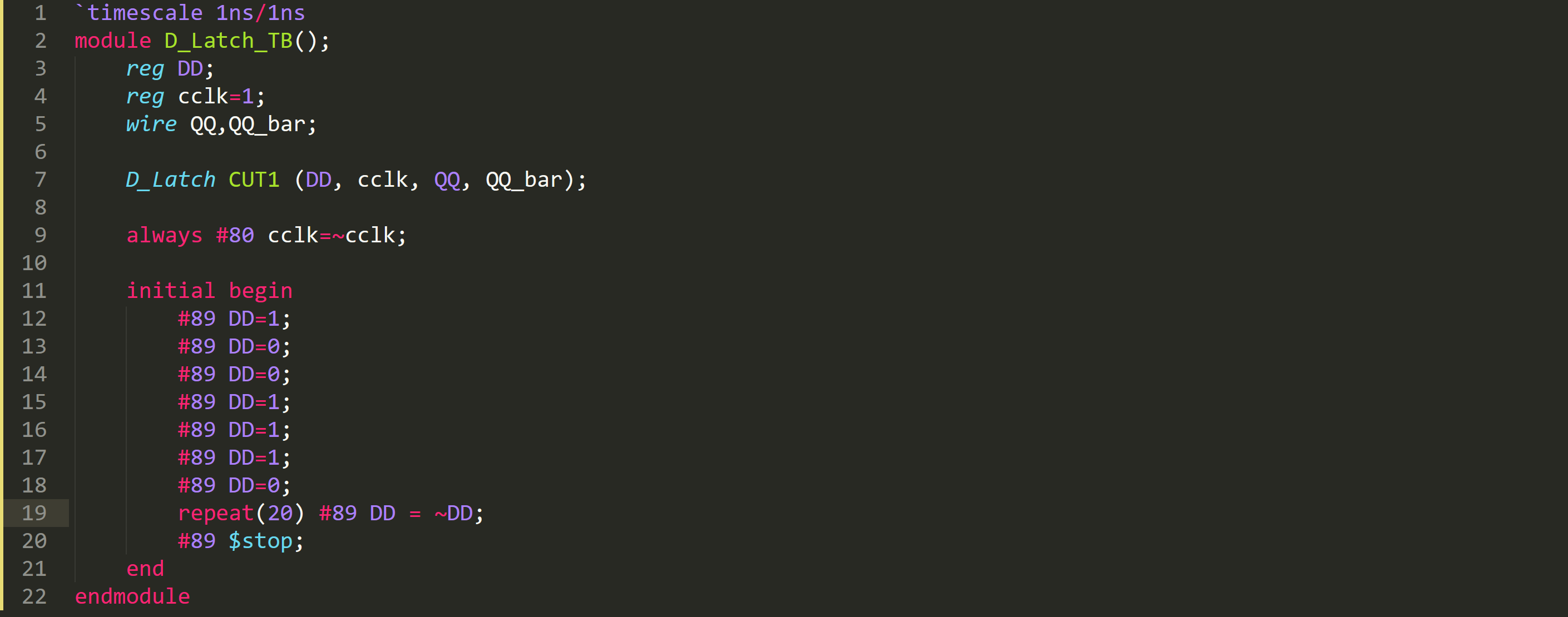
Circuit Diagram



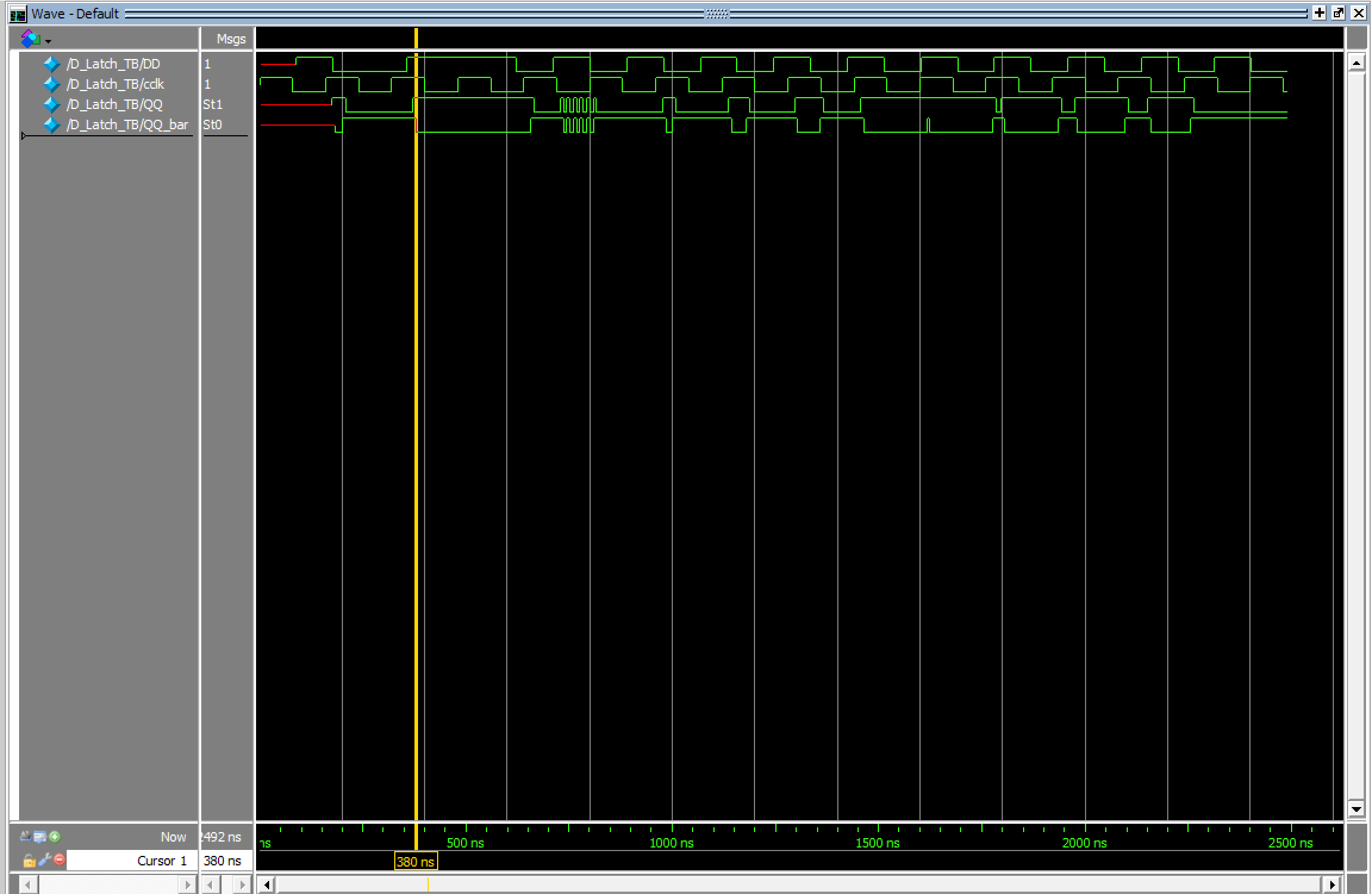
Verilog Code



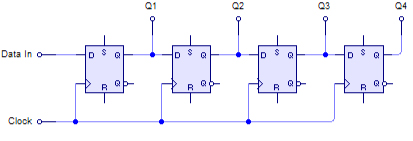
Testbench



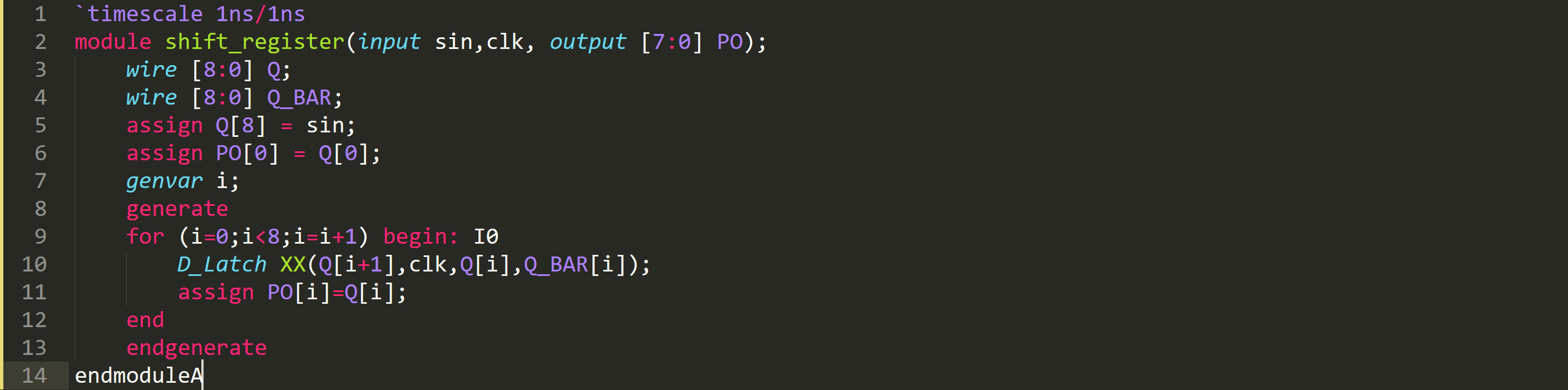
Simulation Result



Problem 4

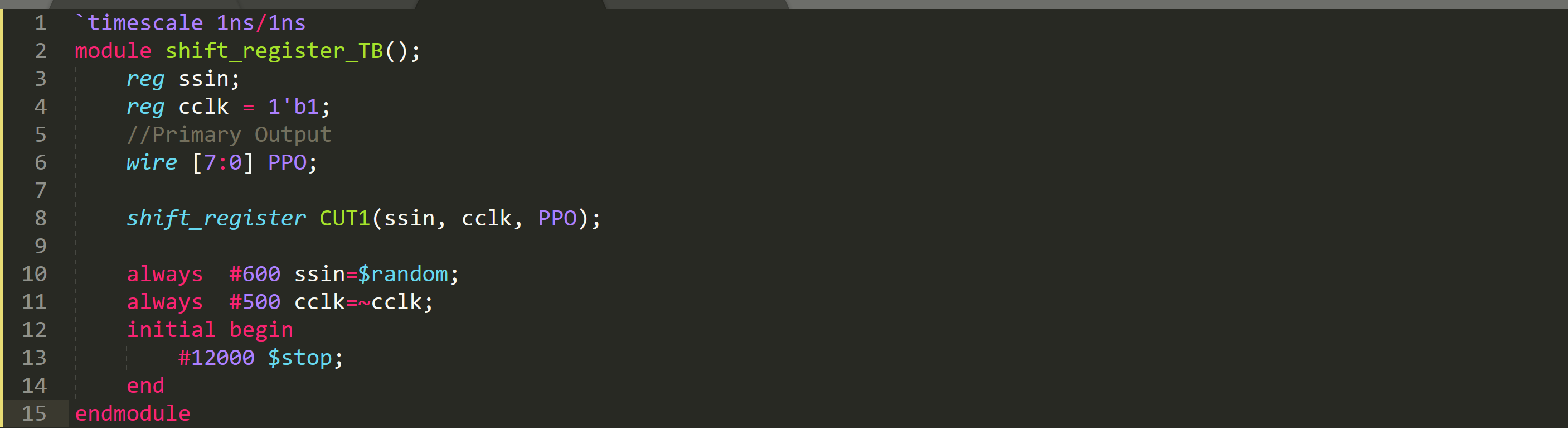
Circuit Diagram

Verilog Code

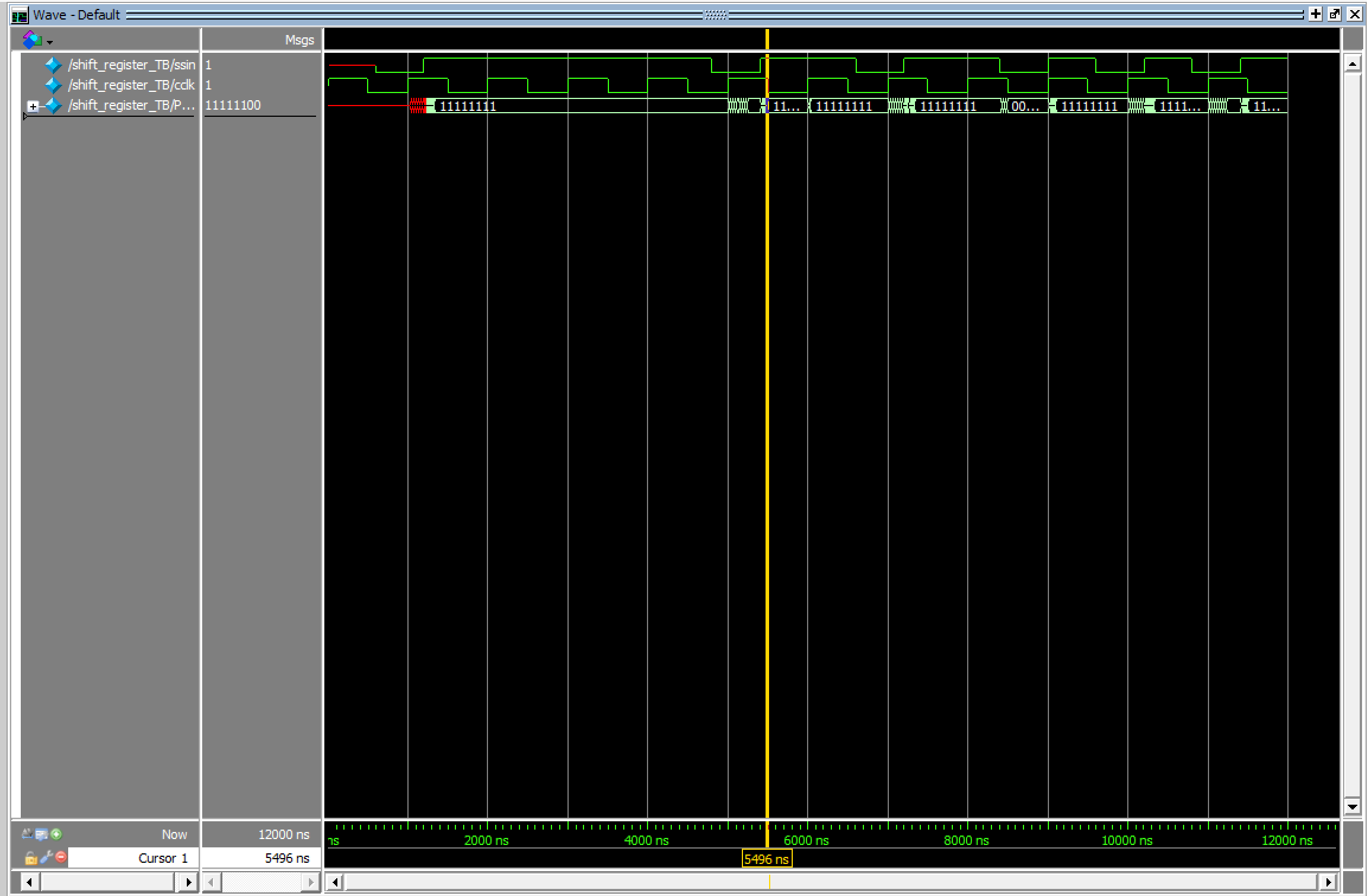


Problem 5

Testbench



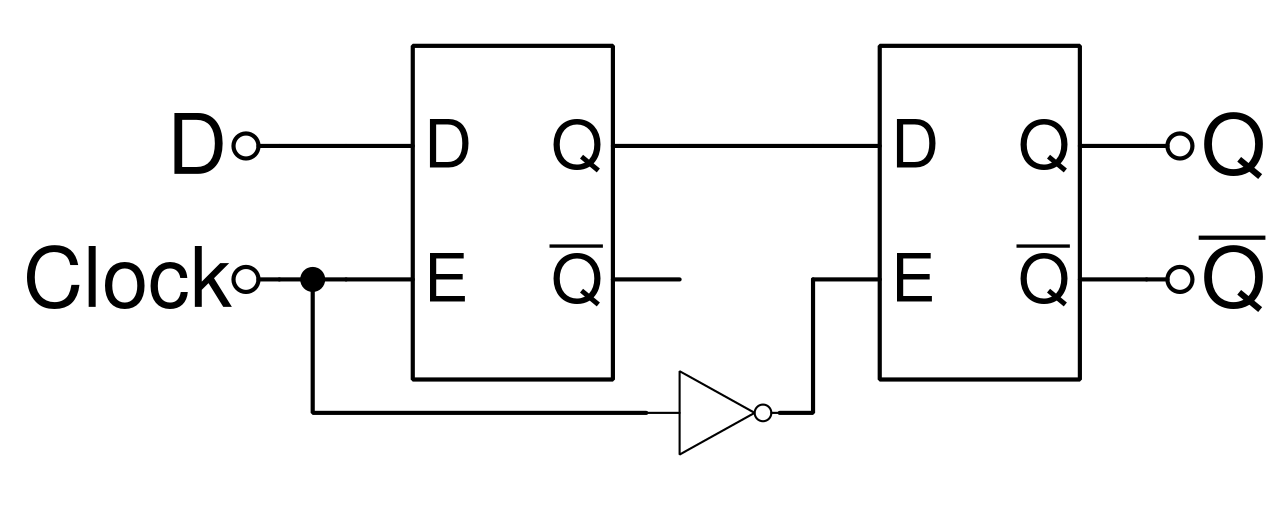
Simulation Result



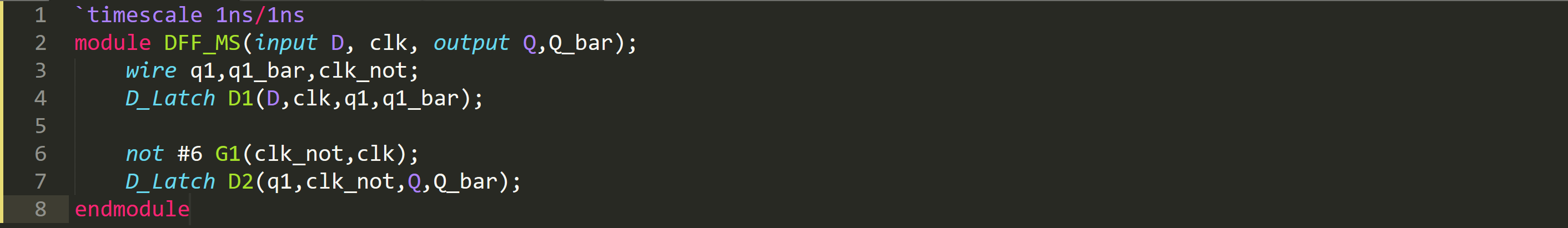
As you can see, this circuit **doesn’t** work because it has **transparency** issue.

Problem 6

Circuit Diagram



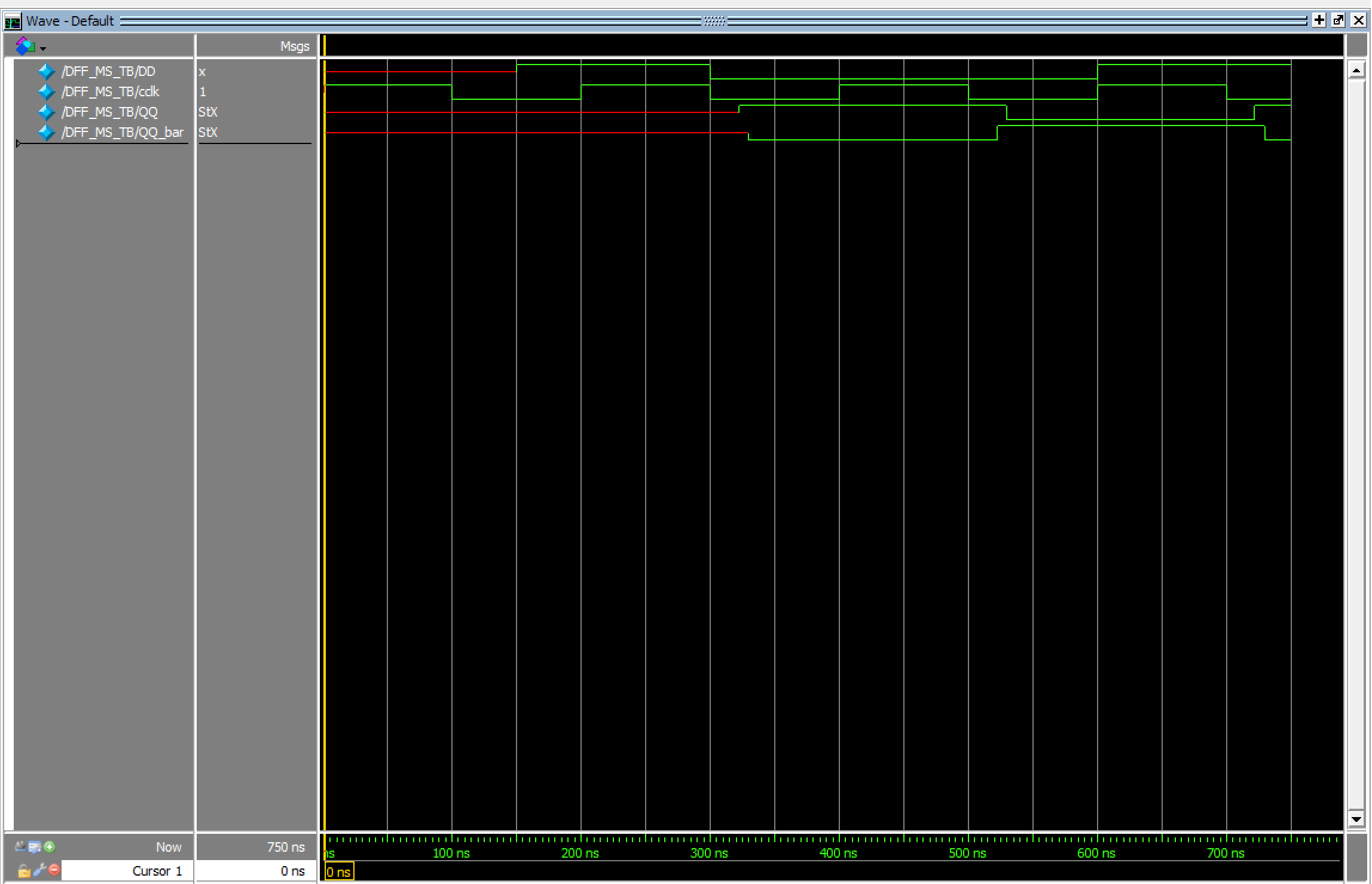
Verilog Code



Testbench

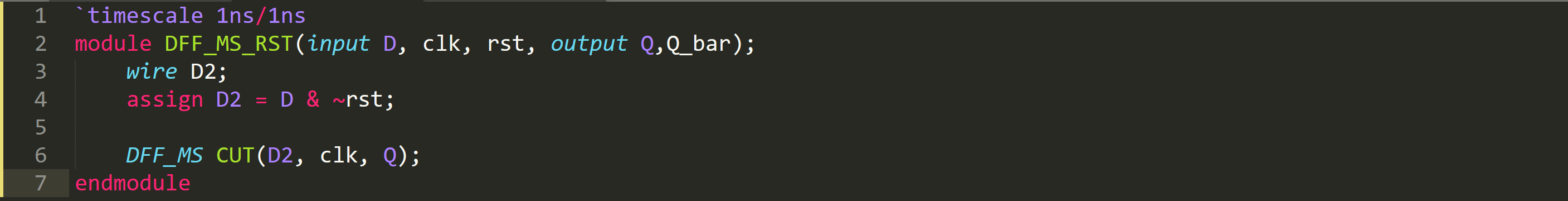


Simulation Result

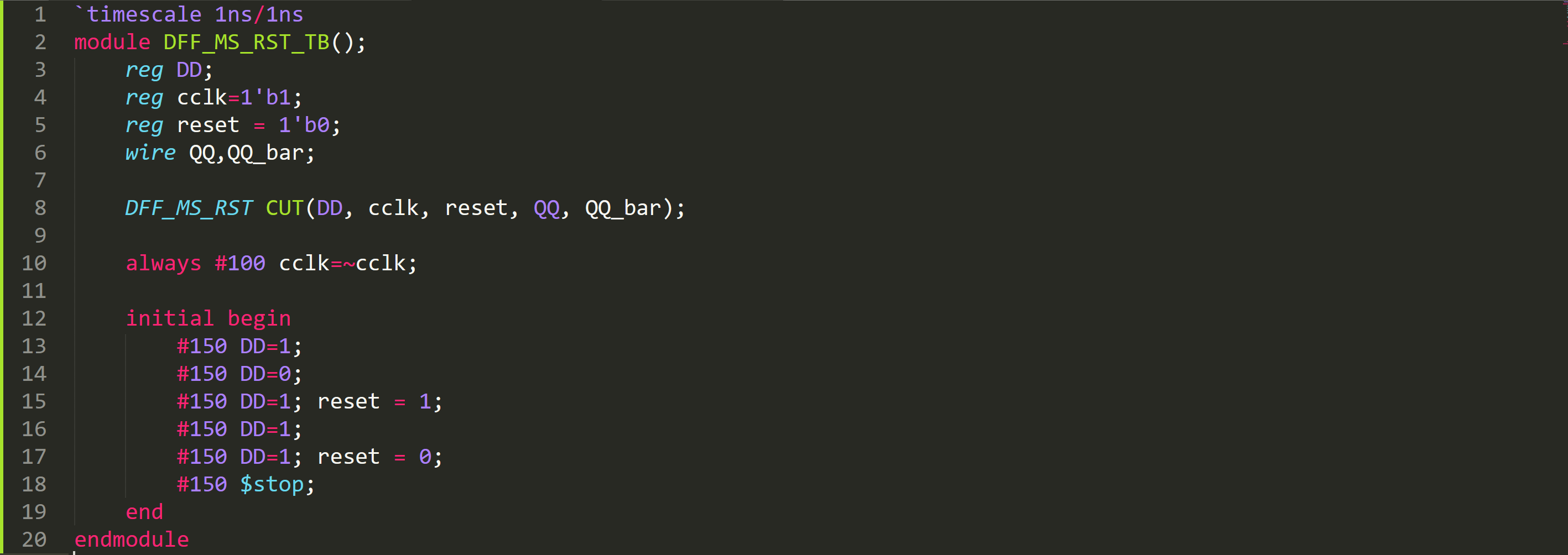


Problem 7

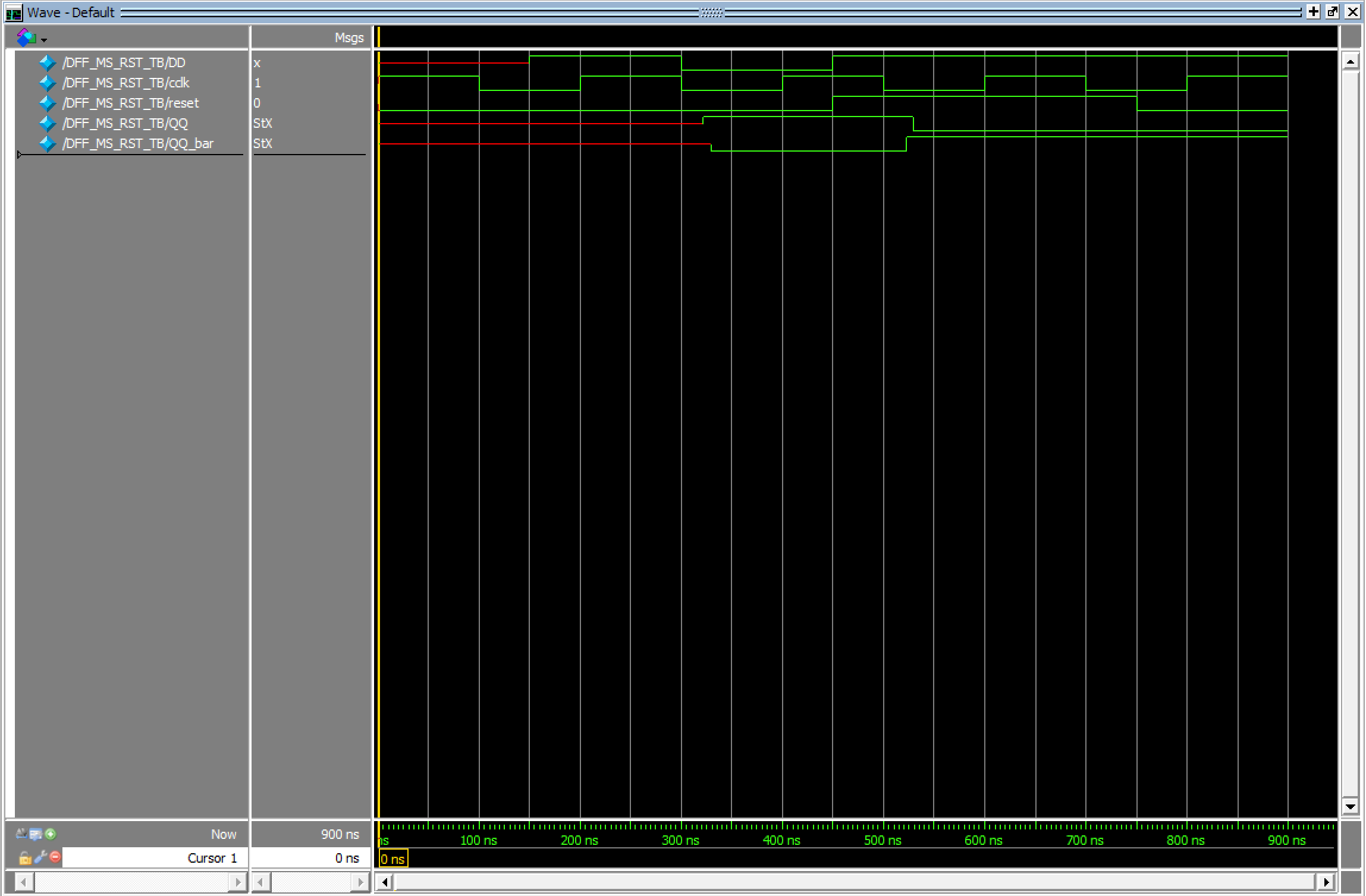
Verilog Code



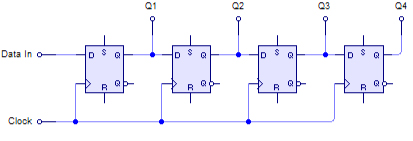
Testbench



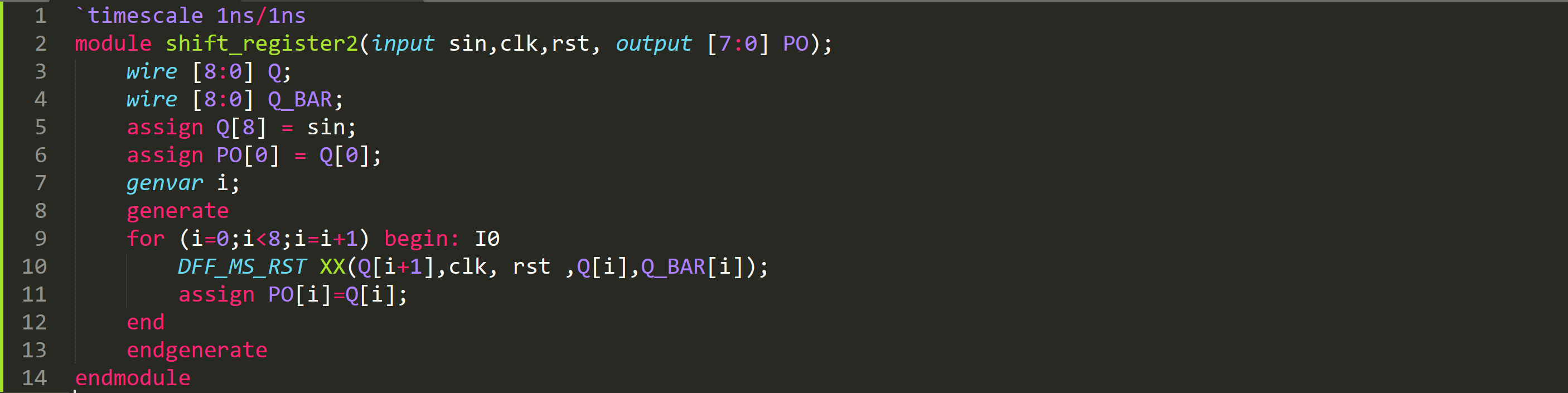
Simulation Result



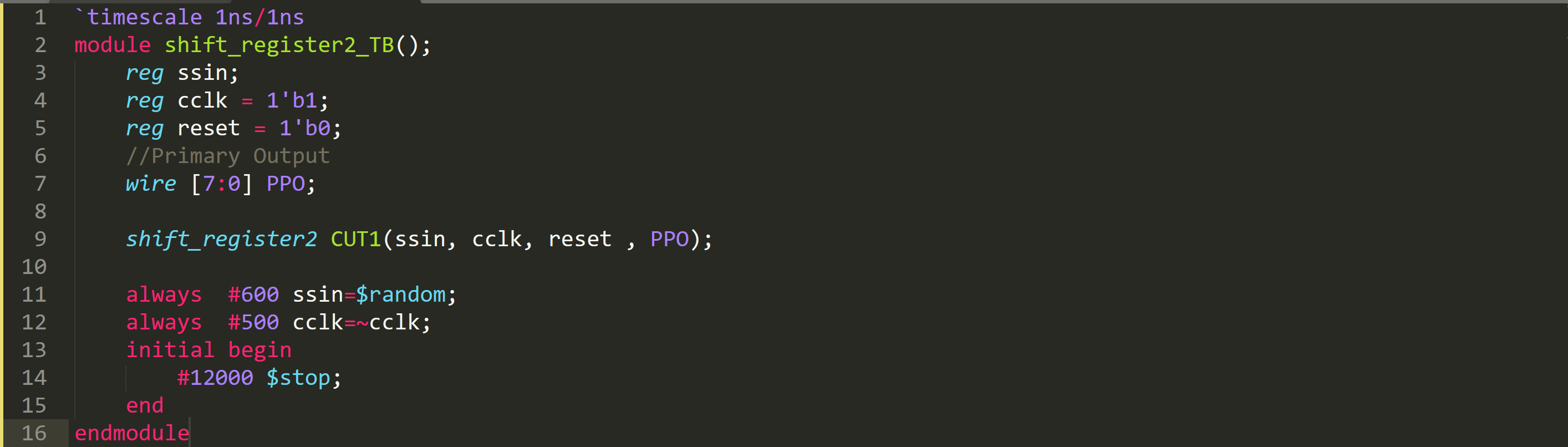
Problem 8

Circuit Diagram

Verilog Code



Testbench



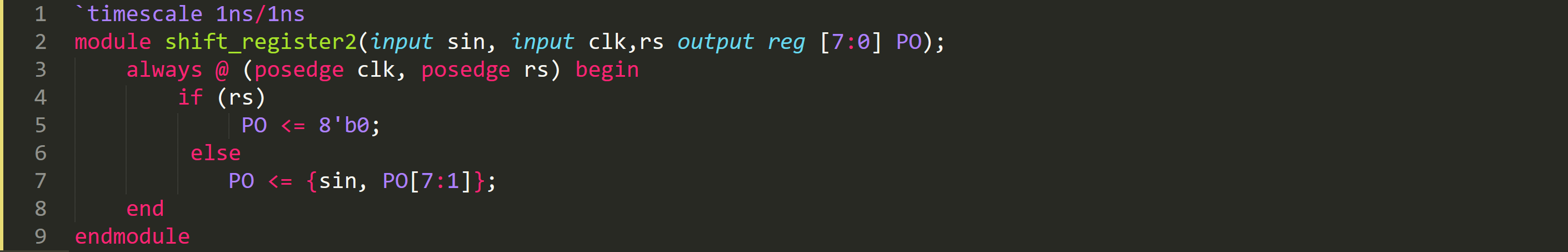
Simulation Result



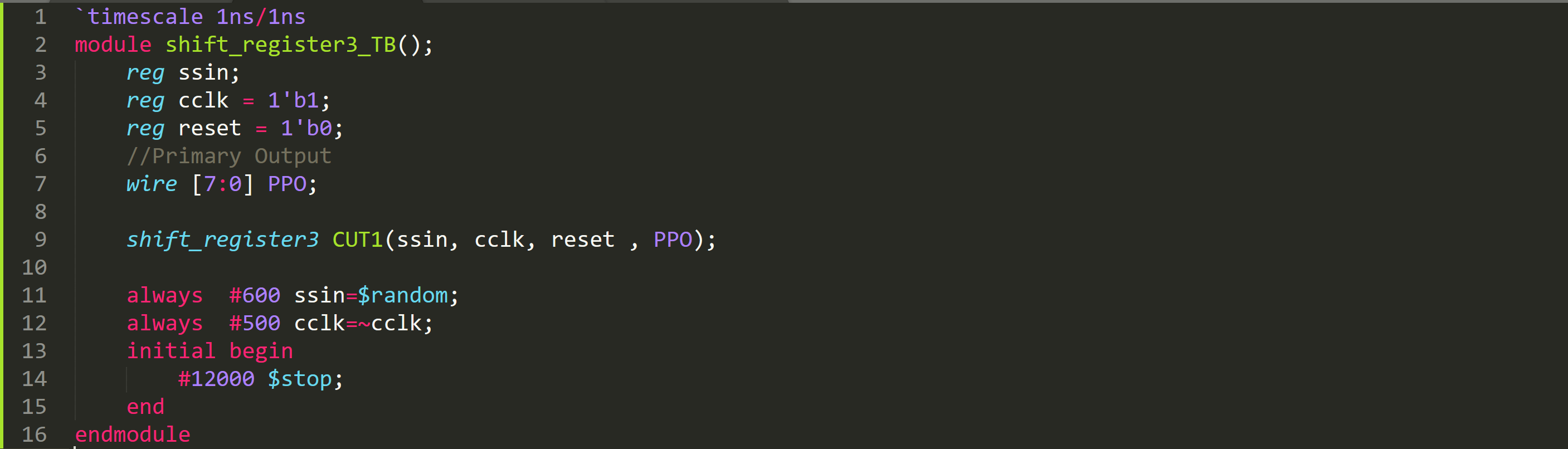
As you can see, this circuit works because it doesn’t has **transparency** issue unlike problem 4.

Problem 9

Verilog Code



Testbench

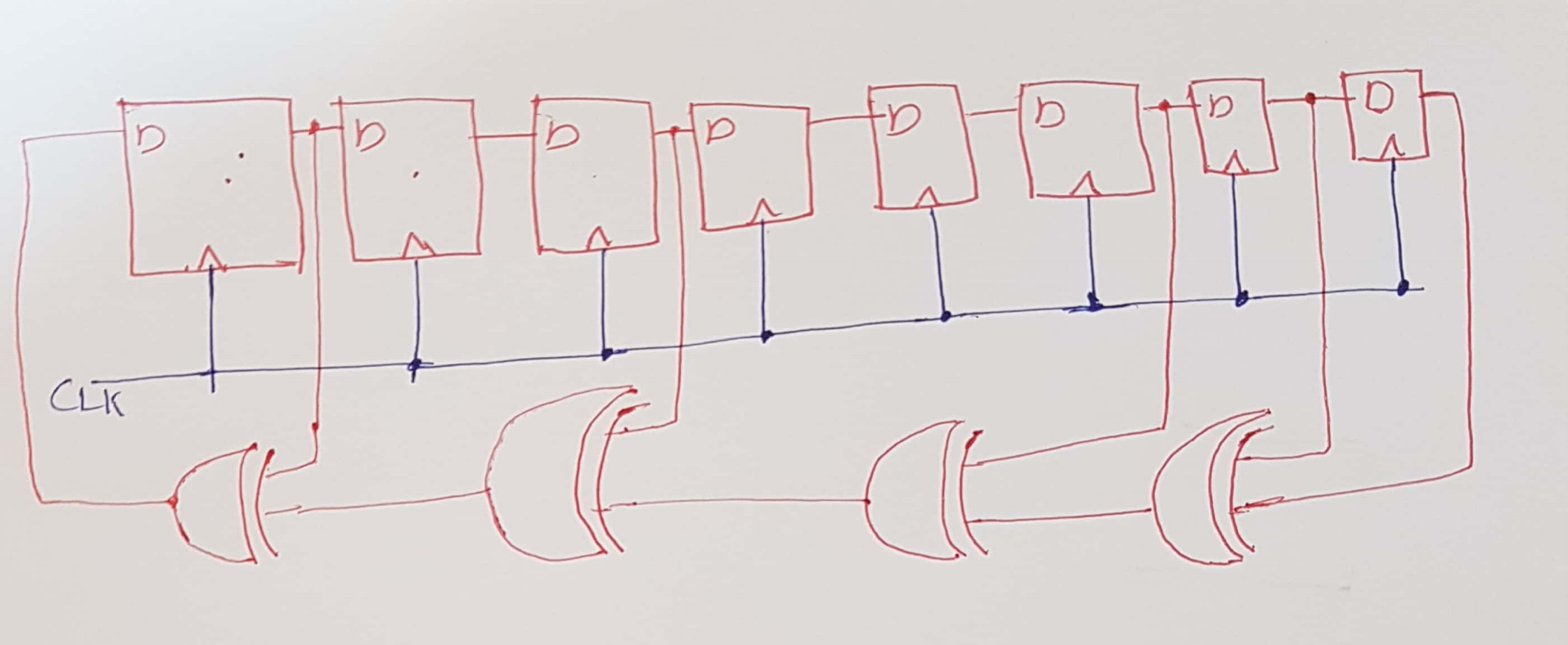


Simulation Result

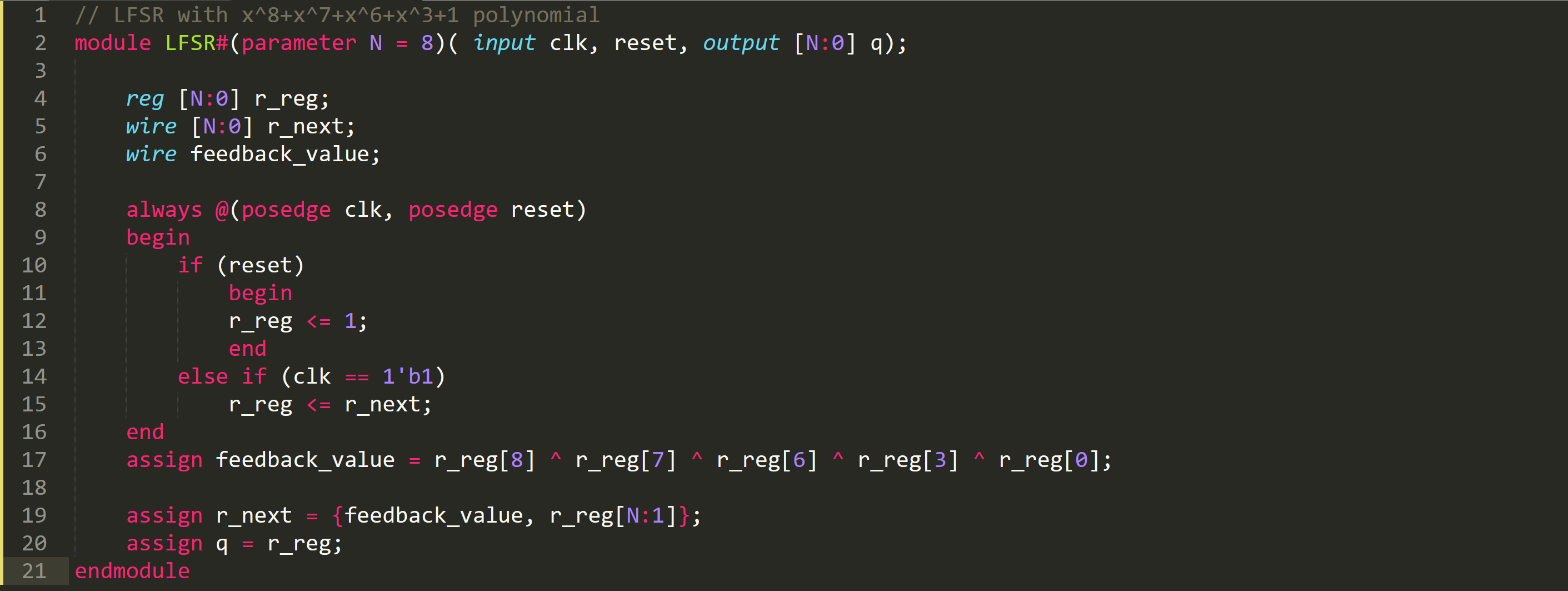


Problem 10

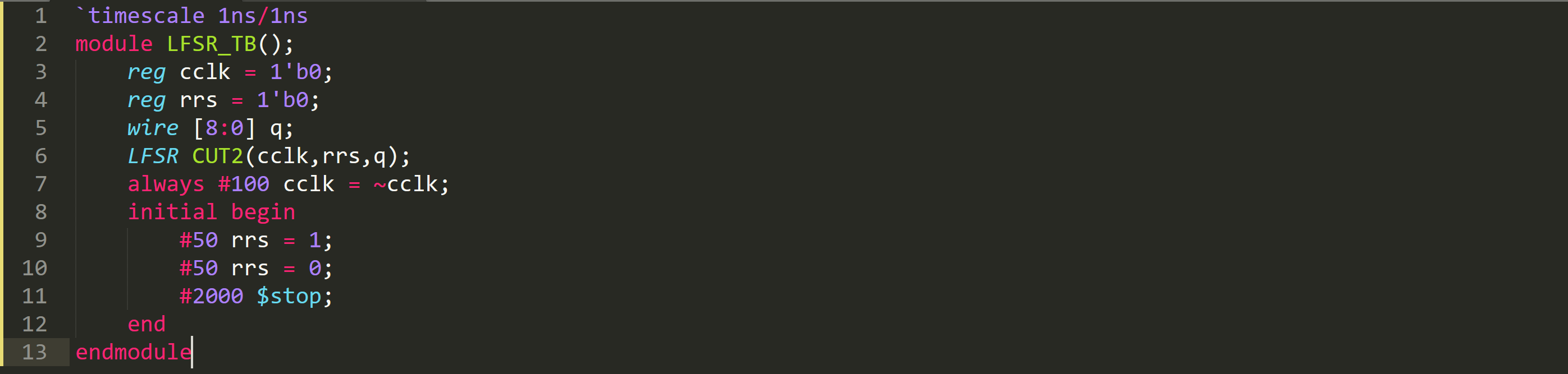
Circuit Diagram



Verilog Code



Testbench



Simulation Result

