

UNIVERSITY OF TEHRAN

Report for Computer Assignment 5

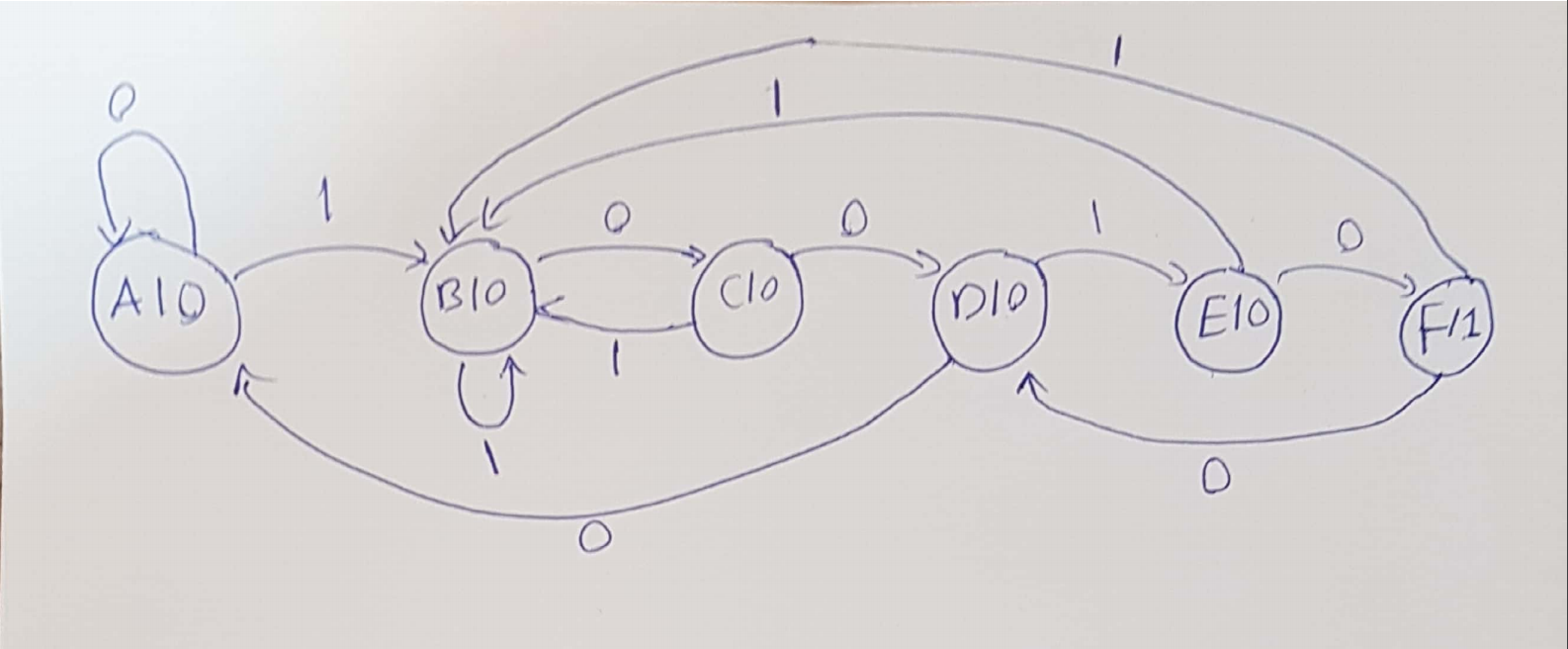
**State Machine Coding, Pre- and Post-Synthesis**

Instructor : Dr. Navabi

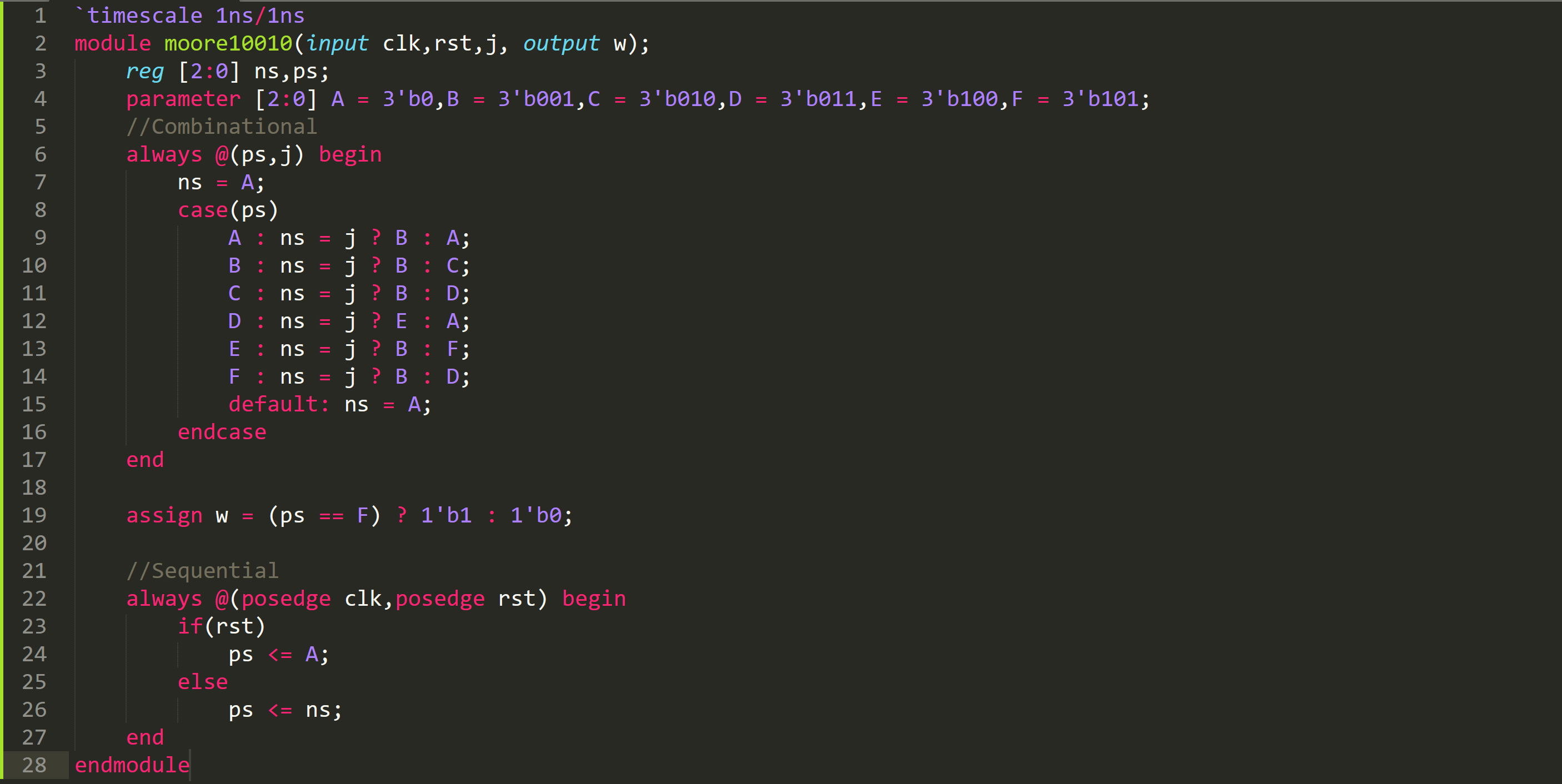
Danial Saeedi

Problem a: 10010 detector

Moore State Diagram

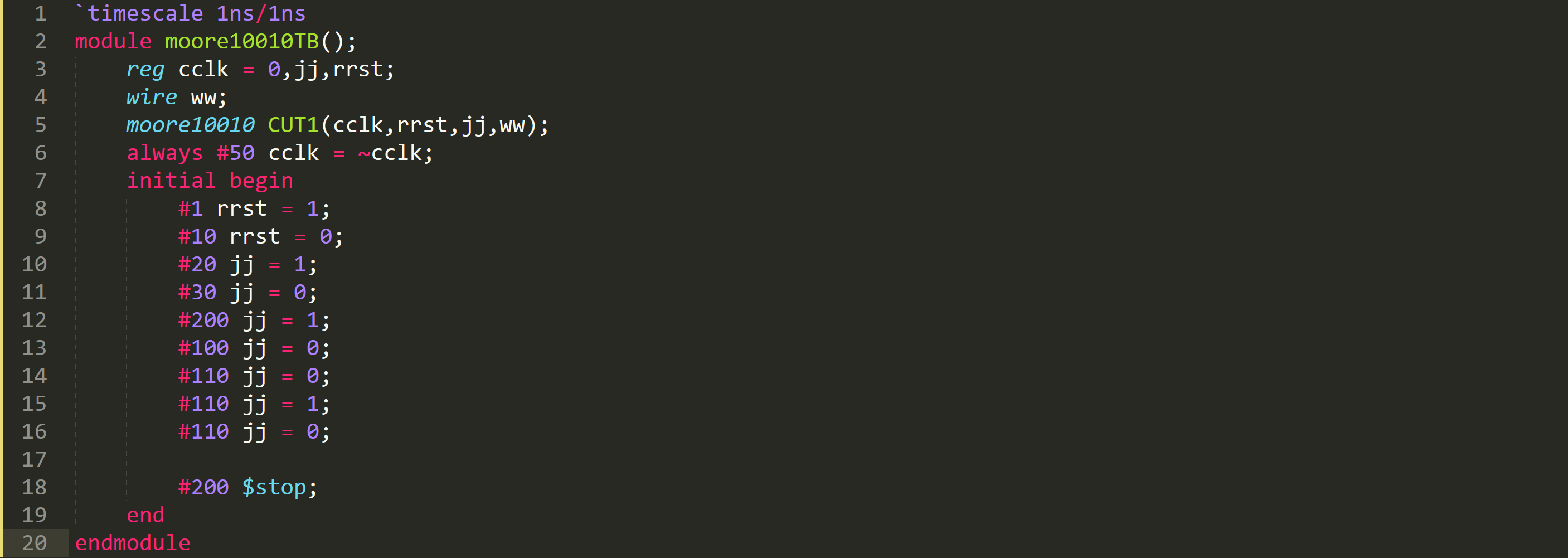


Verilog Code

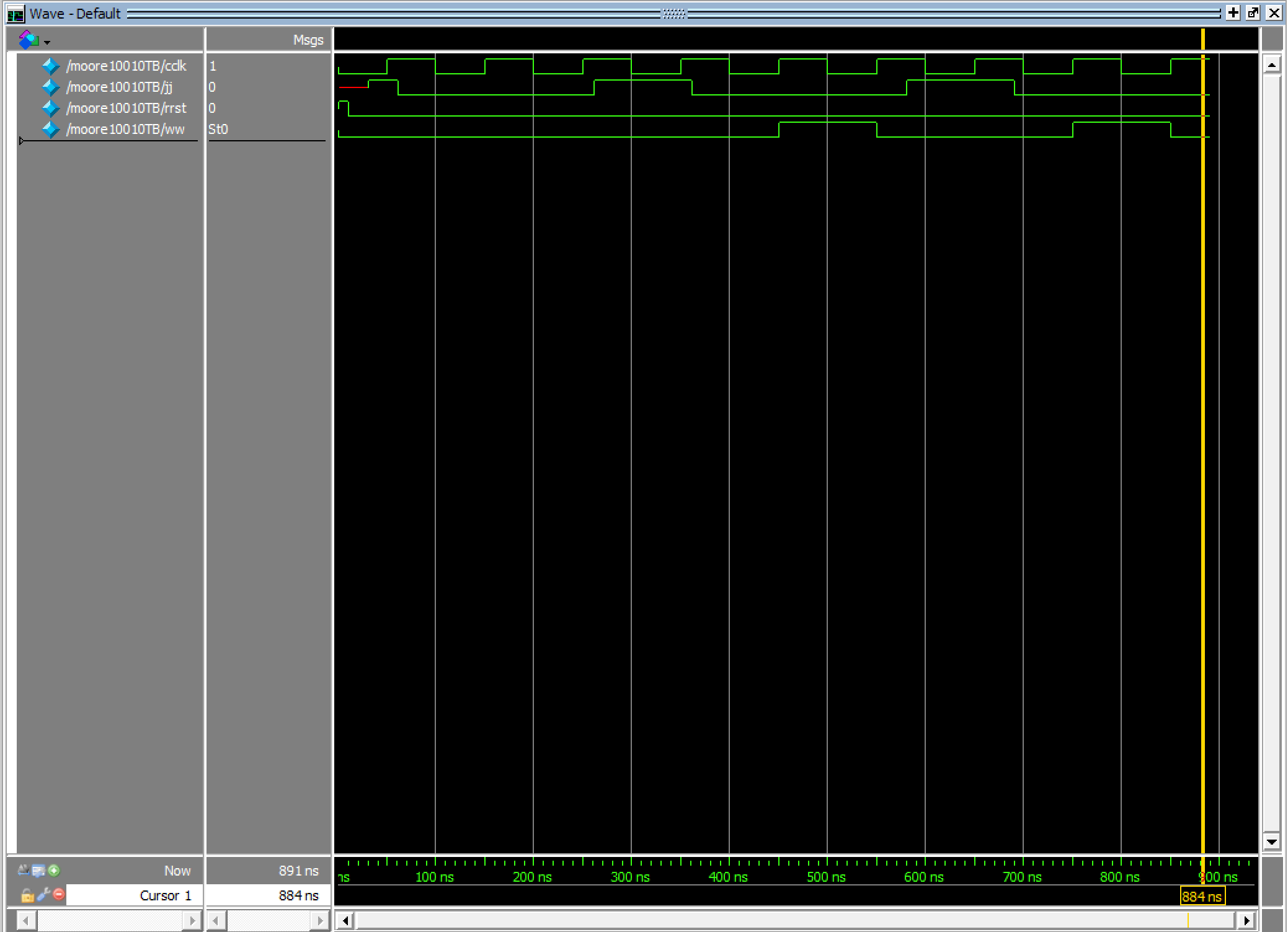


Part i.

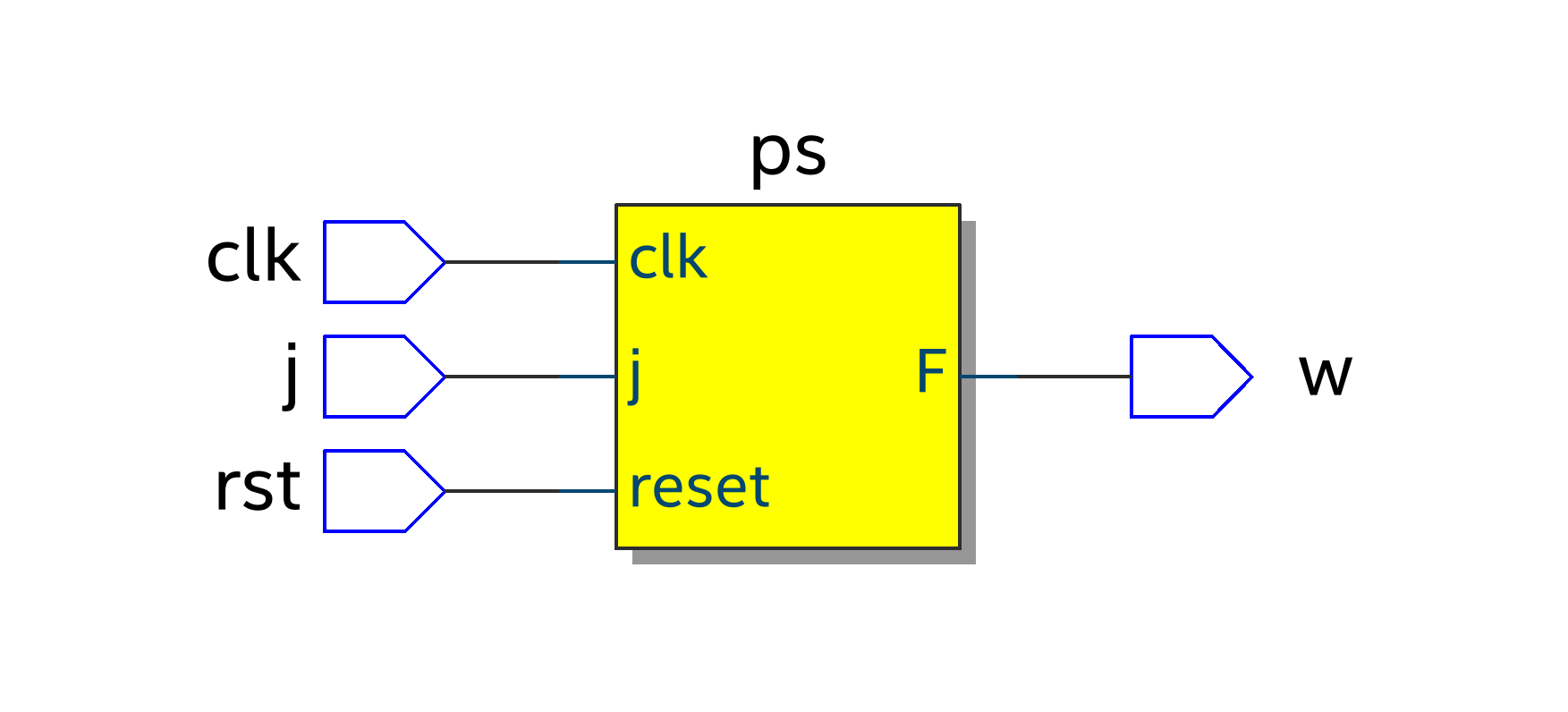
Testbench

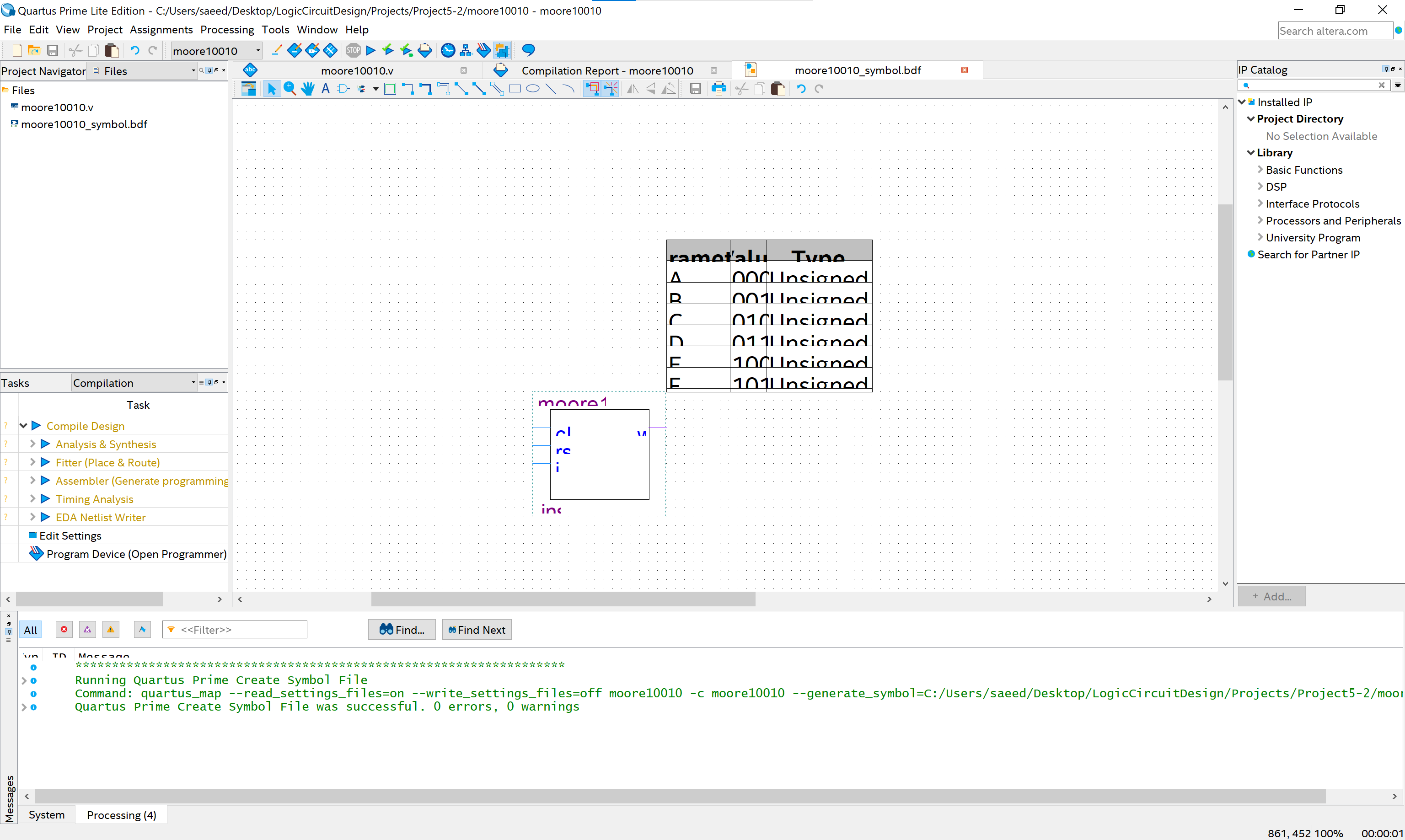


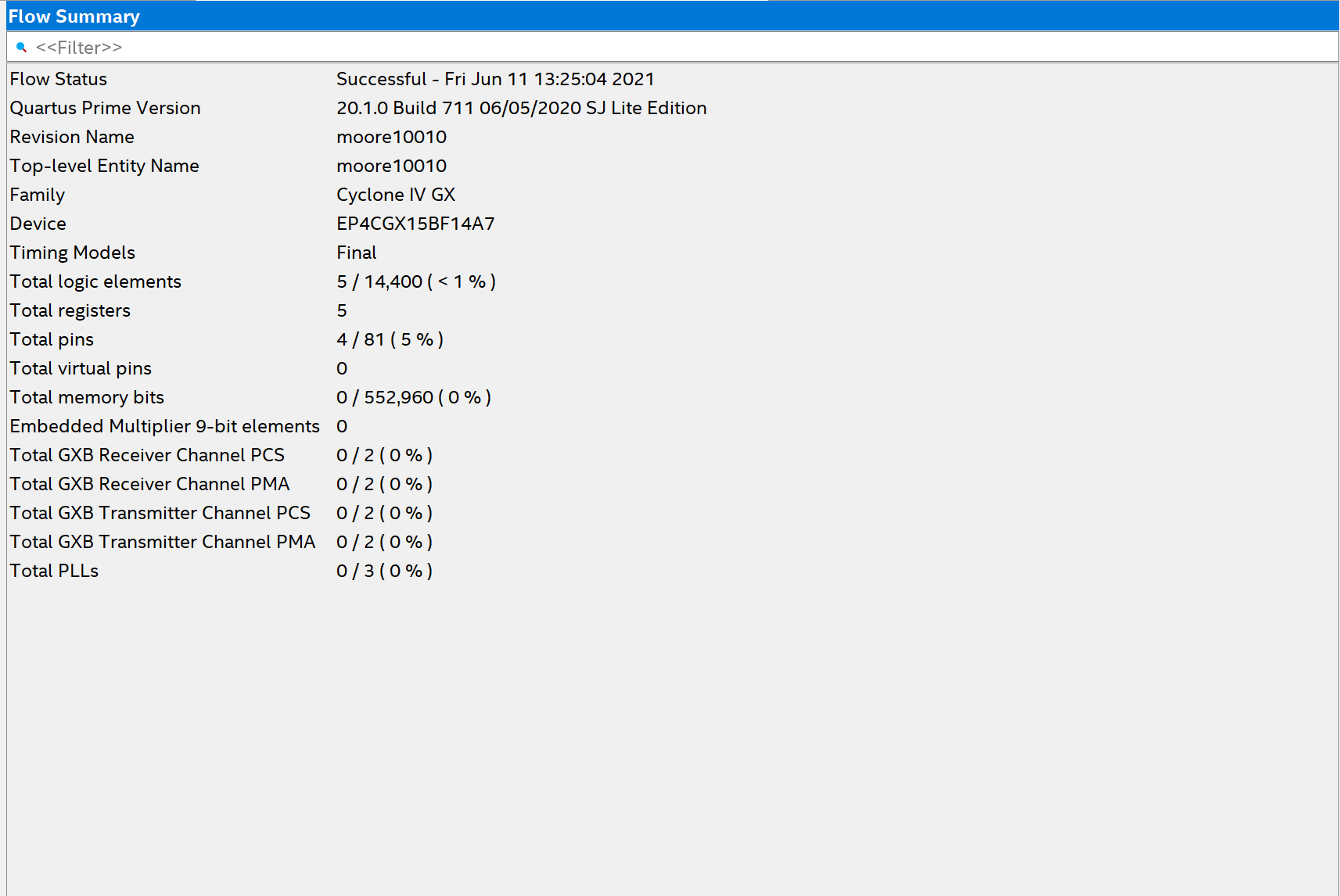
Simulation Result



Part ii.

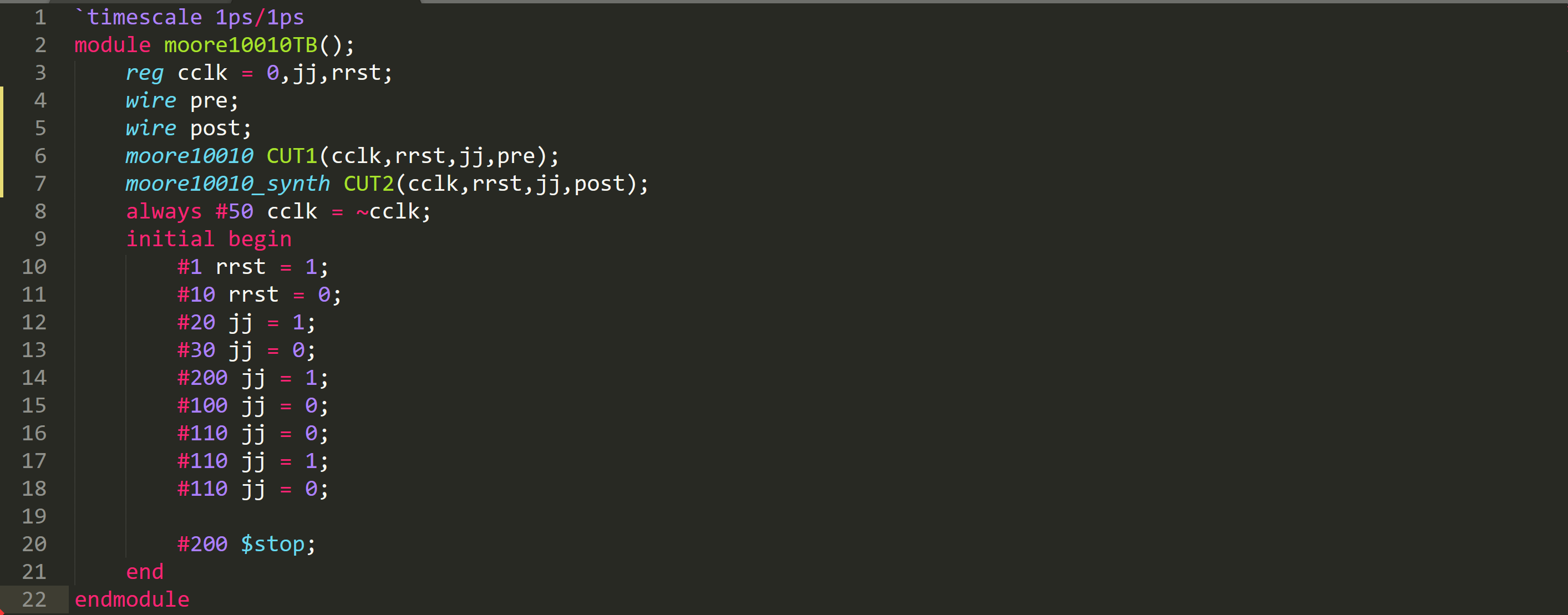




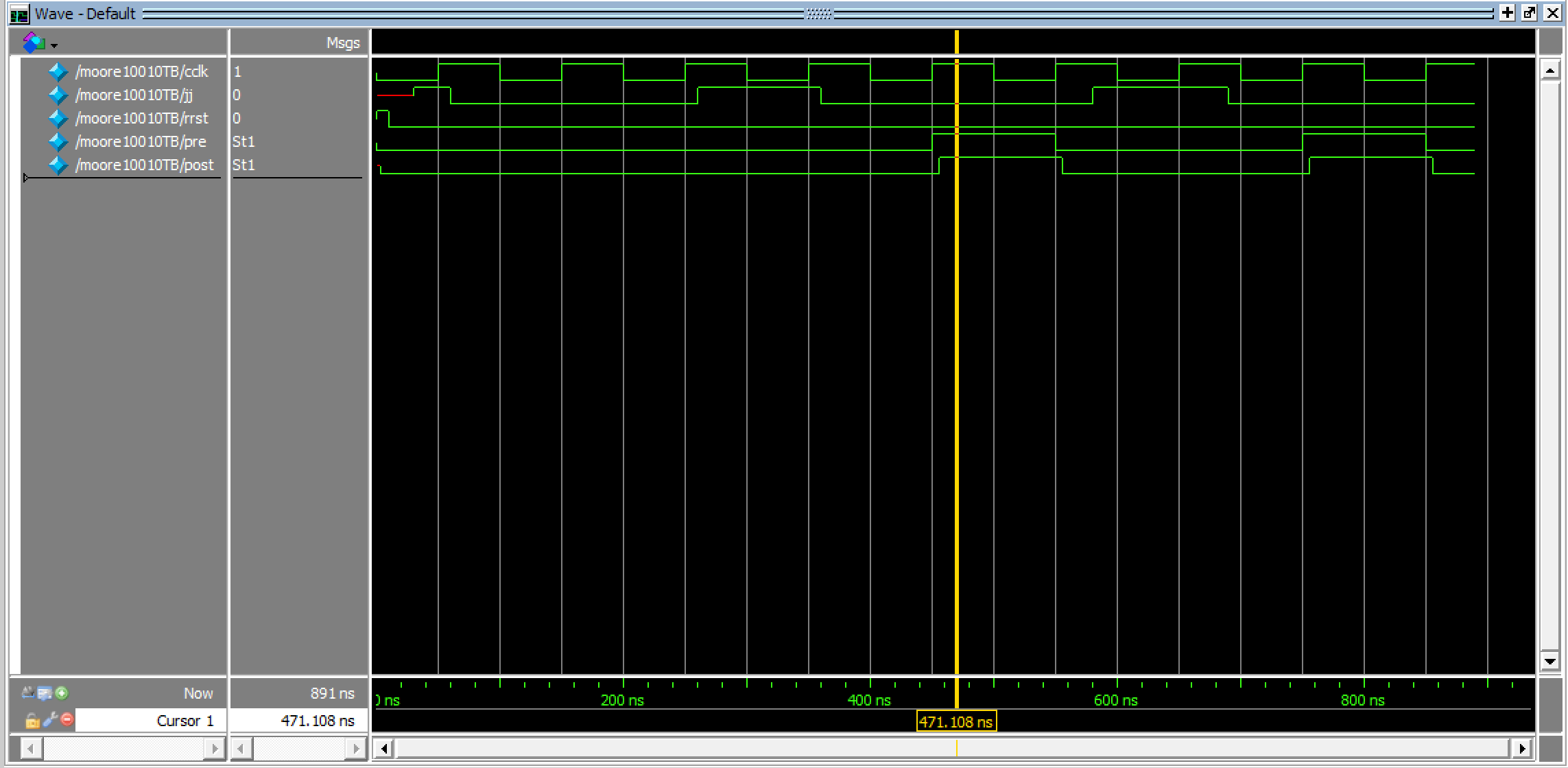


Part iii.

Testbench



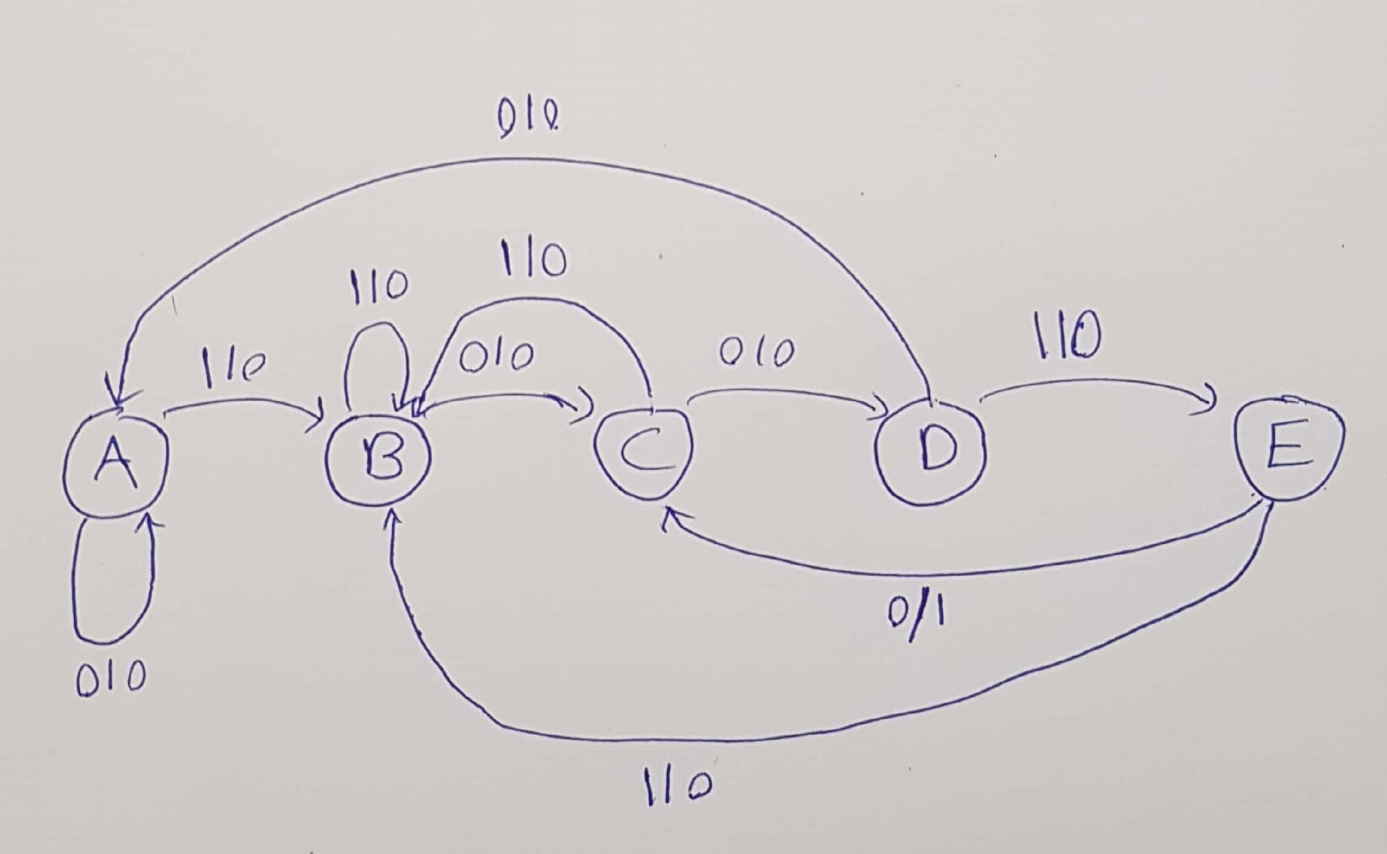
Simulation Result



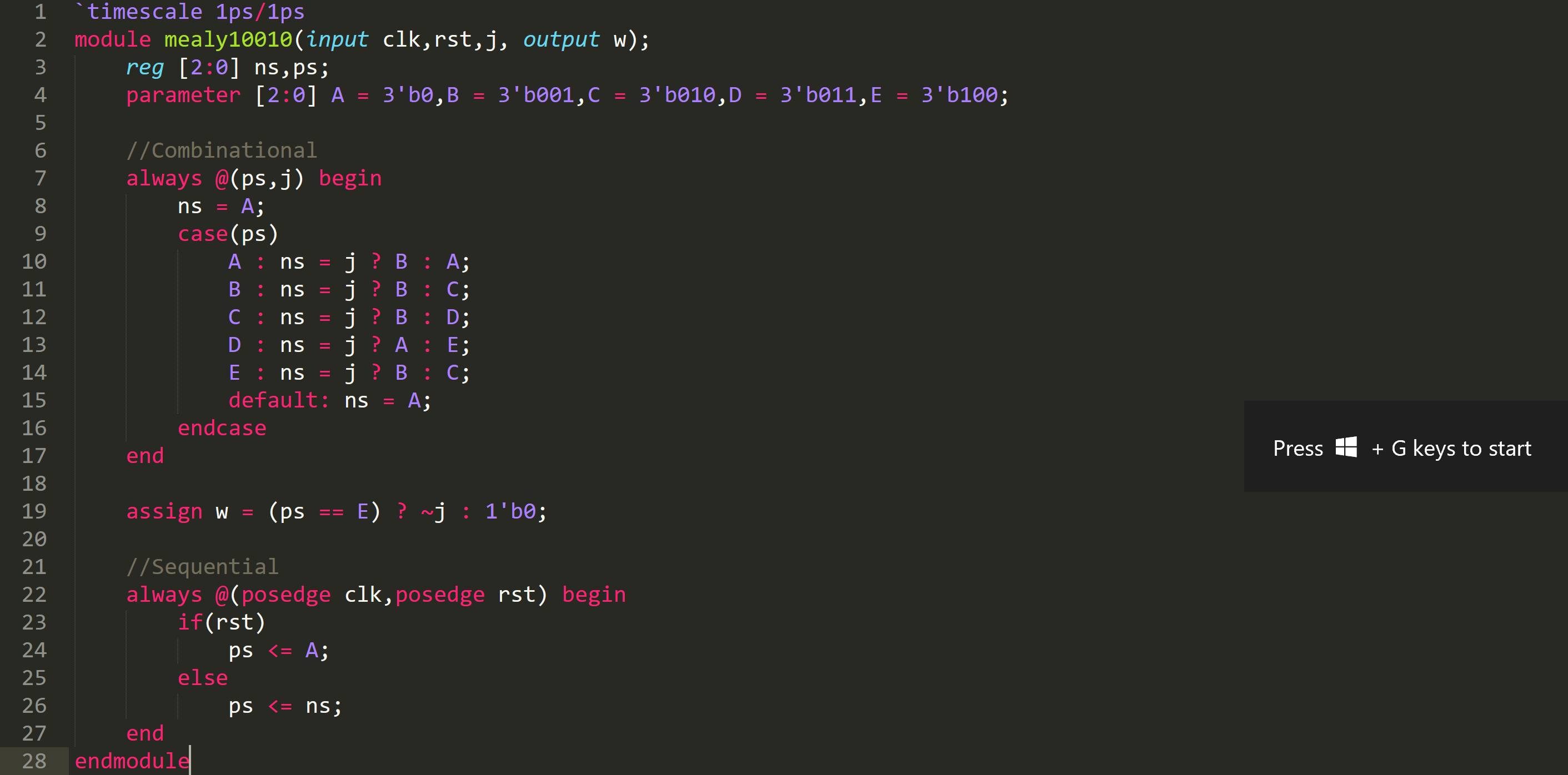
As you can see, the waveform of pre and post synthesis are the same.

Problem b: 10010 detector

Mealy State Diagram

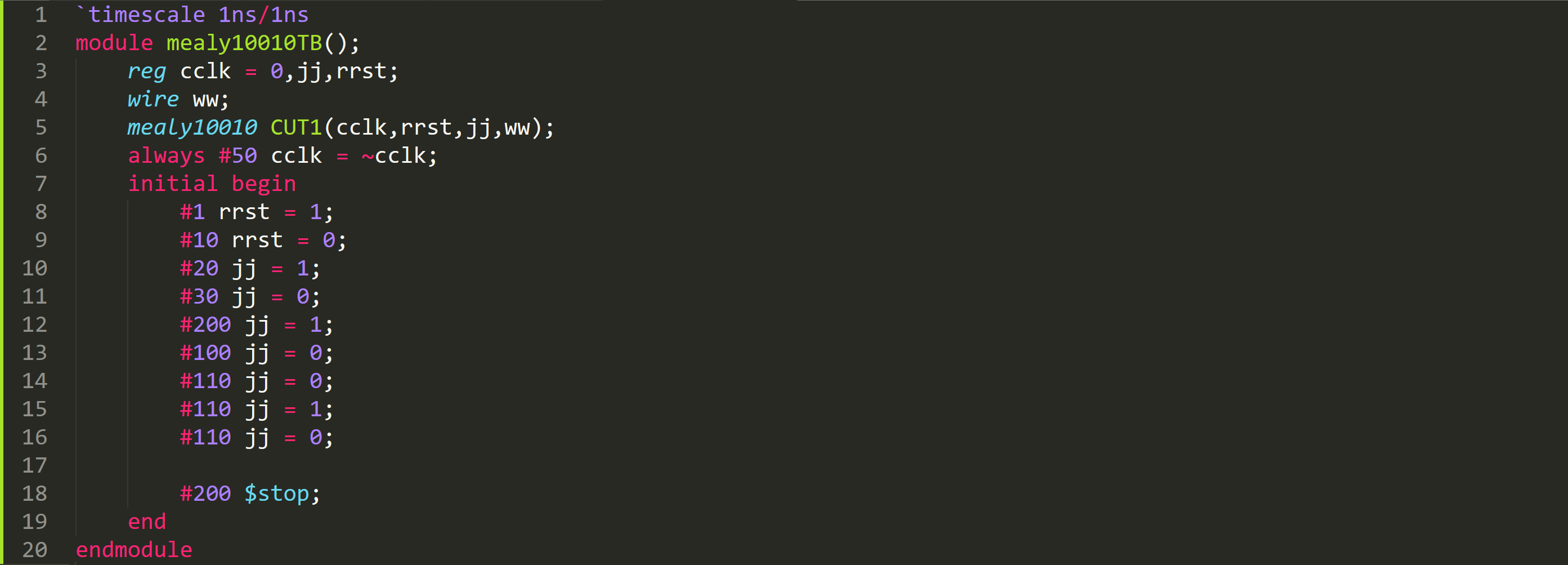


Verilog Code

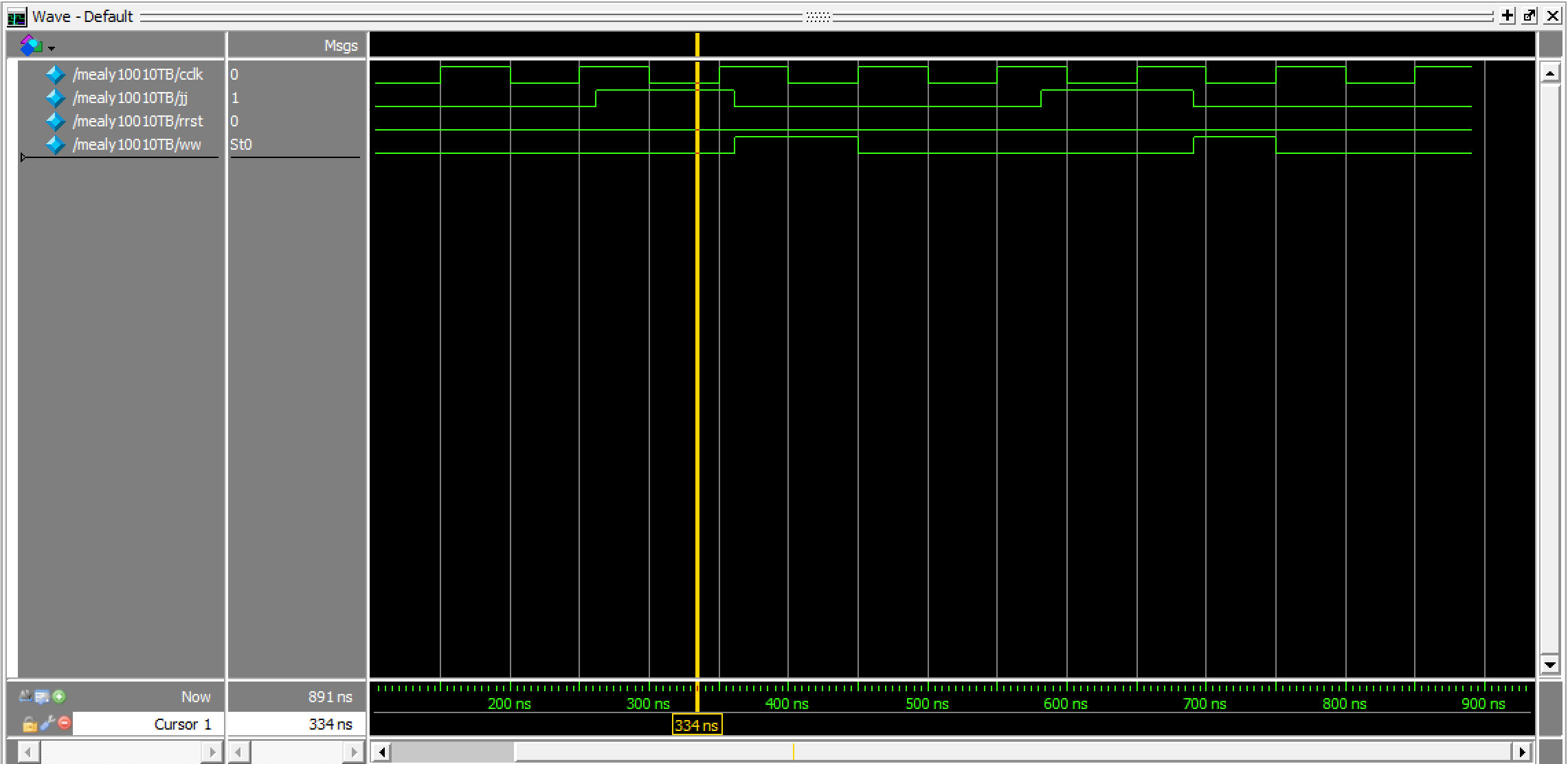


Part i.

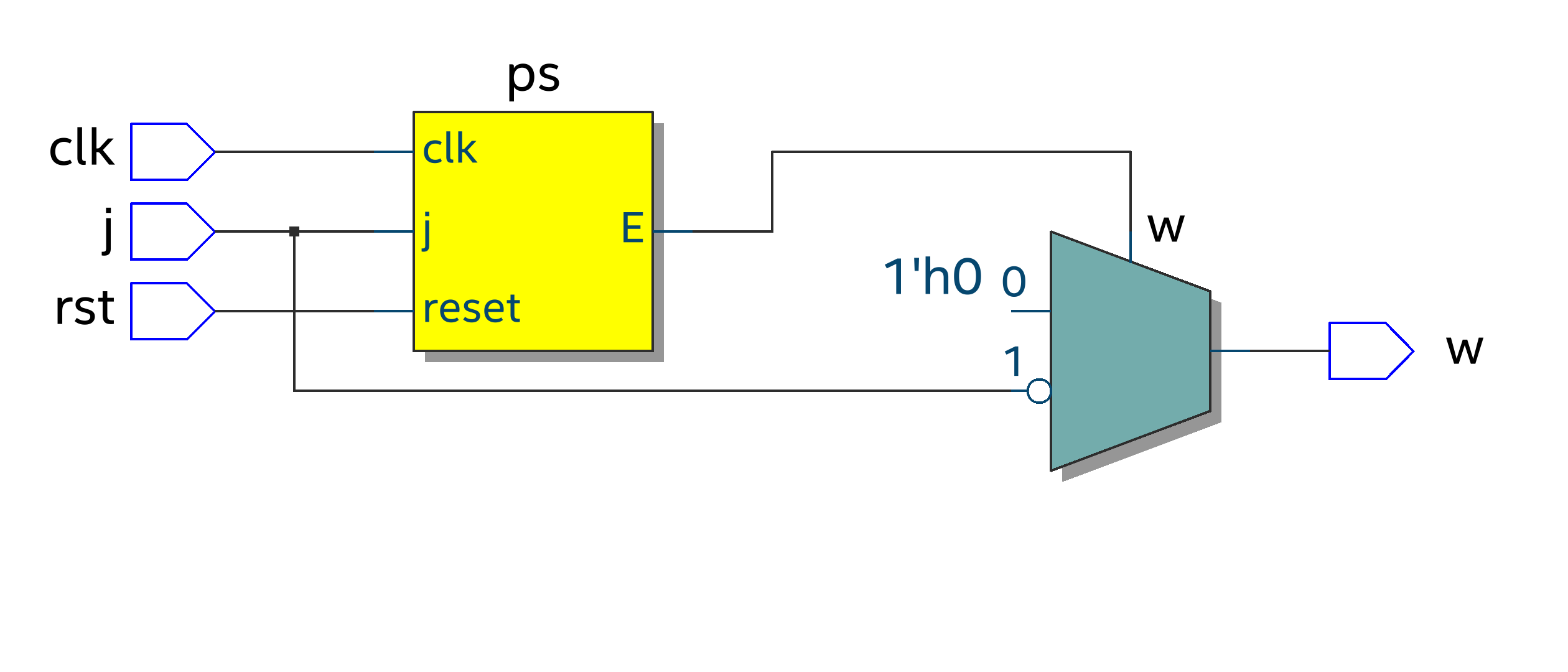
Testbench

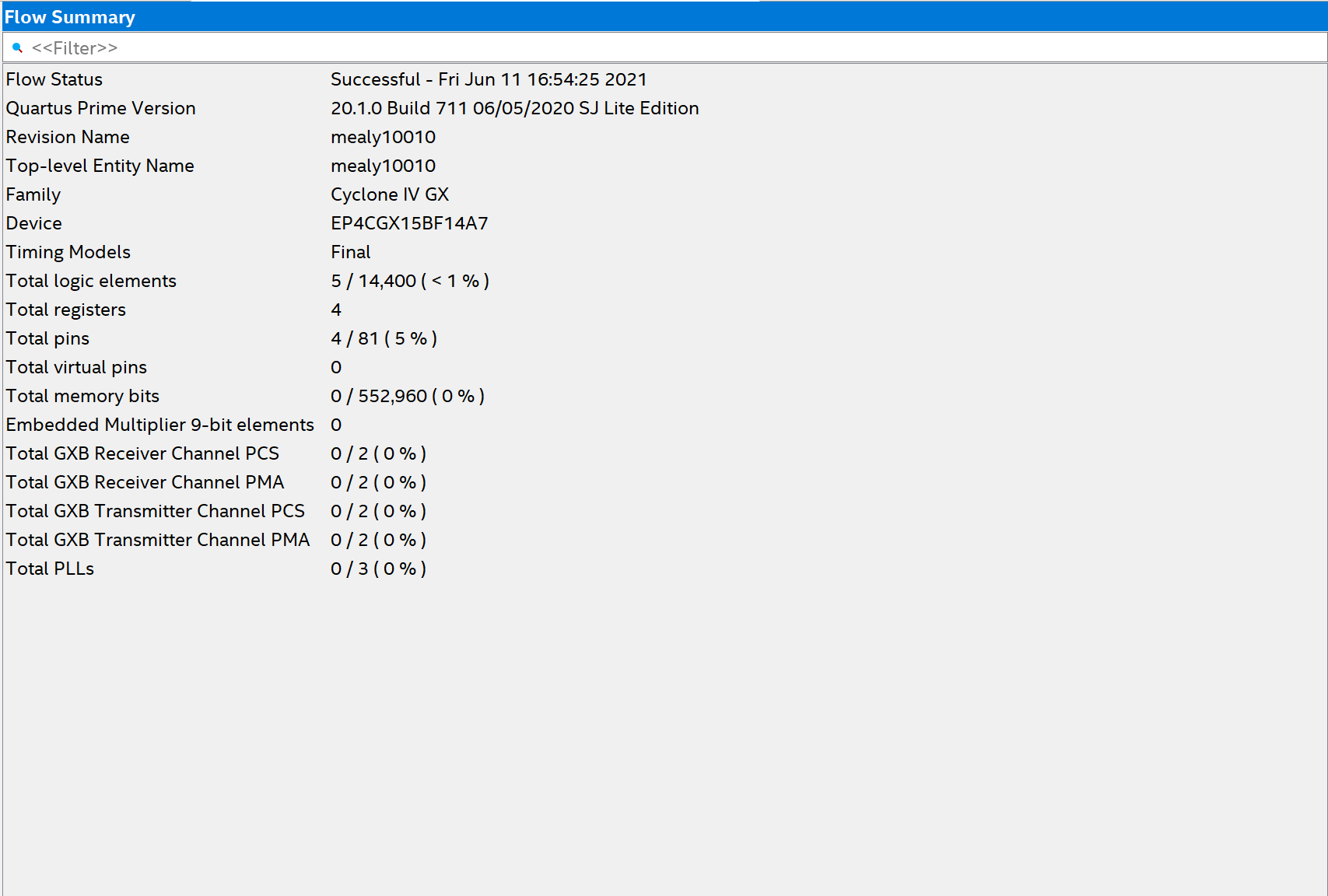


Simulation Result



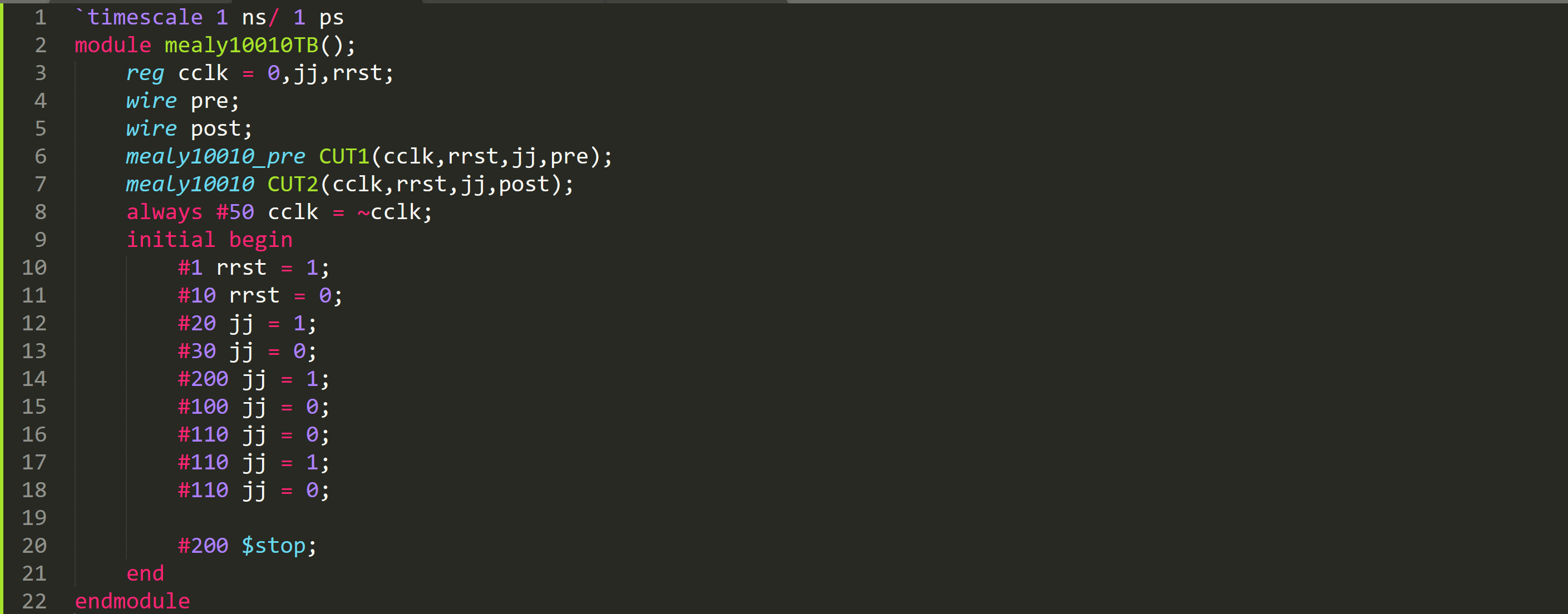
Part ii.



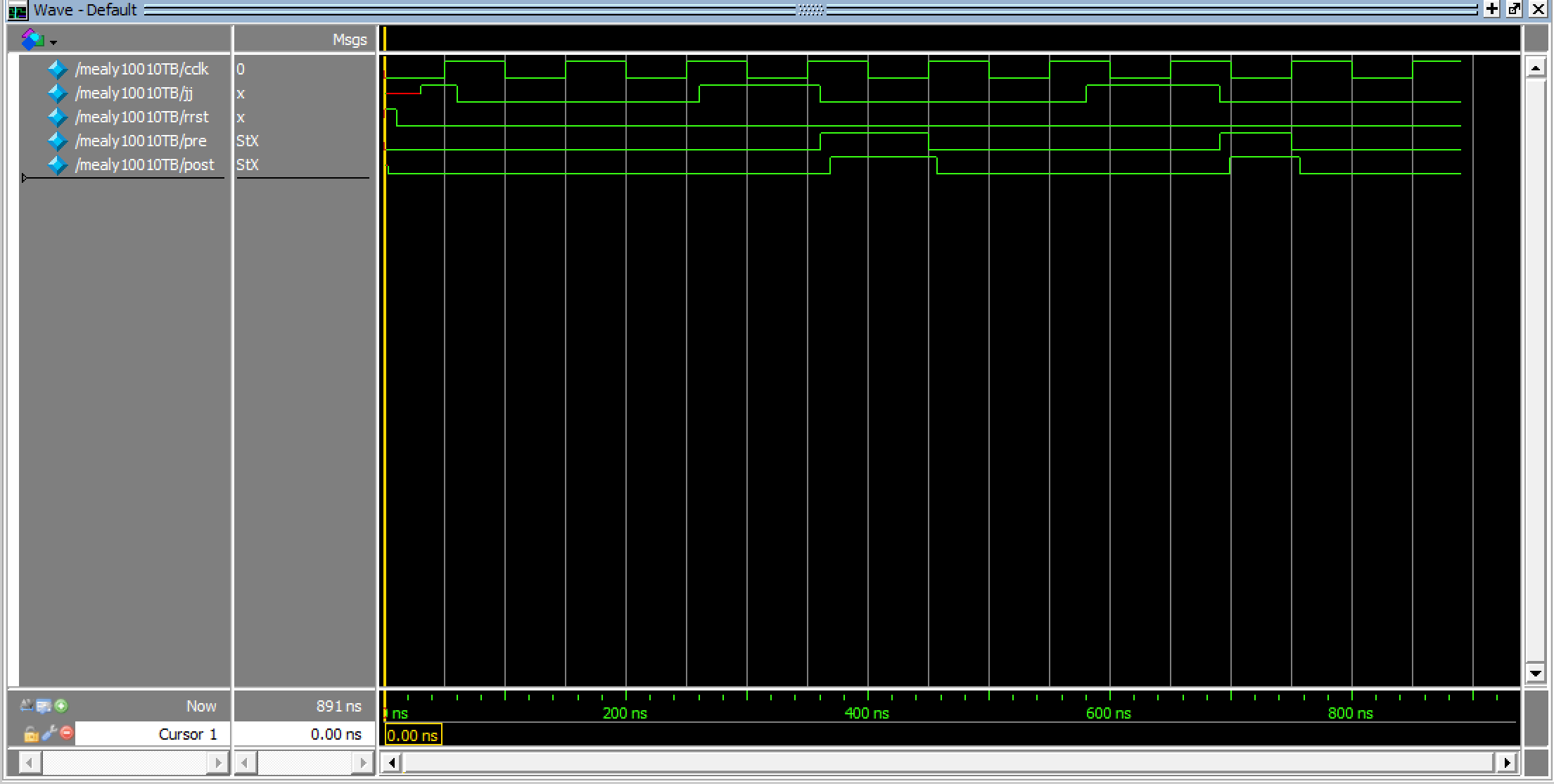


Part iii.

Testbench



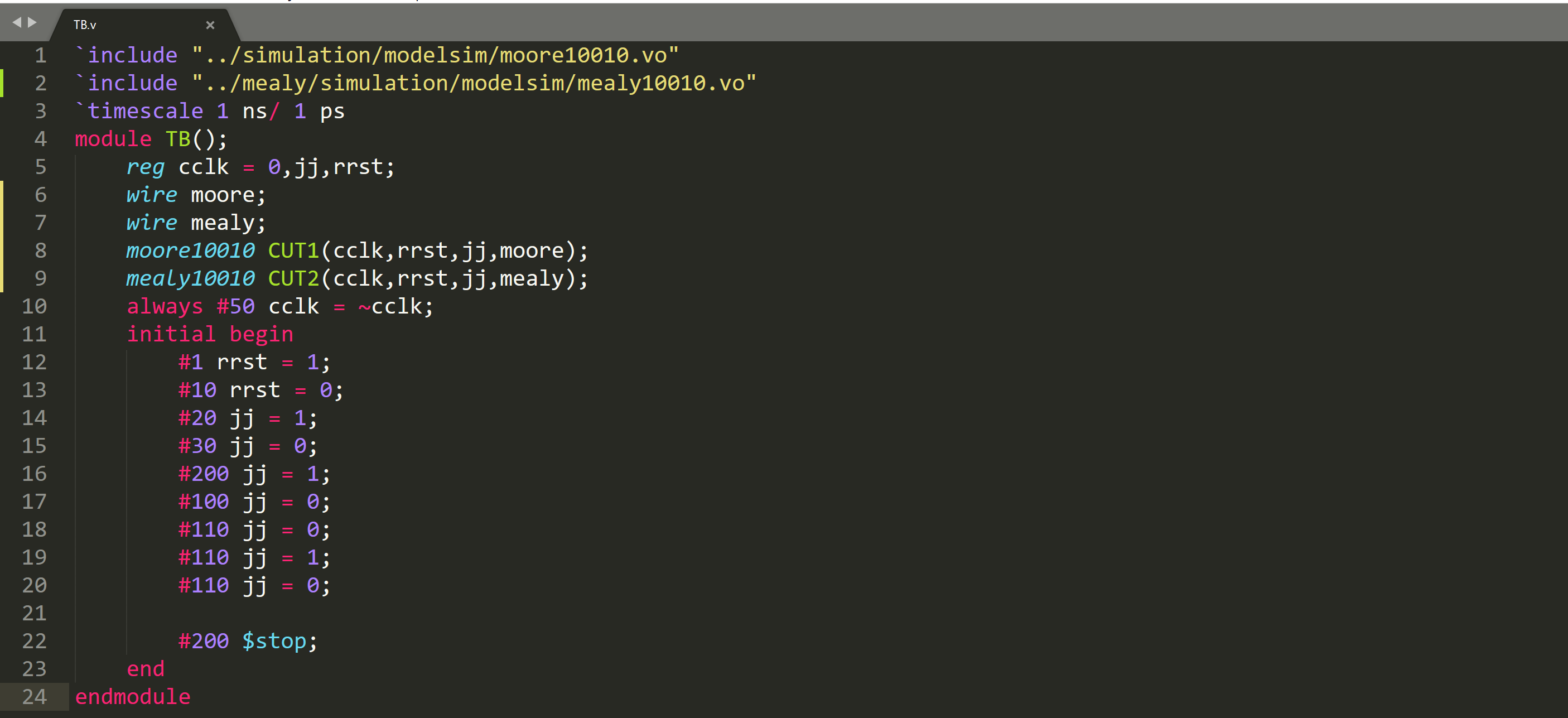
Simulation Result



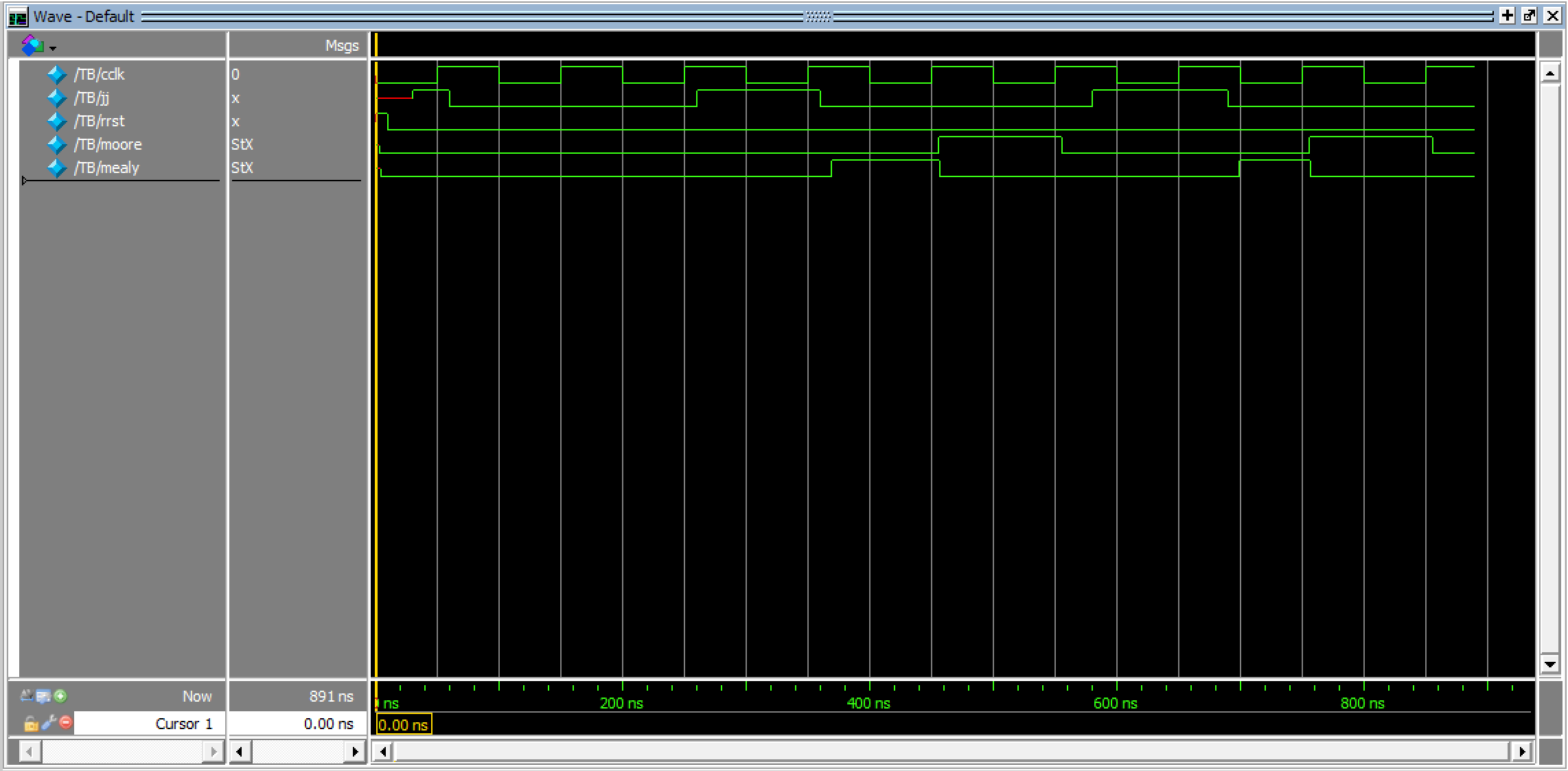
As you can see, the waveform of pre and post synthesis are the same.

Problem C: Compare Moore and Mealy Machine

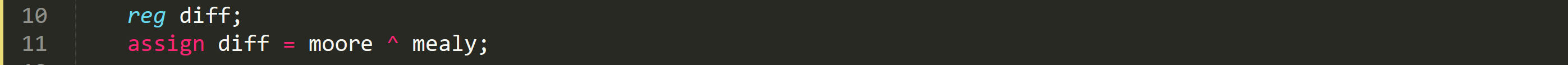
Testbench

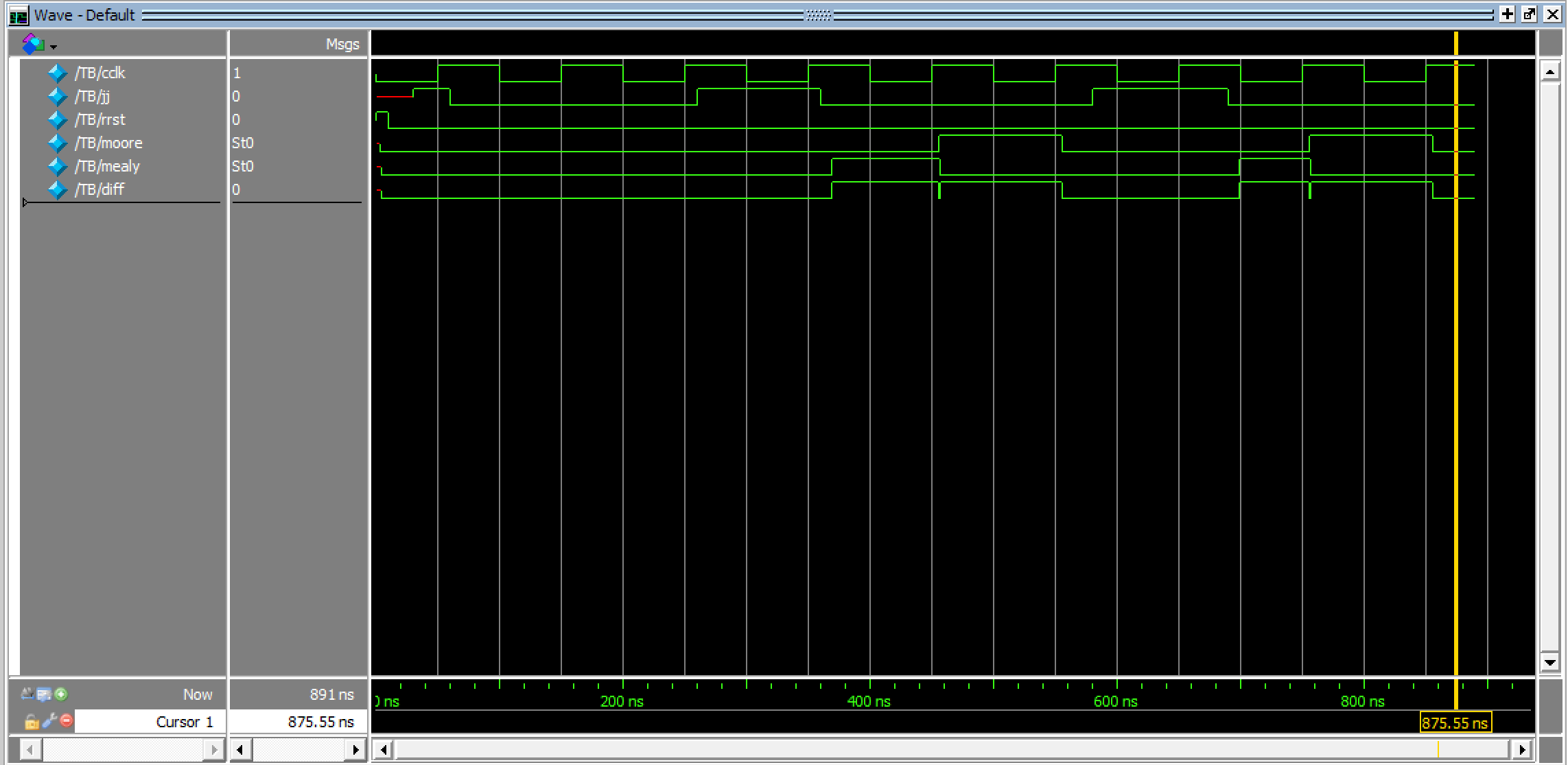


Simulation Result

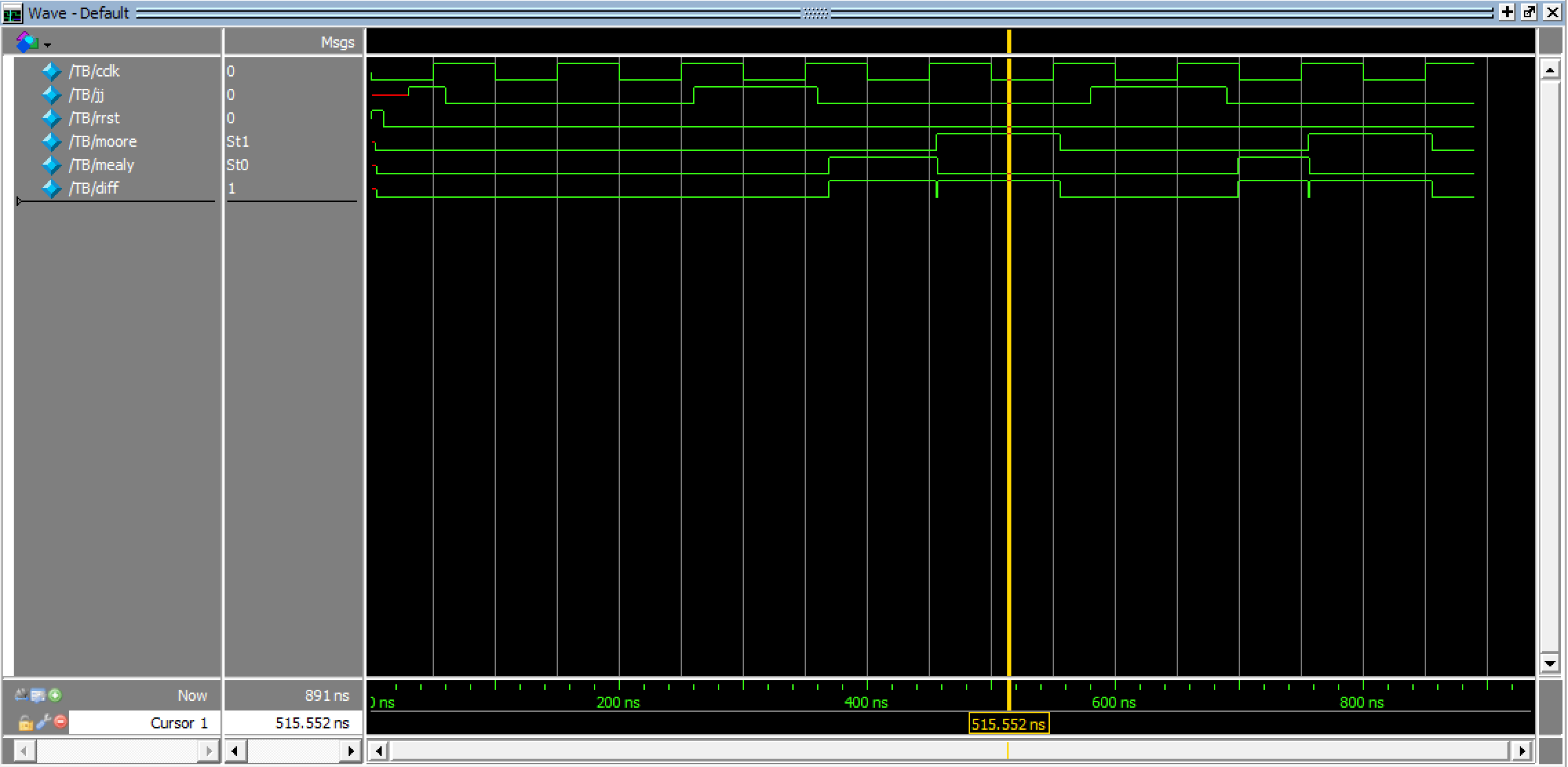


Part i.





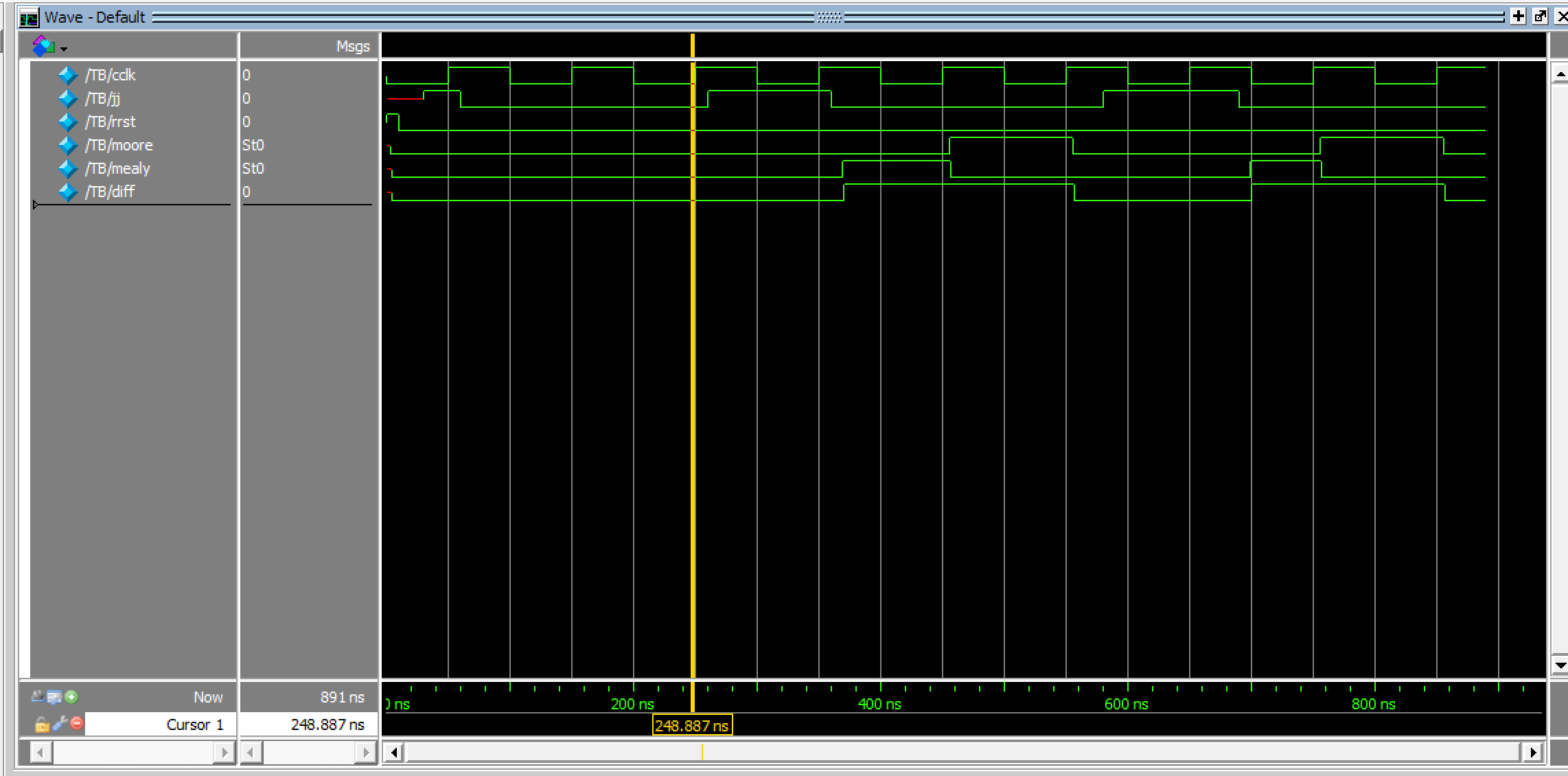
Part ii.



Part iii.

By adding delay to diff, the differences are due to changes on the inputs only:





As you can see there is no glitch anymore.