Header

FPGA UDP Deserializer

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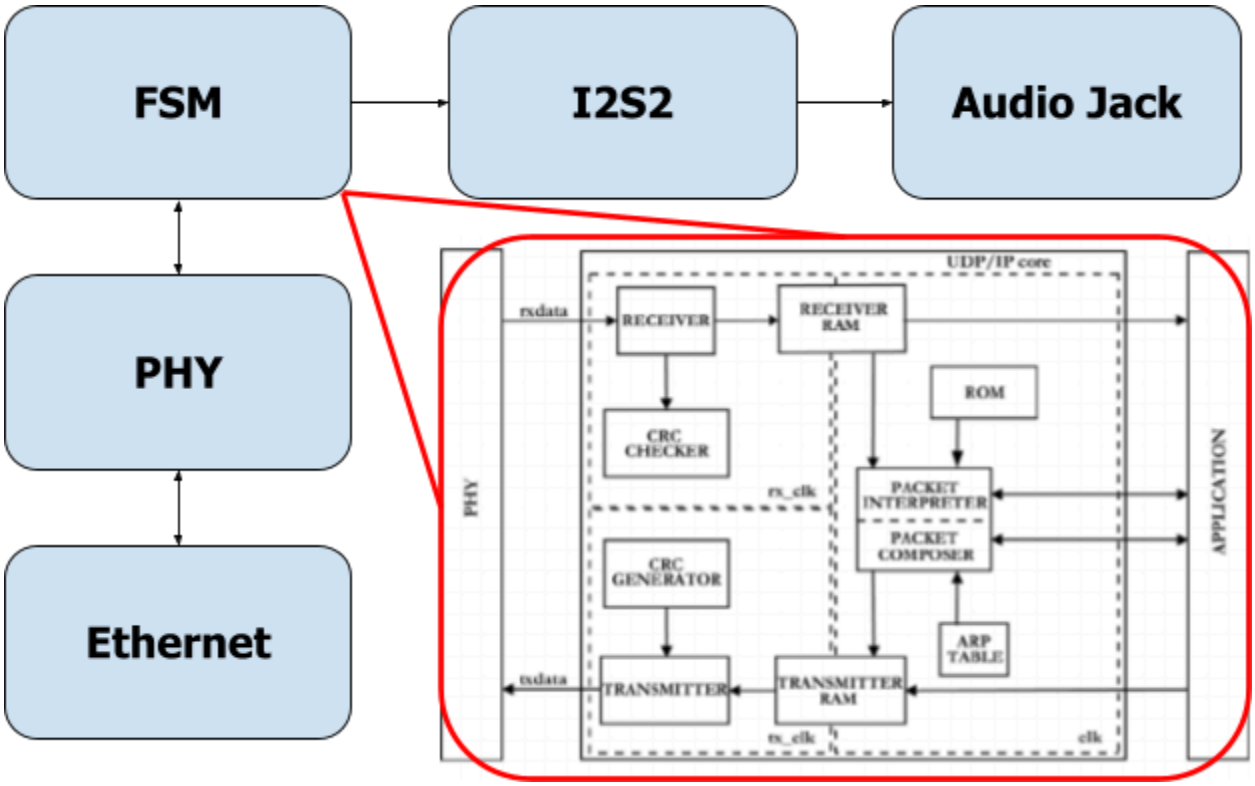
Abstract

Through the power of ~~friendship~~ FPGAs, we will create an FPGA UDP deserializer. Which will allow us to receive information sent over Ethernet to the FPGA. We may then decode this information, such as an audio bitstream, and output it through our I2S2 driver.

Block Diagrams



Description of final documentation deliverable

A UDP Ethernet protocol will be implemented to successfully run at the very least 10 Mbps unidirectionally. As an extension, we may implement more difficult protocols such as TCP/IP, a bidirectional version of UDP, or push the limits of Gbps transfer speed.

External Resources

- Researching the protocols
- “Comparch textbooks”
- Avi

Project Plan

- Describe your minimum viable project - something you could do in a few days with a little help.
  - Flash blinky to an FPGA
  - Make an FSM that does something
  - Get data to work in a very scripted way (synthetic data) or hard coded query stuff
- Stretch goals
  - Add authentication with more advanced cryptography?
  - Speed?
  - Bidirectionality?
  - TCP/IP
- Describe your testing/simulation plan.
  - Loopback testing for different stages of FSM
  - Create memh file of test words to be decoded with packet interpreter module, verify with “expected” file.
  - Use vivado to synthesize modules and view potential warnings/synthesis failures.
- For teams greater than two describe the division of labor
  - Division of work (subject to change):
  - Ari: FSM, always_ff → → →
  - Sid: Packet Decoding, bits and stuff
  - Daniel: OTS-SWE (Off-The-Shelf-SWE) PHY interface 👍
- Known Unknowns - what questions do you want to ask me about how to do your project?
  - How does UDP even work?
  - ~~How feasible is https? Are there hidden pitfalls that would affect us meeting the deadline?~~ (we found this to be too challenging)

Bill of Materials

Item	Vendor	Link	Cost	Quantity	Rationale
Arty A7-(any)T	Digilent	here	$300	1	Ethernet HW
CAT-7 Ethernet Cable	Amazon	here	$16	1	Testing