entity AND2\_tb is

end AND2\_tb;

architecture Behavioral of AND2\_tb is

component AND2

Port (

I0 : in STD\_LOGIC;

I1 : in STD\_LOGIC;

O : out STD\_LOGIC

);

End component;

Signal I0 : std\_logic :=’0’;

Signal I1 : std\_logic :=’0’;

Signal O : std\_logic;

begin

uut:AND2

port map(

I0 => I0,

I1 => I1,

O => O

);

Tb: process

Begin

I0 <= ‘0’;

I1 <= ‘0’;

Wait for 50ns;

I0 <= ‘1’;

I1 <= ‘0’;

Wait for 50ns;

I0 <= ‘0’;

I1 <= ‘1’;

Wait for 50ns;

I0 <= ‘1’;

I1 <= ‘1’;

assert false

report "Fin de la simulación..."

severity failure;

end process;

end Behavioral;