entity AND3\_tb is

end AND3\_tb;

architecture Behavioral of AND3\_tb is

component AND3

Port (

I0 : in STD\_LOGIC;

I1 : in STD\_LOGIC;

I2 : in STD\_LOGIC;

O : out STD\_LOGIC

);

End component;

Signal I0 : std\_logic :=’0’;

Signal I1 : std\_logic :=’0’;

Signal I2 : std\_logic :=’0’;

Signal O : std\_logic;

Begin

uut:AND3

port map(

I0 => I0,

I1 => I1,

I2 => I2,

O => O

);

Tb:PROCESS

BEGIN

I0 <= ‘0’;

I1 <= ‘0’;

I2 <= ‘0’;

Wait for 50ns;

I0 <= ‘1’;

I1 <= ‘0’;

I2 <= ‘0’;

Wait for 50ns;

I0 <= ‘0’;

I1 <= ‘1’;

I2 <= ‘0’;

Wait for 50ns;

I0 <= ‘1’;

I1 <= ‘1’;

I2 <= ‘0’;

Wait for 50ns;

I0 <= ‘0’;

I1 <= ‘0’;

I2 <= ‘1’;

Wait for 50ns;

I0 <= ‘1’;

I1 <= ‘0’;

I2 <= ‘1’;

Wait for 50ns;

I0 <= ‘0’;

I1 <= ‘1’;

I2 <= ‘1’;

Wait for 50ns;

I0 <= ‘1’;

I1 <= ‘1’;

I2 <= ‘1’;

assert false

report "Fin de la simulación..."

severity failure;

END PROCESS;

end Behavioral;