entity Contador\_4b\_tb is

end Contador\_4b\_tb;

architecture behavioral of Contador\_4b\_tb is

component contador\_4b\_td

Port (

UP : in STD\_LOGIC;

DOWN : in STD\_LOGIC;

CLK : in STD\_LOGIC;

LOAD : in STD\_LOGIC;

A0 : in STD\_LOGIC;

A1 : in STD\_LOGIC;

A2 : in STD\_LOGIC;

A3 : in STD\_LOGIC;

RESET : in STD\_LOGIC;

B0 : out STD\_LOGIC;

B1 : out STD\_LOGIC;

B2 : out STD\_LOGIC;

B3 : out STD\_LOGIC;

Q : out STD\_LOGIC;

Q\_N: out STD\_LOGIC

);

End component;

Signal UP : STD\_LOGIC :=’0’;

Signal DOWN : STD\_LOGIC :=’0’;

Signal CLK : STD\_LOGIC;

Signal LOAD : STD\_LOGIC :=’0’;

Signal A0 : STD\_LOGIC :=’0’;

Signal A1 : STD\_LOGIC :=’0’;

Signal A2 : STD\_LOGIC :=’0’;

Signal A3 : STD\_LOGIC :=’0’;

Signal RESET : STD\_LOGIC :=’0’;

Signal B0 : STD\_LOGIC;

Signal B1 : STD\_LOGIC;

Signal B2 : STD\_LOGIC;

Signal B3 : STD\_LOGIC;

Signal Q : STD\_LOGIC;

Signal Q\_N: STD\_LOGIC;

Begin

Uut:Contador\_4b

Port map(

UP => UP,

DOWN => DOWN,

CLK =>CLK,

LOAD => LOAD,

A0 => A0,

A1 => A1,

A2 => A2,

A3 => A3,

RESET => RESET,

B0 => B0,

B1 => B1,

B2 => B2,

B3 => B3,

Q => Q,

Q\_N => Q\_N

);

Tb: process

Begin

UP <=’1’;

Wait for 150ns;

Up <=’0’;

Down <= ‘1’;

Wait for 50ns;

Down <= ‘0’;

Reset <=’1’;

A0 <= ‘1’;

A1 <= ‘1’;

A2 <= ‘1’;

A3 <= ‘1’;

Wait for 50ns;

Reset <= ‘0’;

Load <= ‘1’;

Wait for 50ns;

Load <= ‘0’;

Down <= ‘1’;

Wait for 200ns

assert false

report "Fin de la simulación..."

severity failure;

end process;

end Behavioral;