entity FFJK\_tb is

end FFJK\_tb;

architecture Behavioral of FFJK\_tb is

component FFJK

Port (

J : in STD\_LOGIC;

K : in STD\_LOGIC;

CLK : in STD\_LOGIC;

LOAD : in STD\_LOGIC;

RESET : in STD\_LOGIC;

PRE\_CARGA : in STD\_LOGIC;

Q : out STD\_LOGIC;

Q\_N : out STD\_LOGIC

);

End component;

signal J : STD\_LOGIC :=’0’;

signal K : STD\_LOGIC :=’0’;

signal CLK : STD\_LOGIC;

signal LOAD : STD\_LOGIC :=’0’;

signal RESET : STD\_LOGIC :=’0’;

signal PRE\_CARGA : STD\_LOGIC :=’0’;

signal Q : STD\_LOGIC;

signal Q\_N : STD\_LOGIC;

begin

uut: FFJK

port map(

J => J,

K => K,

CLK => CLK,

LOAD => LOAD,

RESET => RESET,

PRE\_CARGA => PRE\_CARGA,

Q => Q,

Q\_N => Q\_N

);

Tb: process

Begin

Wait for 100ns;

J <=’1’;

K <=’0’;

Wait for 100ns;

J <=’0’;

K <=’1’;

Wait for 100ns;

J <=’1’;

K <=’1’;

Wait for 100ns;

J <=’0’;

K <=’0’;

Wait for 20ns;

RESET<=’1’;

Wait for 30ns;

RESET<=’0’;

PRE\_CARGA<=’1’;

Wait for 100ns;

LOAD<=’1’;

assert false

report "Fin de la simulación..."

severity failure;

end Behavioral;